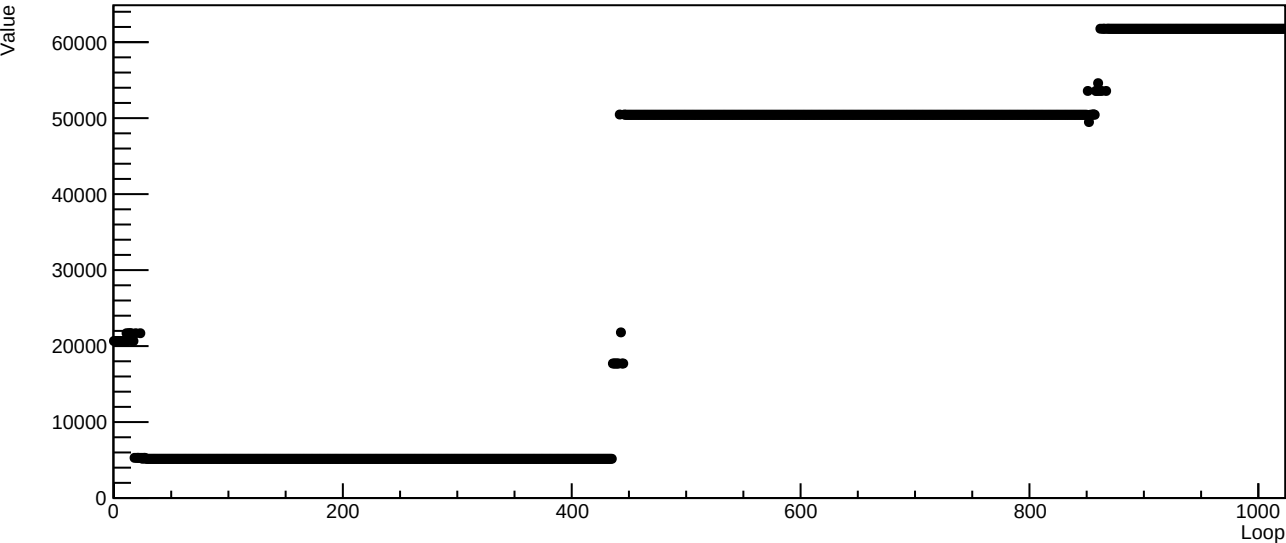
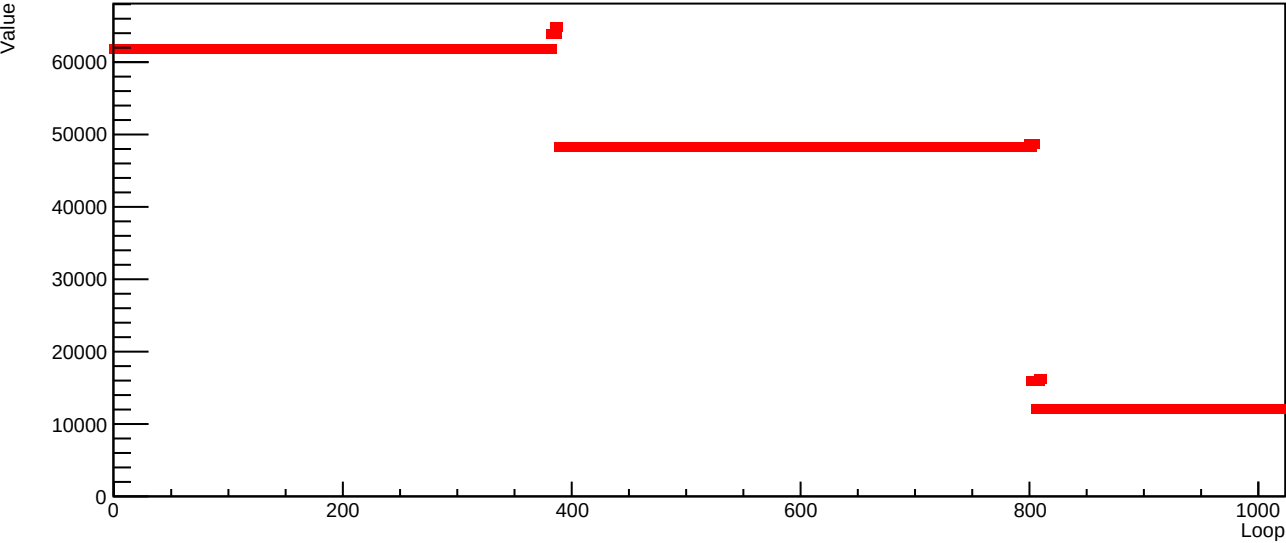


DCL timing2-reset1.out MCM0



DCL timing2-reset1.out MCM1



DCL timing2-reset1.out MCM2

