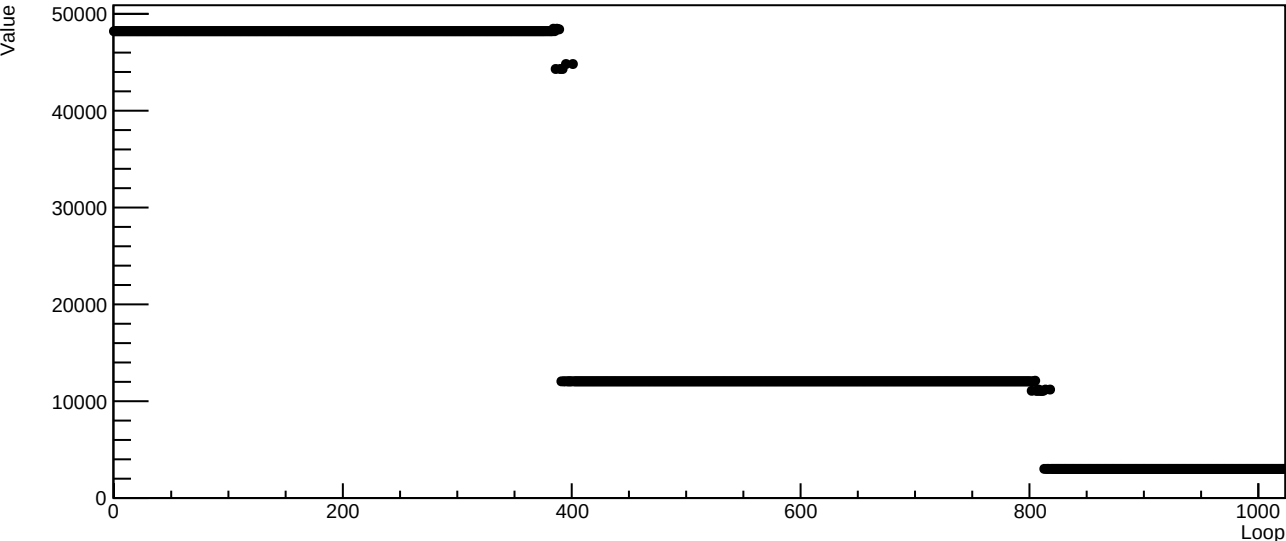
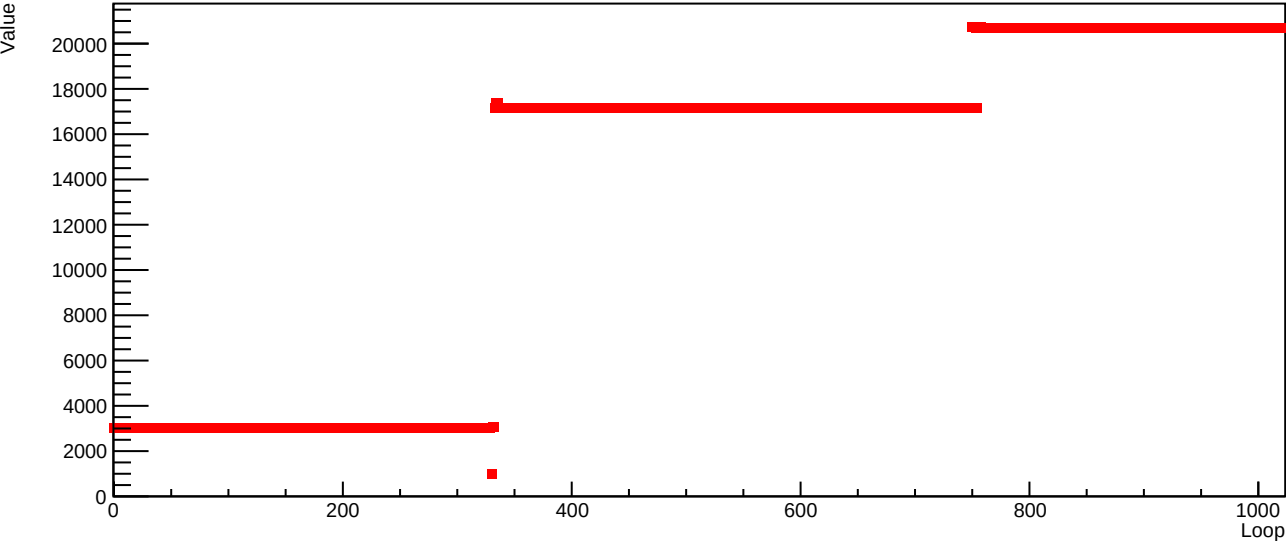


DCL timing2-reset2.out MCM0



DCL timing2-reset2.out MCM1



DCL timing2-reset2.out MCM2

