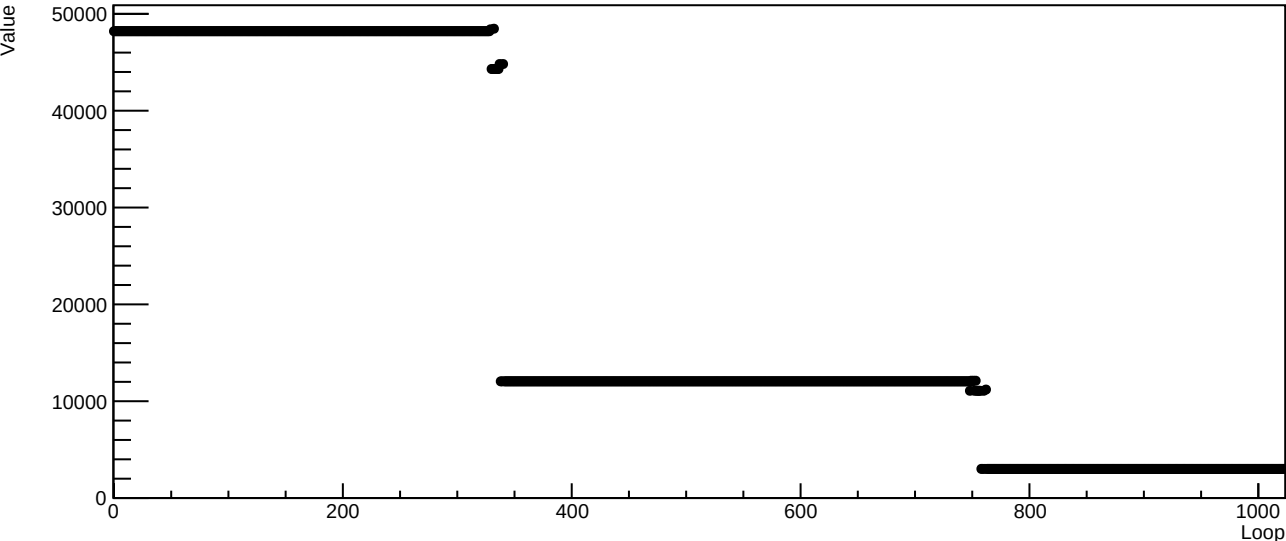
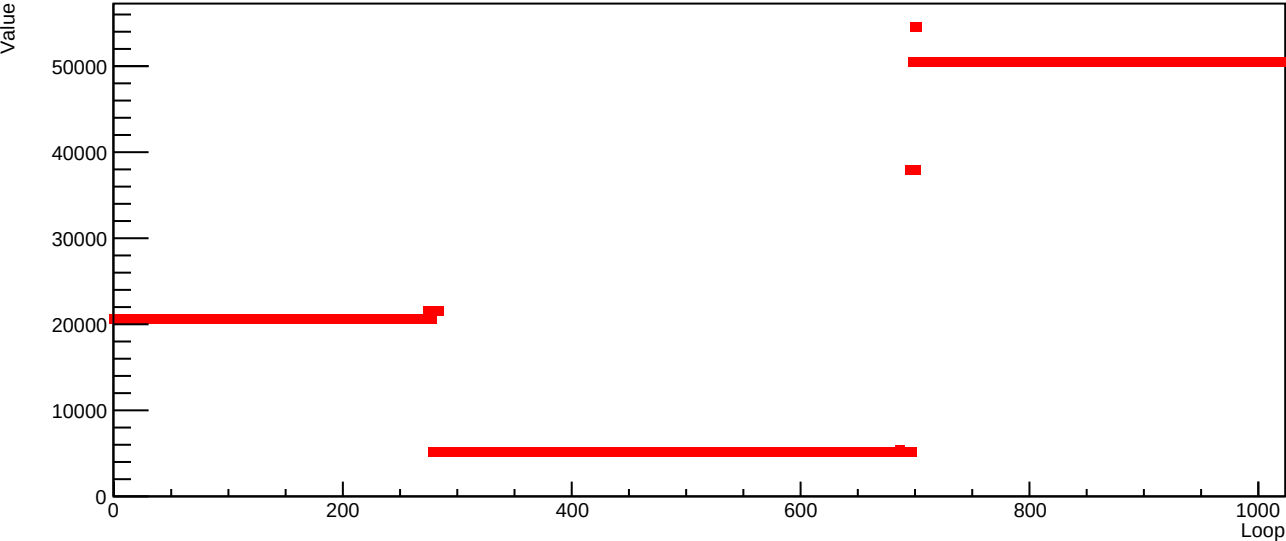


DCL timing4-reset1.out MCM0



DCL timing4-reset1.out MCM1



DCL timing4-reset1.out MCM2

