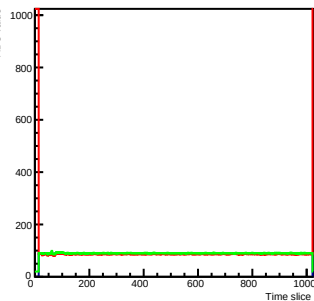
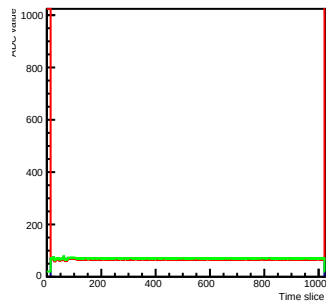


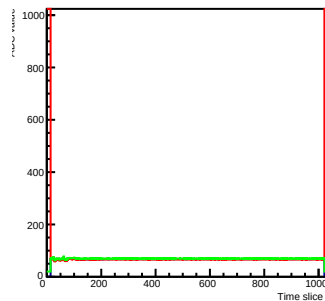
Run 0 Time mcm 0 chip 0 chan 0 s0



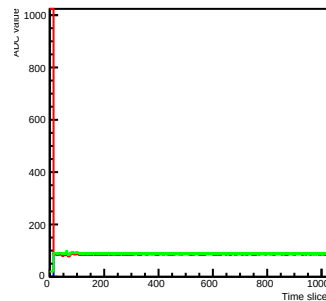
Run 0 Time mcm 0 chip 0 chan 1 s0



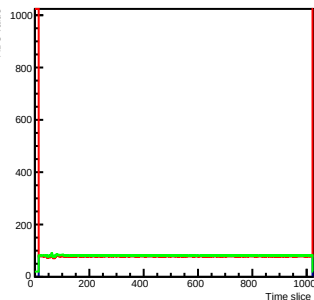
Run 0 Time mcm 0 chip 0 chan 2 s0



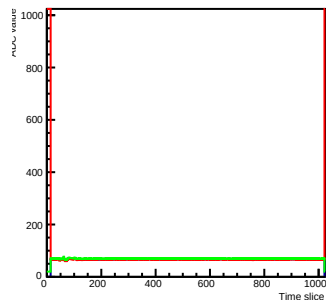
Run 0 Time mcm 0 chip 0 chan 3 s0



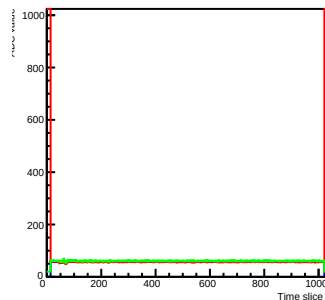
Run 0 Time mcm 0 chip 0 chan 4 s0



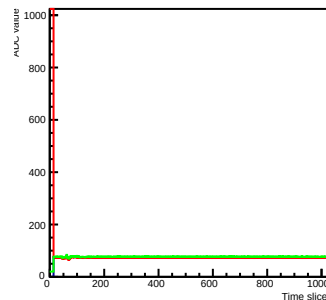
Run 0 Time mcm 0 chip 0 chan 5 s0



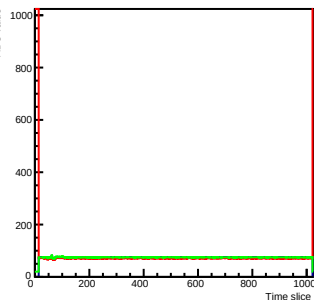
Run 0 Time mcm 0 chip 0 chan 6 s0



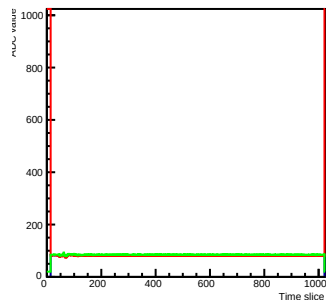
Run 0 Time mcm 0 chip 0 chan 7 s0



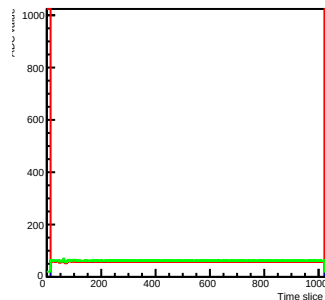
Run 0 Time mcm 0 chip 0 chan 8 s0



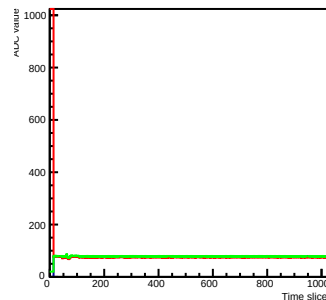
Run 0 Time mcm 0 chip 0 chan 9 s0



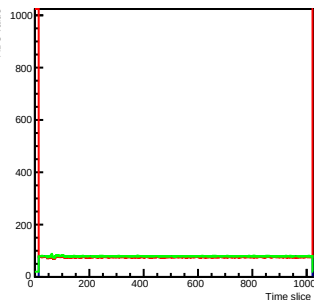
Run 0 Time mcm 0 chip 0 chan 10 s0



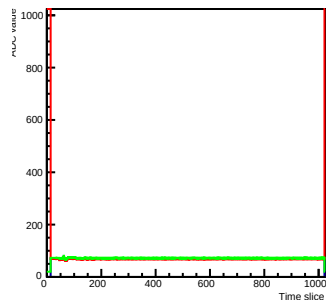
Run 0 Time mcm 0 chip 0 chan 11 s0



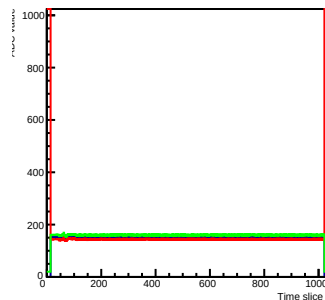
Run 0 Time mcm 0 chip 0 chan 12 s0



Run 0 Time mcm 0 chip 0 chan 13 s0



Run 0 Time mcm 0 chip 0 chan 14 s0



Run 0 Time mcm 0 chip 0 chan 15 s0

