

CHIP 63

20180806

Runs taken with SRU.

2 channels per run with 1000 samples.

Runs added together to make the plots.

500 events per run.

NOTE --preamp 1 --gain 0 --shaper 0 some ch have high rms

NOTE --preamp 1 --gain 3 --shaper 0 GAIN HIGH signal 3.0V -> 1023 in ADC

PULSER CHIP 63 DECAY = 09

--preamp 1 --gain 3 --shaper 0

3.0V

Plot 1: pedestals with nominal vref 0.25,0.75,1.25

Plot 1: gain 0 shaper 0 decay=0.5V

Plot 2-8: pedestals with vref = 0.25,0.80,1.35

(should have been 0.2,0.75,1.30)

Plot 2: gain 0 shaper 0

Plot 3: gain 1 shaper 0

Plot 4: gain 2 shaper 0

Plot 5: gain 3 shaper 0

Plot 6: gain 0 shaper 0 preampmode

Plot 7: gain 1 shaper 0 preampmode

Plot 8: gain 2 shaper 0 preampmode

Plot 9: gain 3 shaper 0 preampmode

Plot 10-15: study of effect of decay setting and pulse shape

pulser and with vref = 0.25,0.80,1.35

Plot 10: Max pulse height, gain 3 shaper 0 preampmode decay=0.1V

Plot 11: Max pulse height, gain 3 shaper 0 preampmode decay=0.5V

Plot 12: Max pulse height, gain 3 shaper 0 preampmode decay=0.9V

Plot 13: Pulse width: gain 3 shaper 0 preampmode decay=0.1V

Plot 14: Pulse width: gain 3 shaper 0 preampmode decay=0.5V

Plot 15: Pulse width: gain 3 shaper 0 preampmode decay=0.9V

Plots for study of effect of shaper, should be shorter pulse length for shorter shaper time.

Plot 16:

Max pulse height for shaper=0, gain=0, decay=0.5

Plot 17:

Max pulse height for shaper=1, gain=0, decay=0.5

Plot 18:

Max pulse height for shaper=3, gain=0, decay=0.5

Plot 19:

Max pulse height for shaper=7, gain=0, decay=0.5

Plot 20:

pulse length for shaper=0, gain=0, decay=0.5

Plot 21:

pulse length for shaper=1, gain=0, decay=0.5

Plot 22:

pulse length for shaper=3, gain=0, decay=0.5

Plot 23:

pulse length for shaper=7, gain=0, decay=0.5

Page 24: Study that clustering works in zerosuppression

Max pulse height for clusters with $ph > 100$, when zerosuppression

Plot 25-26: Study that clustering works in zerosuppression

The length of each cluster when zerosuppression, calculated and cluster length.

Plot 27-30: Pulse height for different gains

Plot 31: study if any bit problem

Used pedestal memory as data, the data is ramp 0,1,....

The plot show ADC value distribution for 500 events.

The plots should be flat at 500.

Plot 32: polarity = 0

Pedestals

Additional tests:

test of register for chip address = 0,4,6,7