

20180814

We have tested two batches (34 and 50 chips) of Novapack packaged chips.

Test of batch 1 on CERN testboard and LUND socketmcm.

Summary of test results:

Chip	socketmcm	cern testboard
65	ch2 high-low	ch2 high low
63	ch9 high-low	ch9 high-low
62	ch1 high-low	ch1 high-low
61	OK	OK
60	ch11 high-low	ch11 high-low
57	ch12 high low (weak)	ch1 bit error(?)
55	ch15 bit error, also ramp	ch15 bit error, also ramp
52	ch9 high-low	ch9 bit error, high-low weak
40	ch14 bit error?	Chip not working, readout errors.
38	ch2 bit error, also ramp	ch2 bit error, also ramp. Ch4 suspect.

All other chips and channels seems OK. Chip 61 was tested on both setup as a reference chip.

High-low means that the time samples in pedestals is: low, high,low,high,low, etc. i.e. every second has a high value, every second has a low value.

Software trigger was used. 20 MHz sampling. Did also try auxilliary clock on some chips. No change.

Nominal reference voltages (V):

	CERN testboard	LUND socketmcm
refp	1.365	1.25
refn	0.276	0.25
vcm	0.819	0.75
cmout	0.819	0.75

Below are summary plots. They show pedestals, time sweeps for the faulty channel and for various settings and pulsing. All to illustrate the particular problem.

Nominal setting was gain=0 (lowest), shaping = 120 ns, polarity=1.

gain3=highest gain.

Ch=channel.

Preampmode = shaper is not used. This was used to be able to get a pulse with long tail to get the full ADC scale in one event.

Ramp = pedestal memory used as data, 0-1000.

Page 3-6 CHIP 63

pedestals

pedestals ch9

time sweep pedestal ch9

time sweep pulser+gain3+preampmode ch9

Page 7-11 CHIP 62

pedestals
pedestal ch1
time sweep detail ch1
time sweep full ch1
time sweep pulser+gain3+preampmode ch1

Page 12-14 CHIP 60

pedestals
time sweep preampmode+gain1 ch11
time sweep pulser+gain3+preampmode ch11

Page 15-16 CHIP 57

pedestals
pedestals ch1

Page 17-19 CHIP 55

pedestals
time sweep preampmode+gain3+pulser ch15
time sweep ramp+auxclk ch15

Page 20-22 CHIP 52

time sweep preampmode+gain3+pulser ch8
time sweep preampmode+gain3+pulser ch9 (high pulse)
time sweep preampmode+gain3+pulser ch9 (low pulse)

CHIP 40

Readout errors, not possible to read.
Not further investigated yet.
No plot.

Page 23-26 CHIP 38

pedestal preampmode+gain3 ch2
time sweep preampmode+gain3 ch2
time sweep preampmode+gain3+pulser ch2
time sweep ramp ch2

Test of batch 2 on LUND socketmcm

None of the above problems was seen. Summary:

Chip 16: Register test OK, do not get any events.

Chip 30: short ground and iopower.

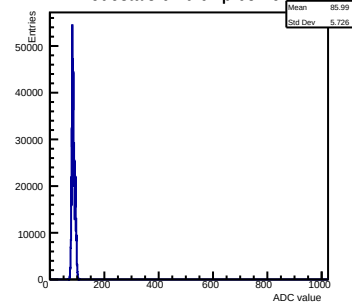
Chip 31: no connection with any pin

Chip 75: draw less current (0.36A expect 0.47A). Register test fails.

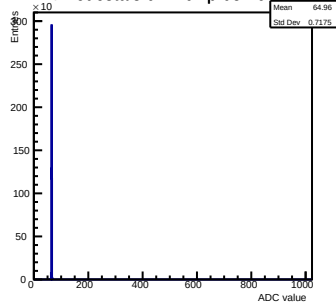
Page 27: Some chips are “nosiy” for some settings (in preampmode)

Page 28: Some channel have some bit missing (also when using pedestal memory as data), always at time slice 504 for the channel shown.

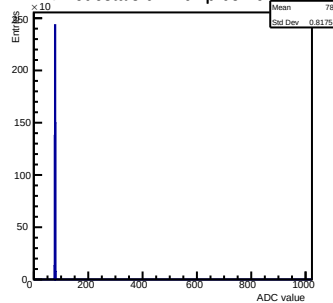
Pedestals ch 0 chip 63 nom



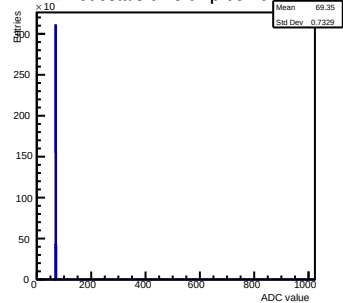
Pedestals ch 1 chip 63 nom



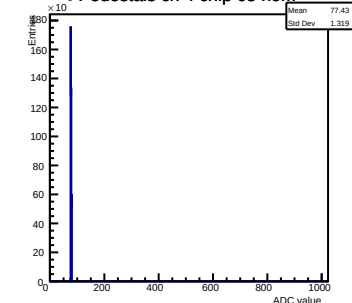
Pedestals ch 2 chip 63 nom



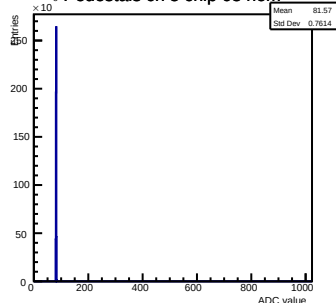
Pedestals ch 3 chip 63 nom



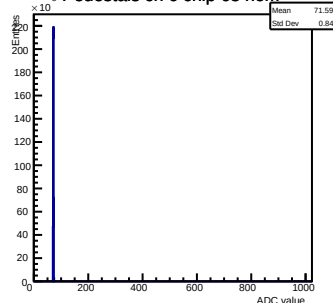
Pedestals ch 4 chip 63 nom



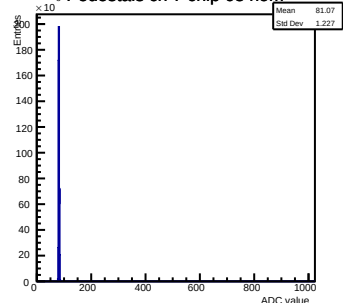
Pedestals ch 5 chip 63 nom



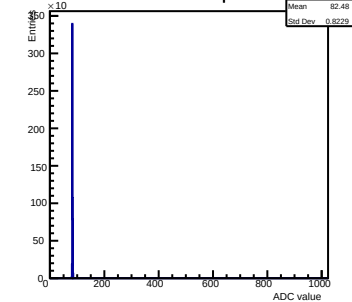
Pedestals ch 6 chip 63 nom



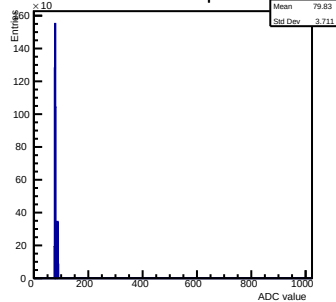
Pedestals ch 7 chip 63 nom



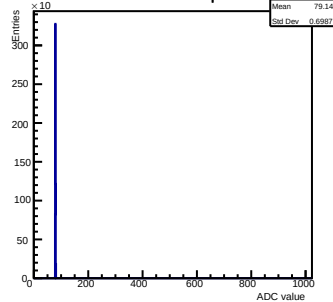
Pedestals ch 8 chip 63 nom



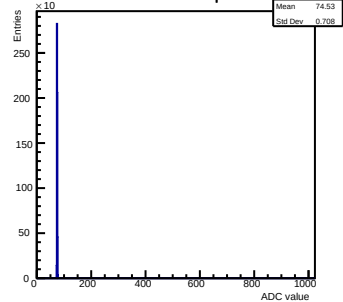
Pedestals ch 9 chip 63 nom



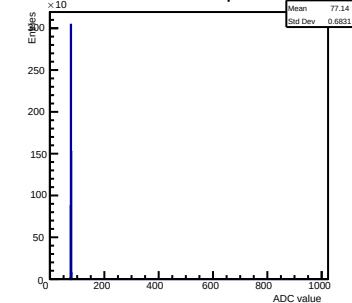
Pedestals ch 10 chip 63 nom



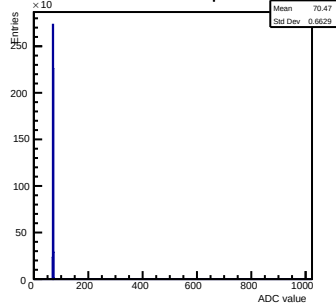
Pedestals ch 11 chip 63 nom



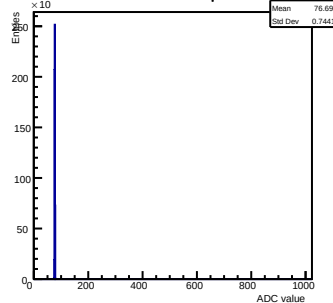
Pedestals ch 12 chip 63 nom



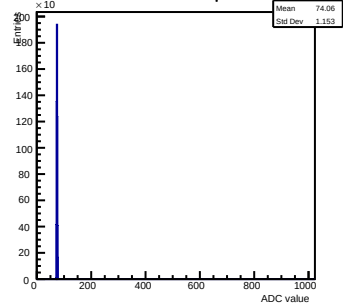
Pedestals ch 13 chip 63 nom



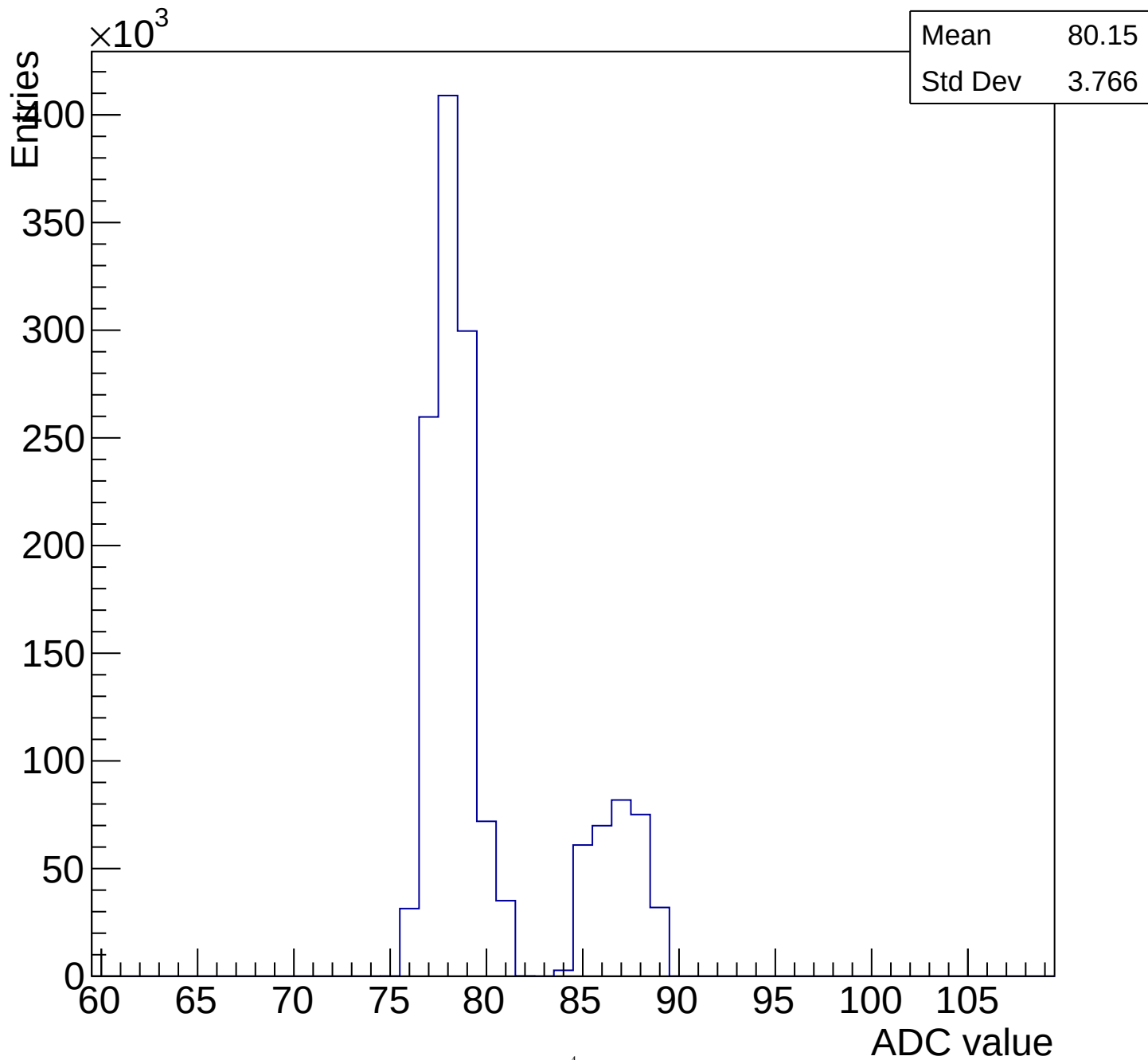
Pedestals ch 14 chip 63 nom



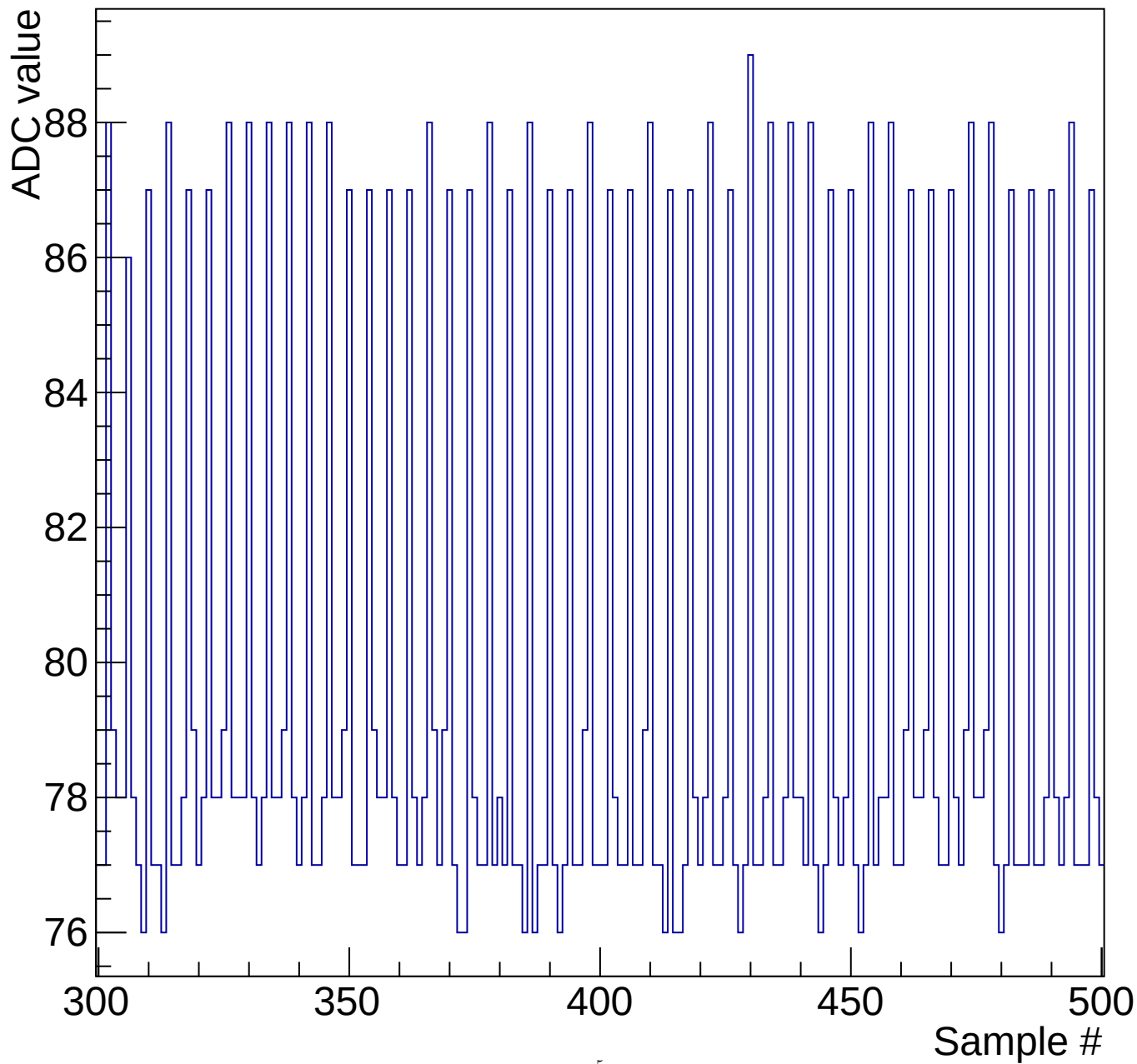
Pedestals ch 15 chip 63 nom



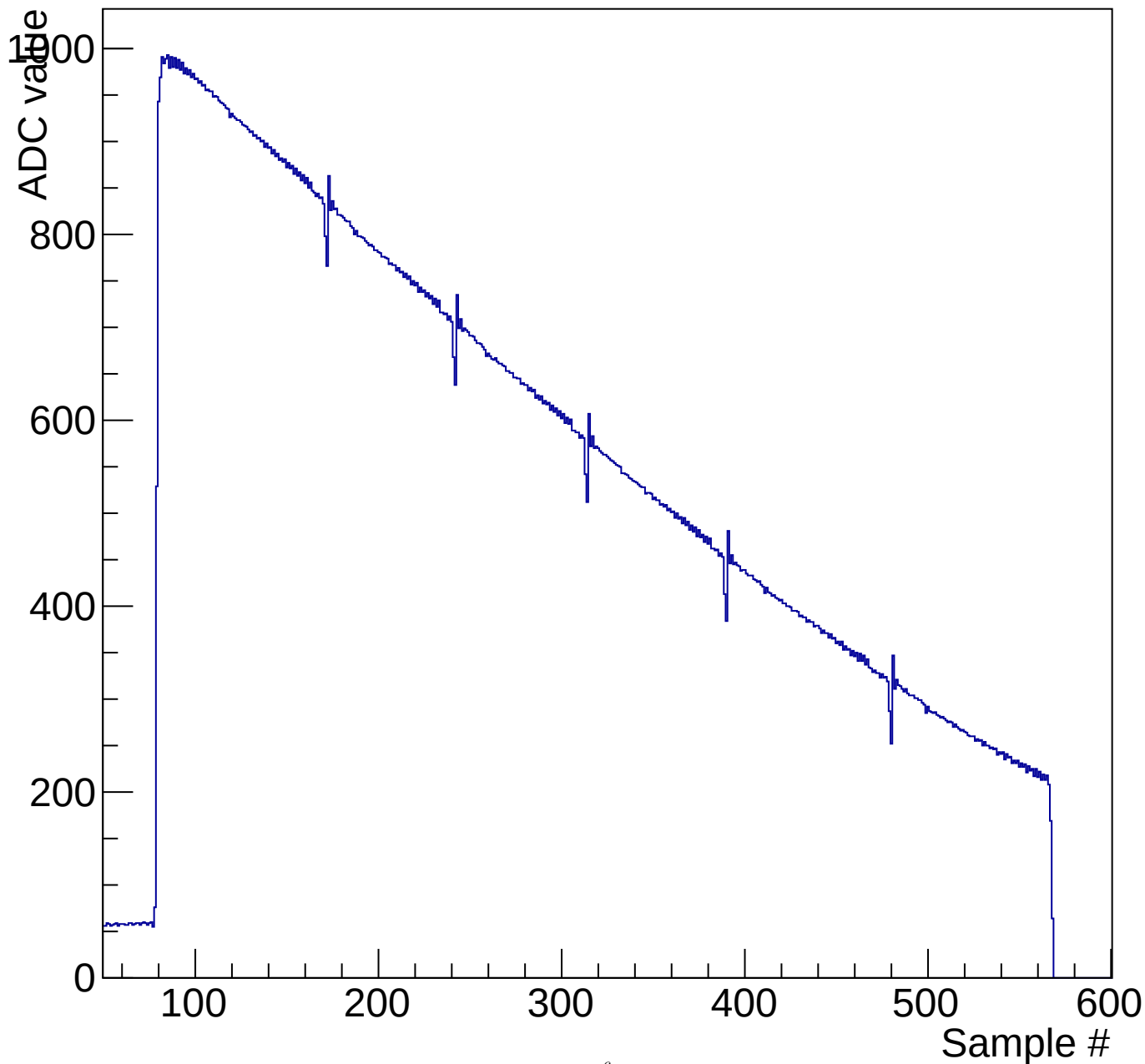
Pedestals ch 9 chip 63 run 34339 nom



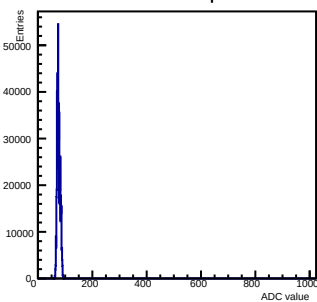
Run 34339 Event 2 Chip 63 Channel_9



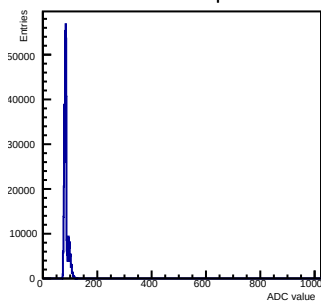
Run 34346 Event 7 Chip 63 Channel_9



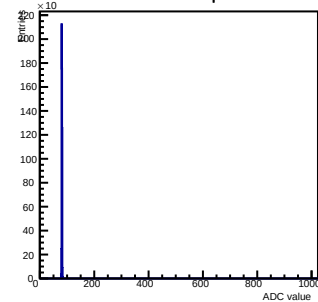
Pedestals ch 0 chip 62 nom



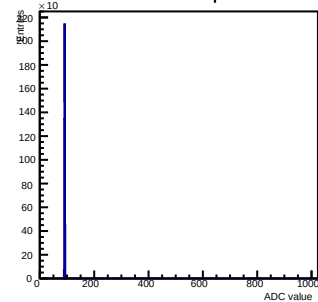
Pedestals ch 1 chip 62 nom



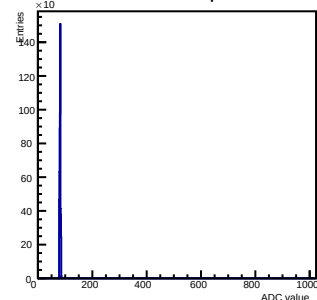
Pedestals ch 2 chip 62 nom



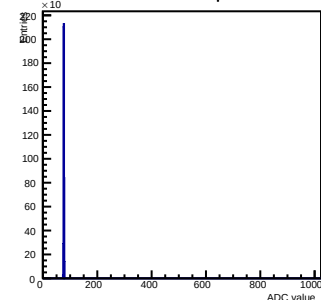
Pedestals ch 3 chip 62 nom



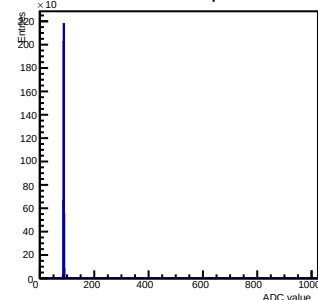
Pedestals ch 4 chip 62 nom



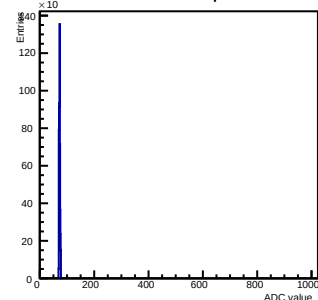
Pedestals ch 5 chip 62 nom



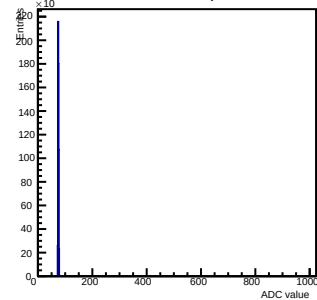
Pedestals ch 6 chip 62 nom



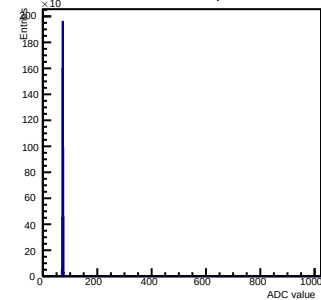
Pedestals ch 7 chip 62 nom



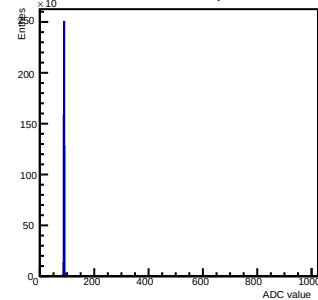
Pedestals ch 8 chip 62 nom



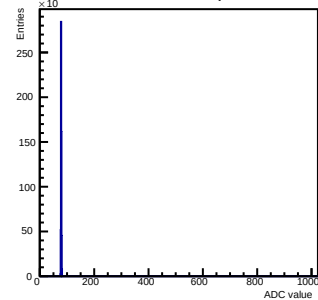
Pedestals ch 9 chip 62 nom



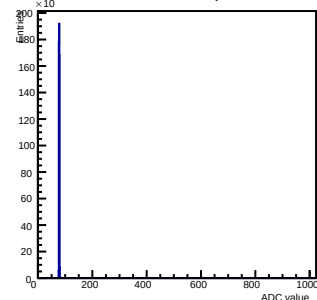
Pedestals ch 10 chip 62 nom



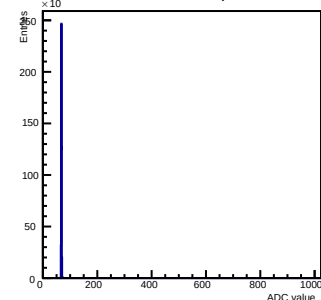
Pedestals ch 11 chip 62 nom



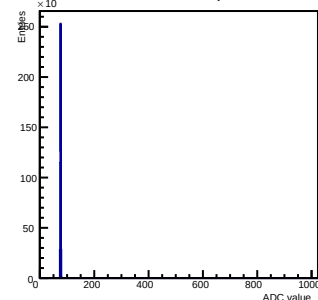
Pedestals ch 12 chip 62 nom



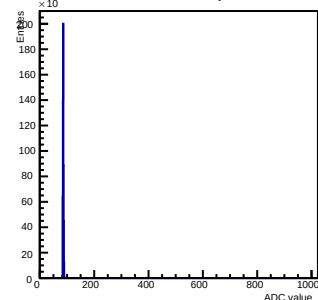
Pedestals ch 13 chip 62 nom



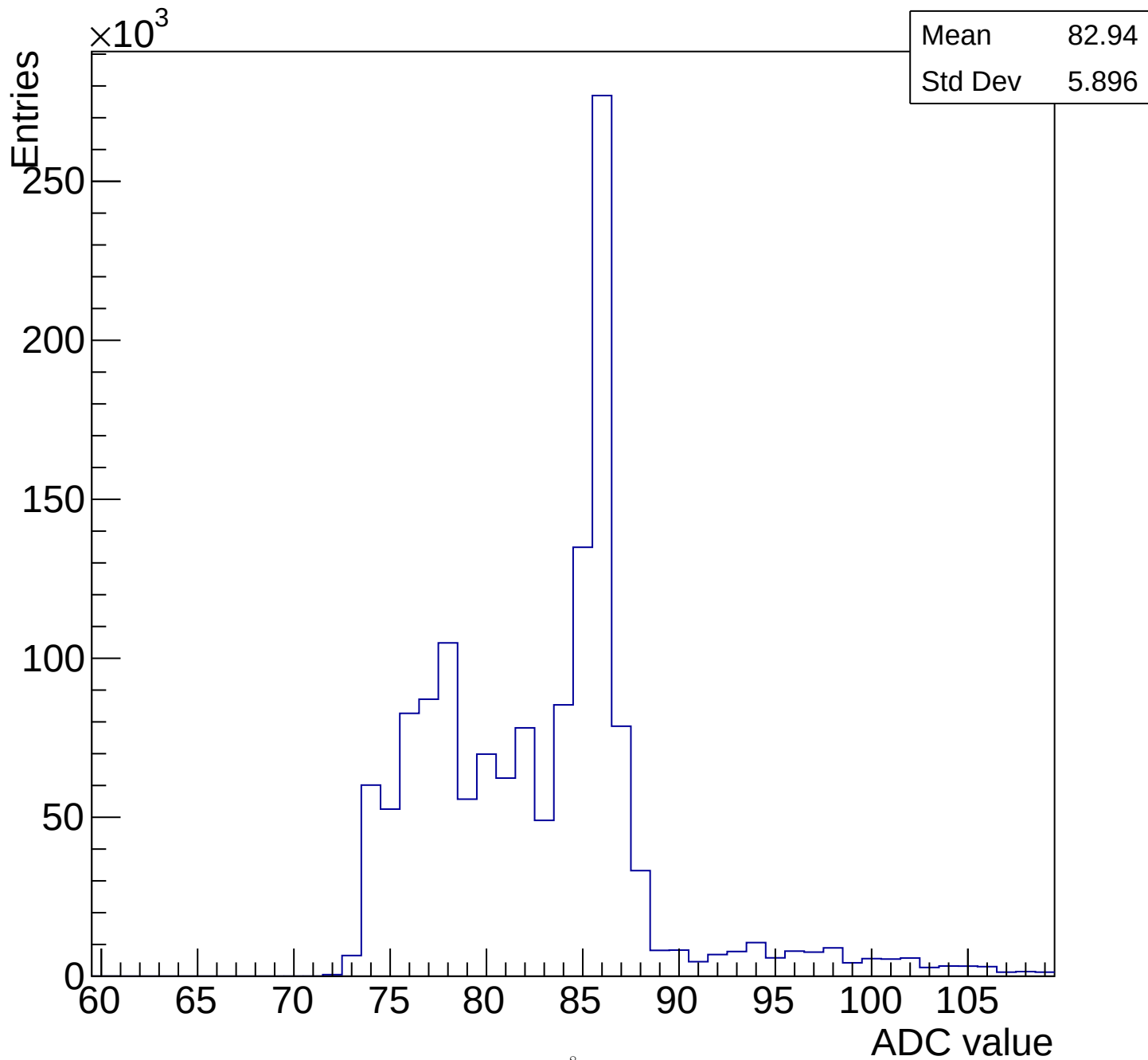
Pedestals ch 14 chip 62 nom



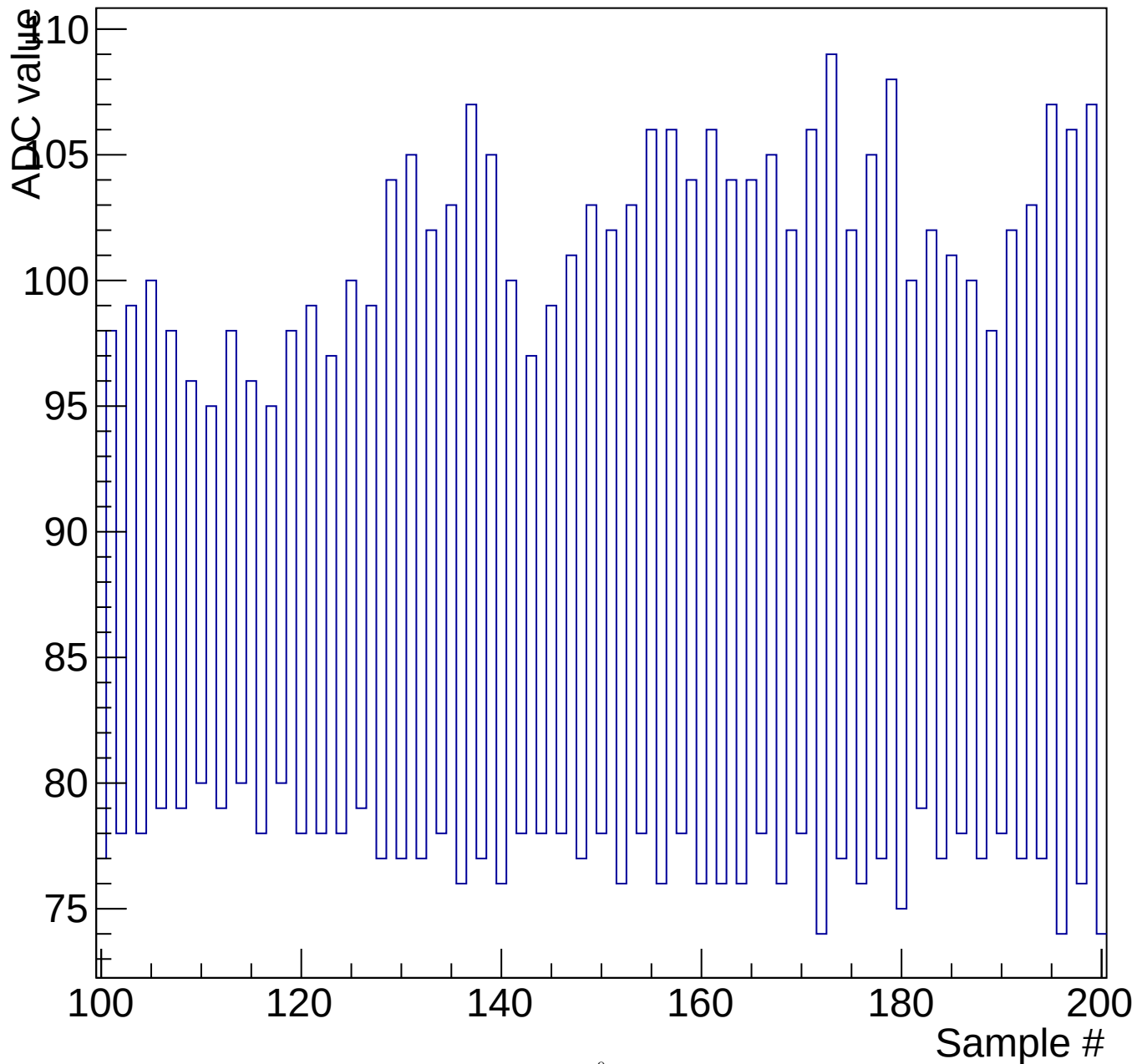
Pedestals ch 15 chip 62 nom



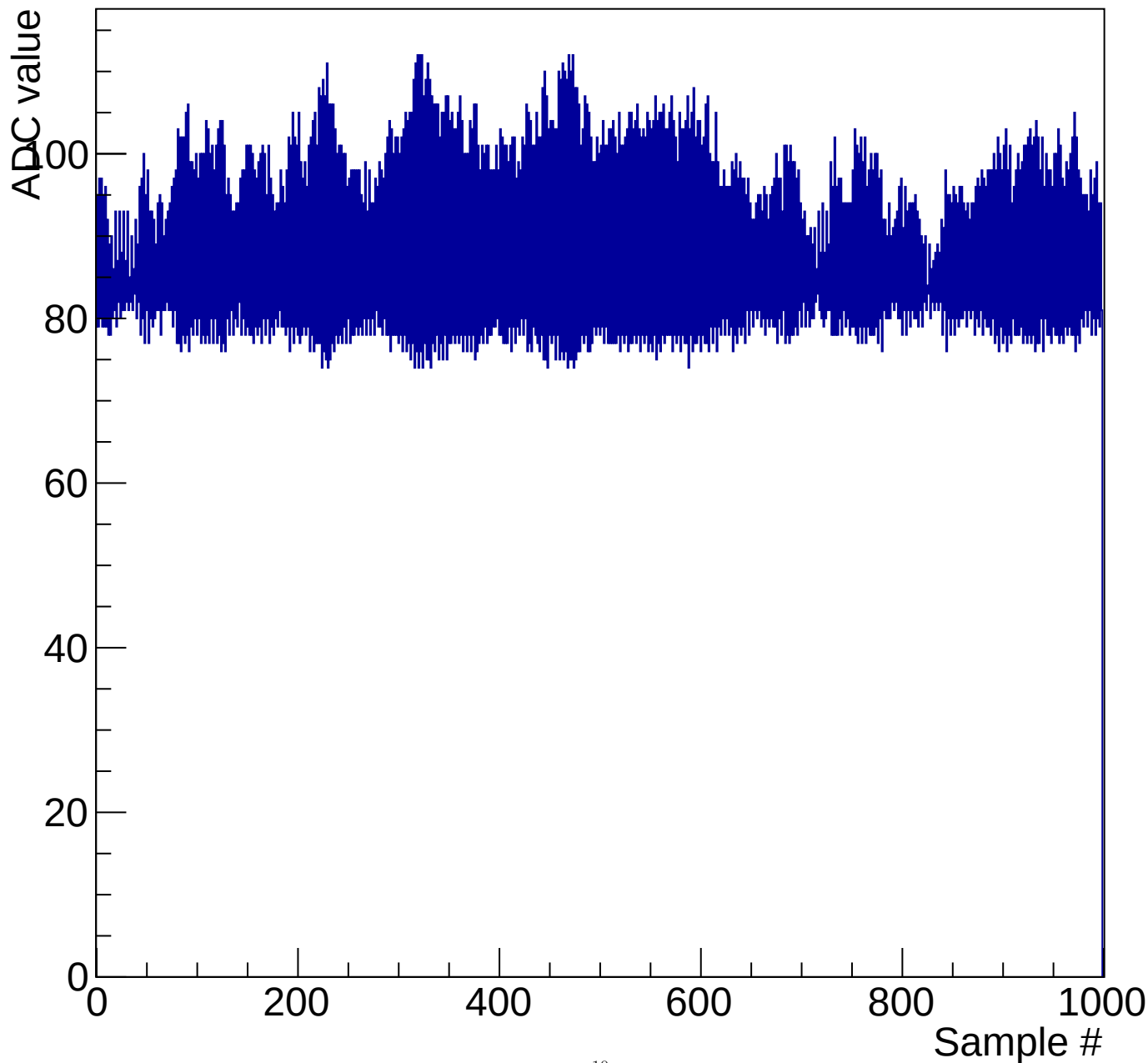
Pedestals ch 1 chip 62 run 34351 nom



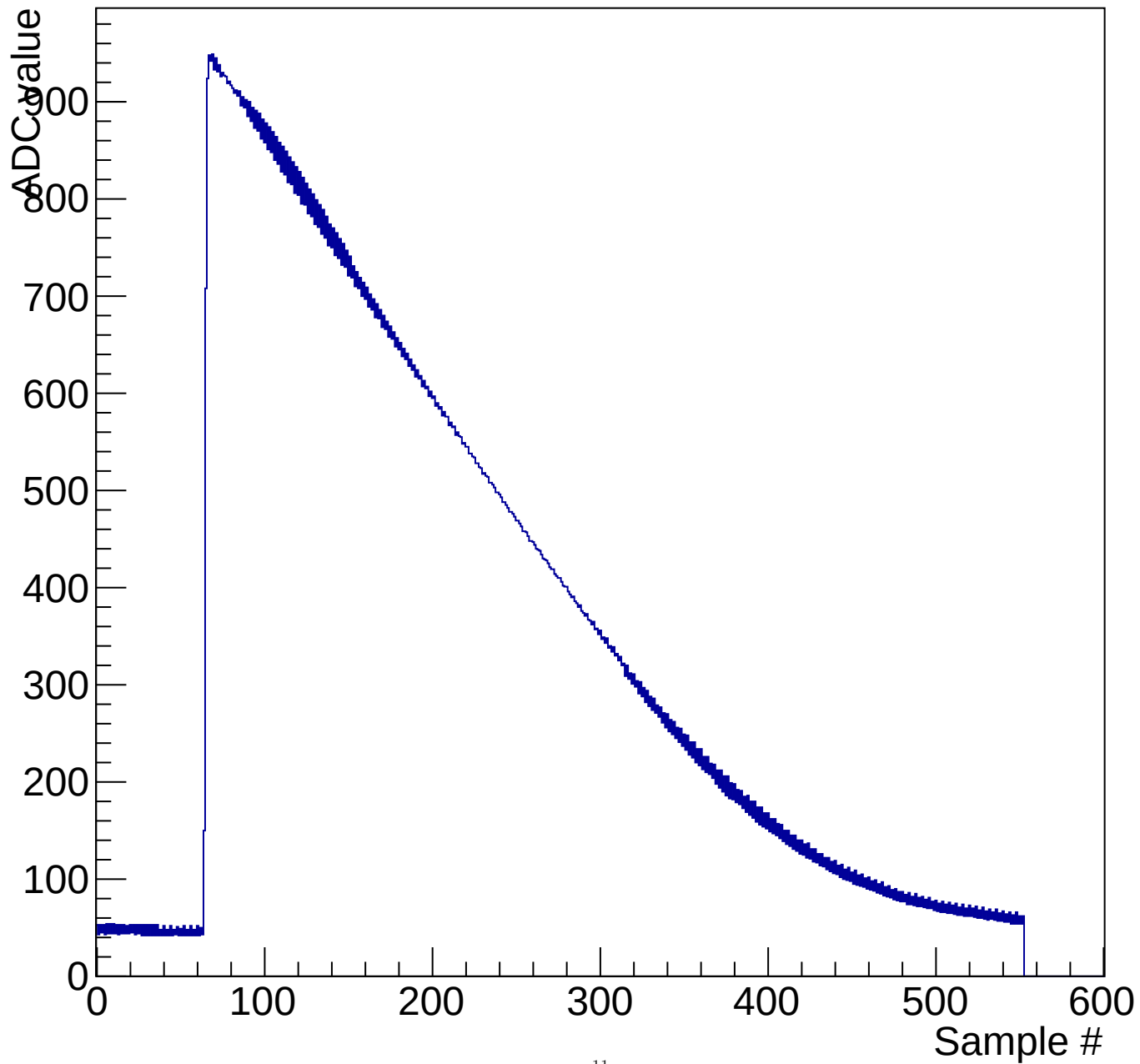
Run 34351 Event 1 Chip 62 Channel_1



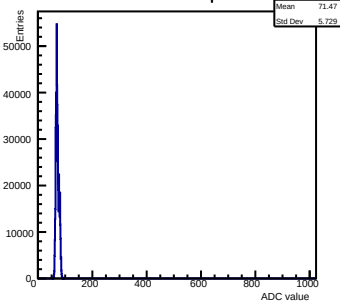
Run 34351 Event 2 Chip 62 Channel_1



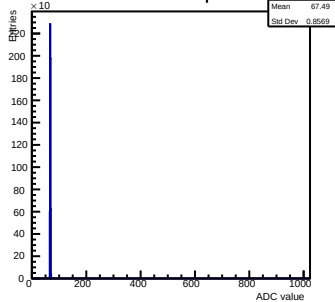
Run 34354 Event 126 Chip 62 Channel_1



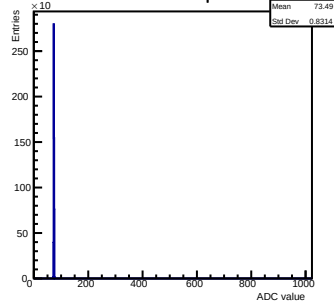
Pedestals ch 0 chip 60 nom



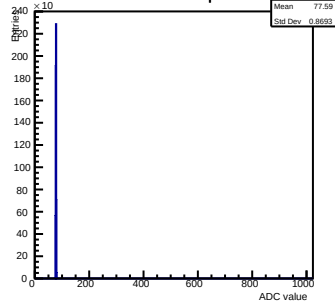
Pedestals ch 1 chip 60 nom



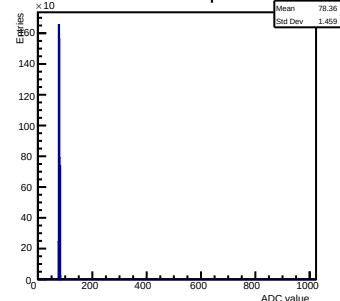
Pedestals ch 2 chip 60 nom



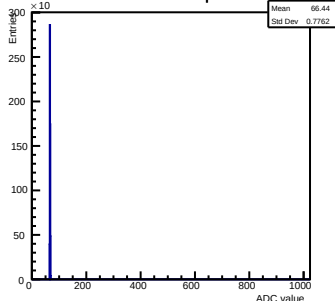
Pedestals ch 3 chip 60 nom



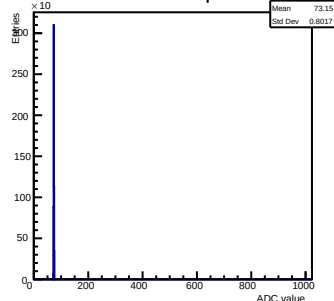
Pedestals ch 4 chip 60 nom



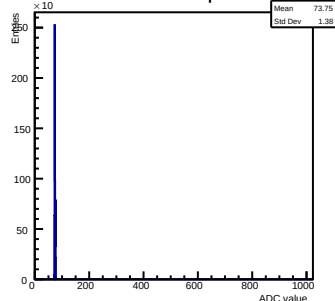
Pedestals ch 5 chip 60 nom



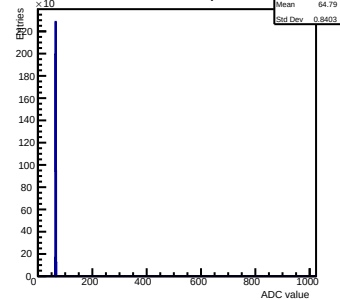
Pedestals ch 6 chip 60 nom



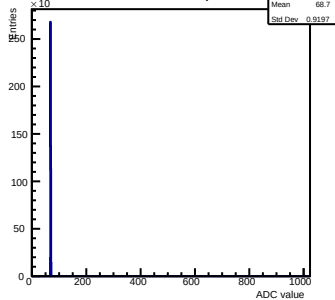
Pedestals ch 7 chip 60 nom



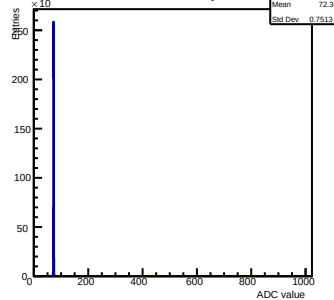
Pedestals ch 8 chip 60 nom



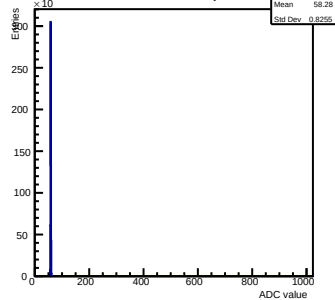
Pedestals ch 9 chip 60 nom



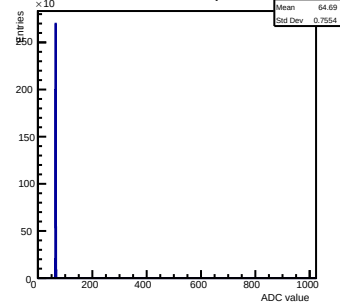
Pedestals ch 10 chip 60 nom



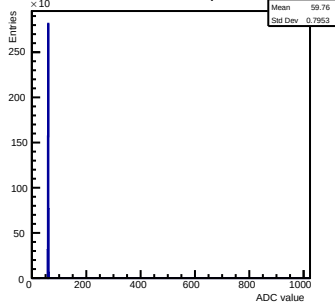
Pedestals ch 11 chip 60 nom



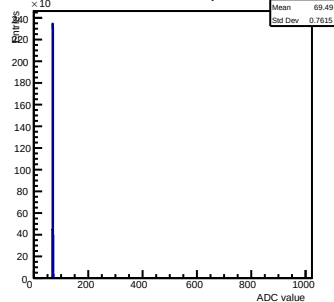
Pedestals ch 12 chip 60 nom



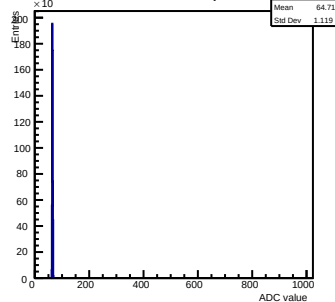
Pedestals ch 13 chip 60 nom



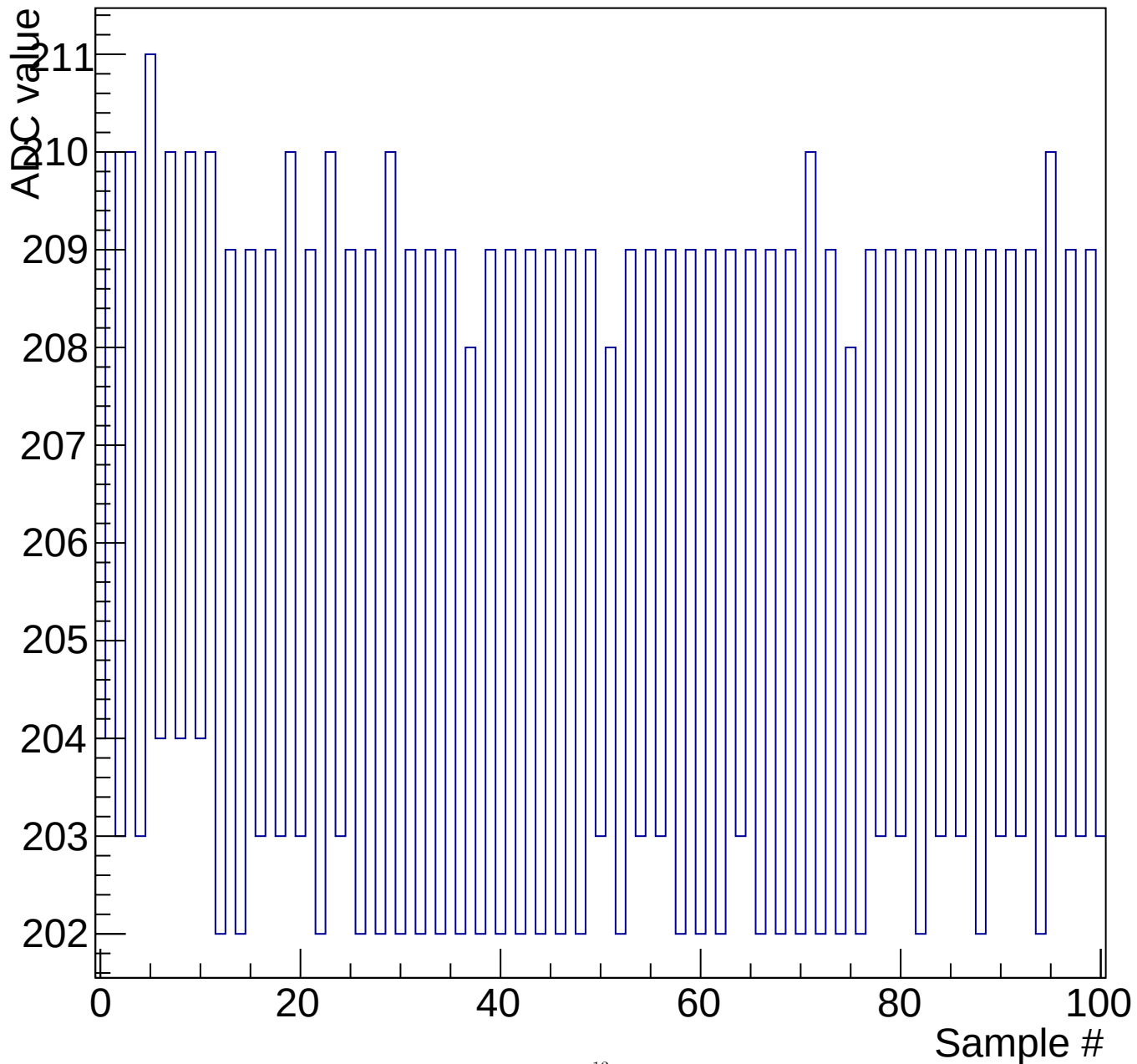
Pedestals ch 14 chip 60 nom



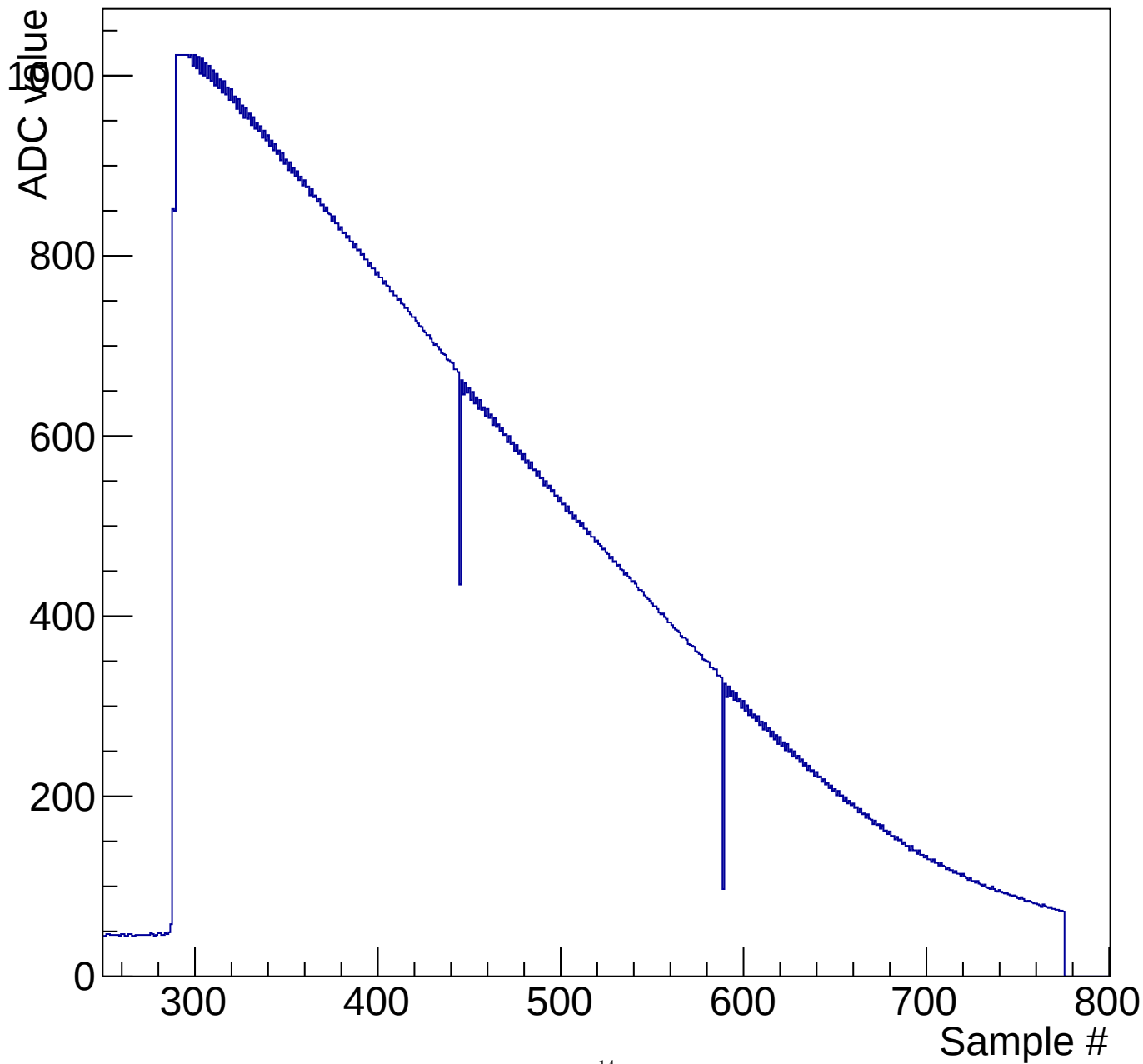
Pedestals ch 15 chip 60 nom

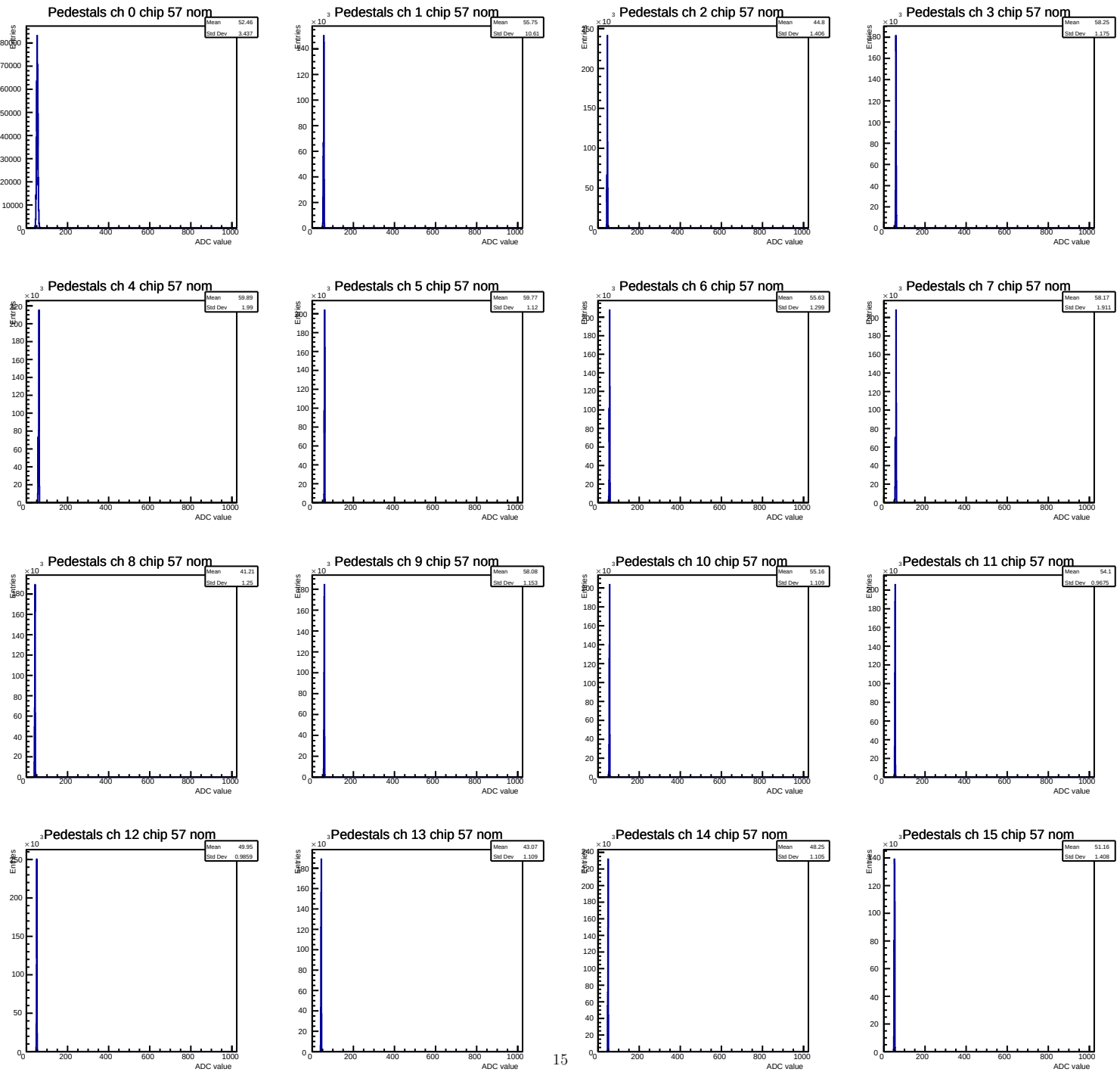


Run 34362 Event 1 Chip 60 Channel_11

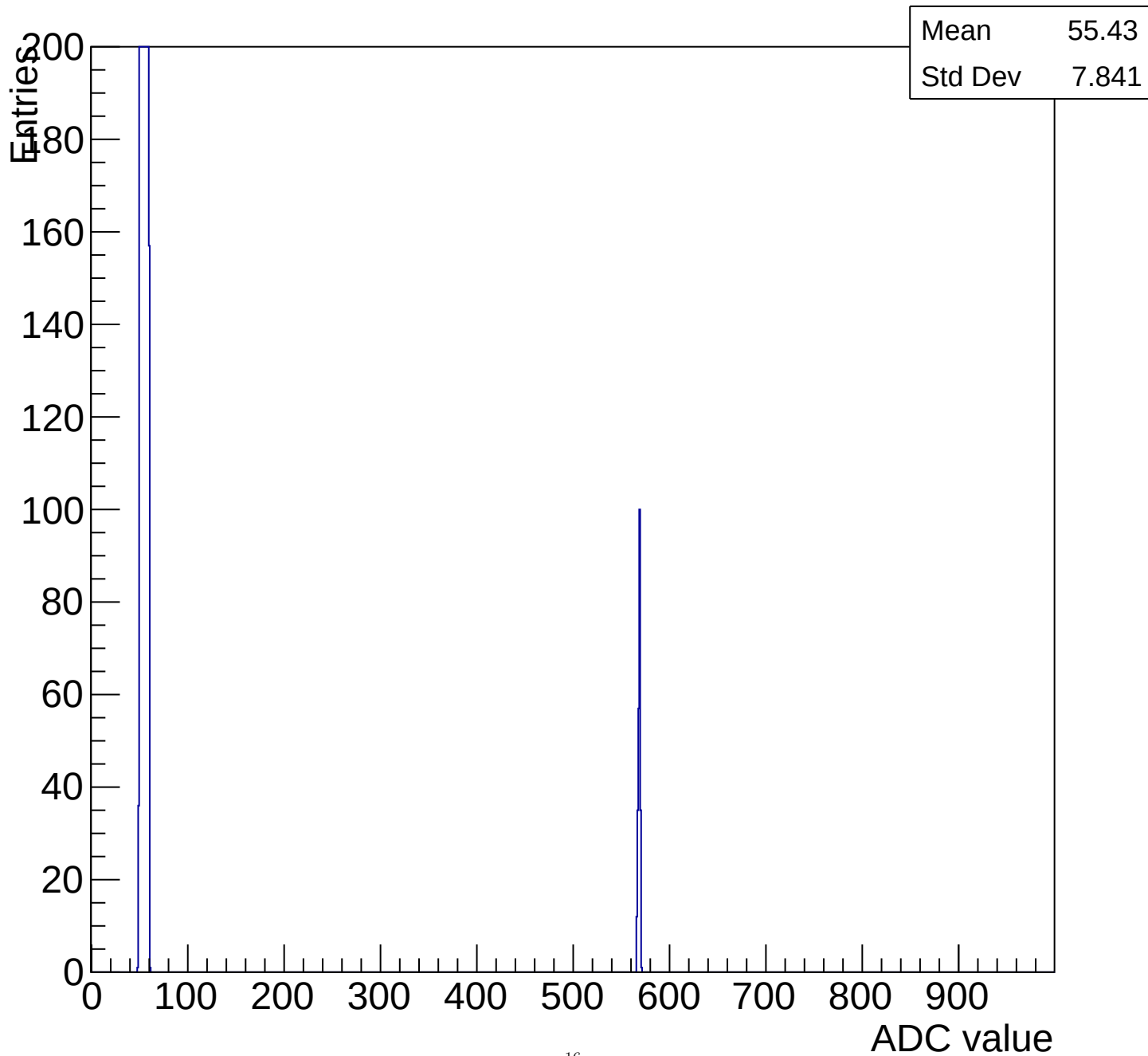


Run 34365 Event 95 Chip 60 Channel_11

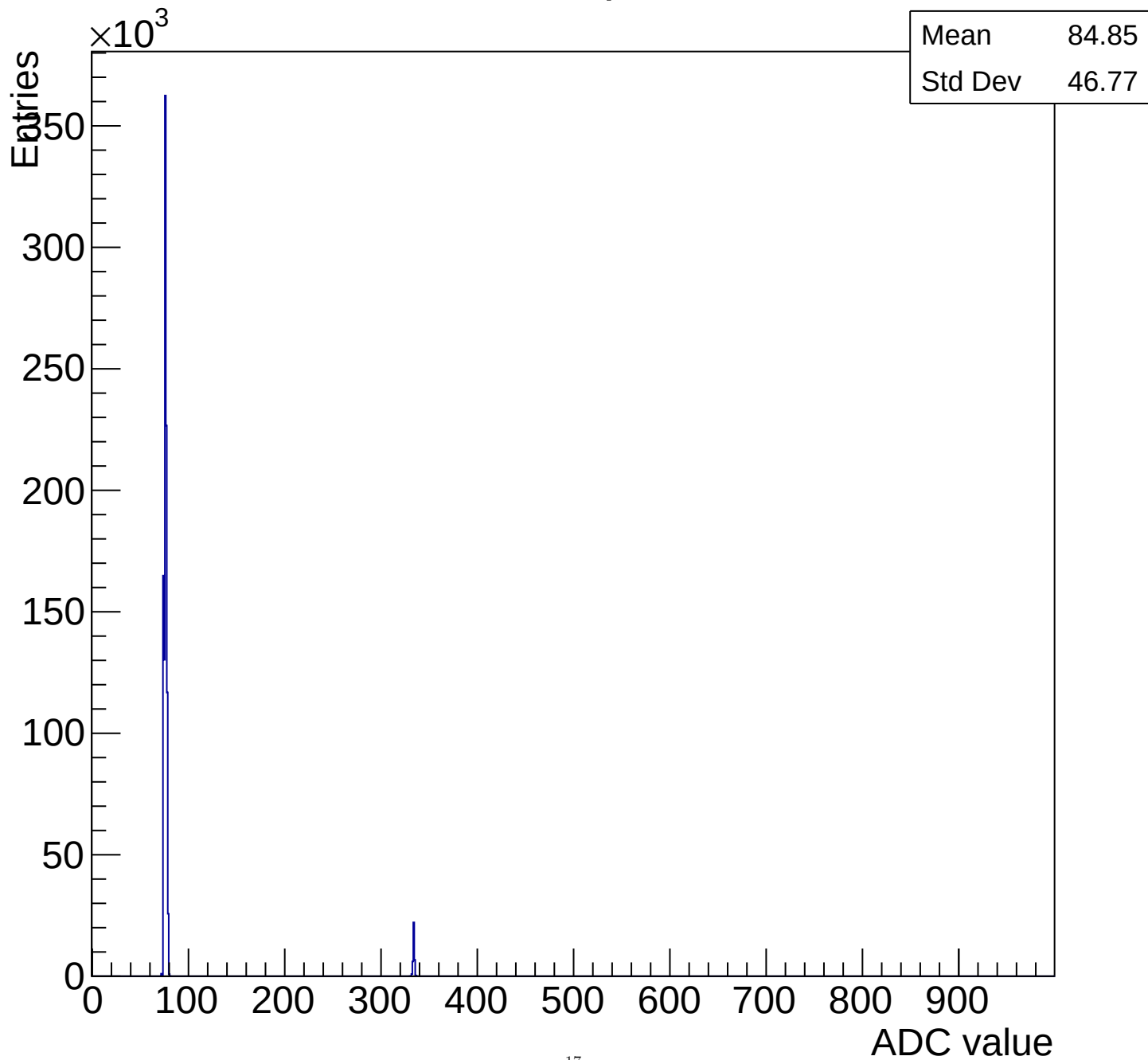




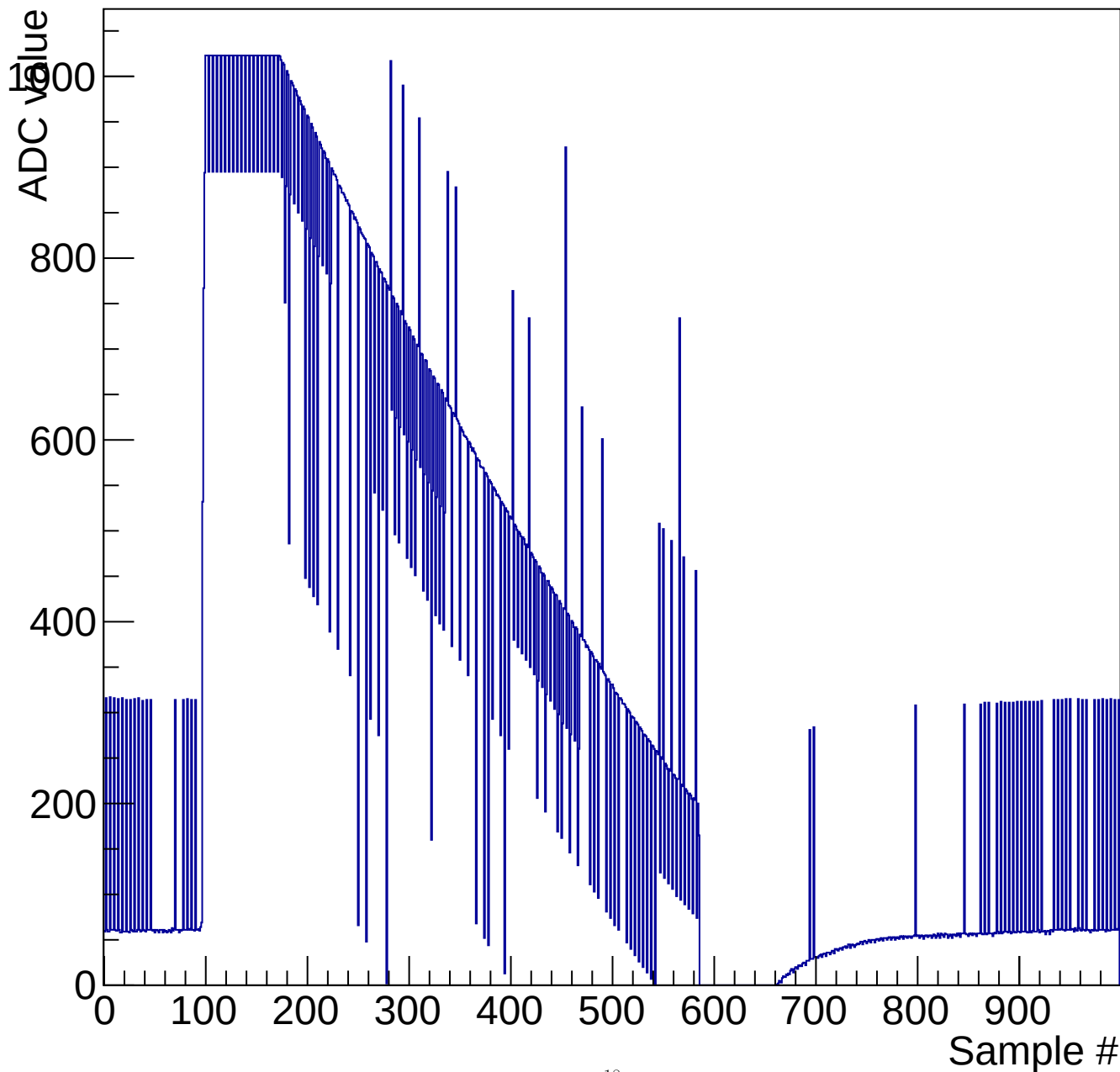
Pedestals ch 1 chip 57 run 34366 nom



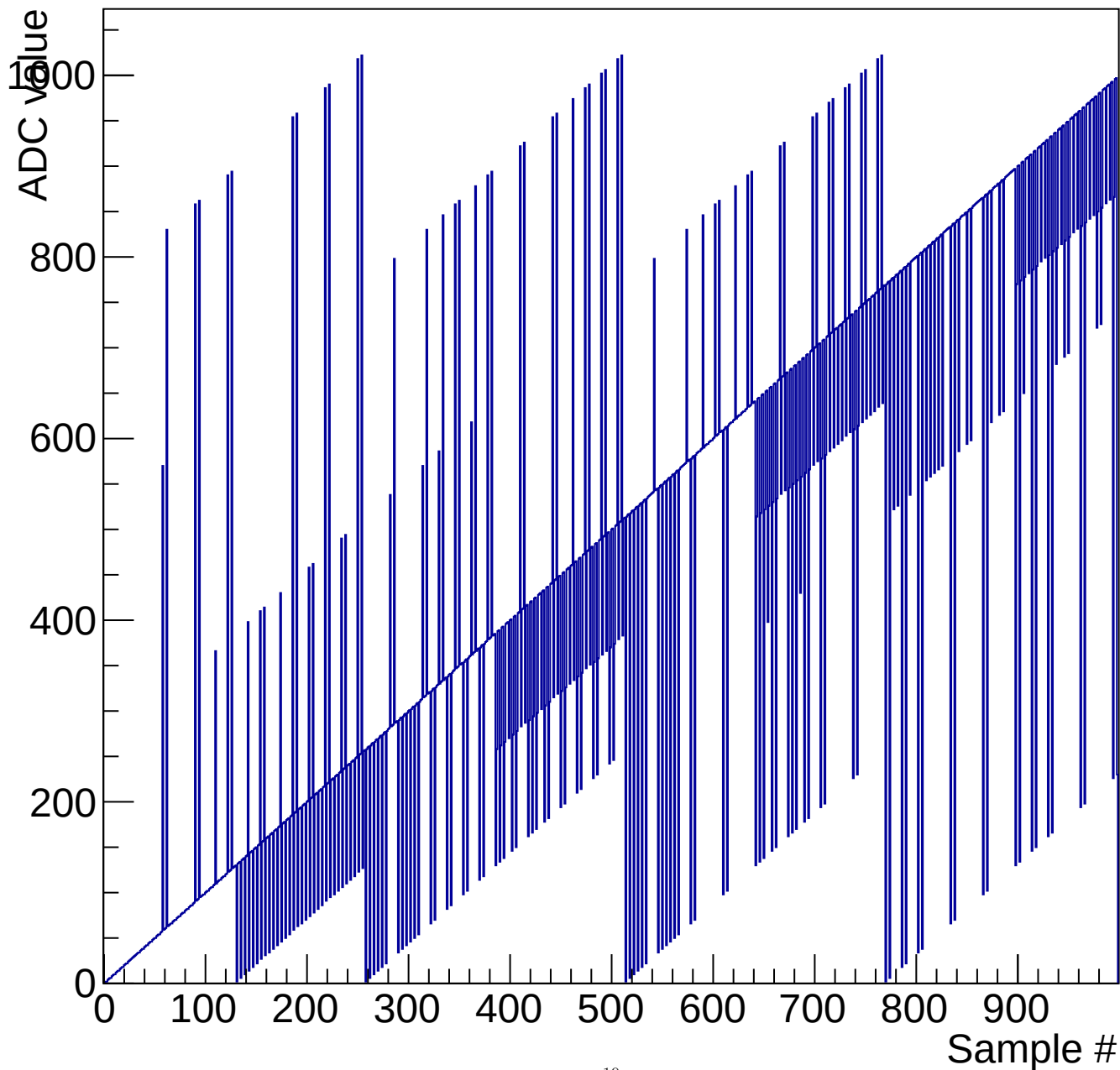
Pedestals ch 15 chip 55 run 34369 1



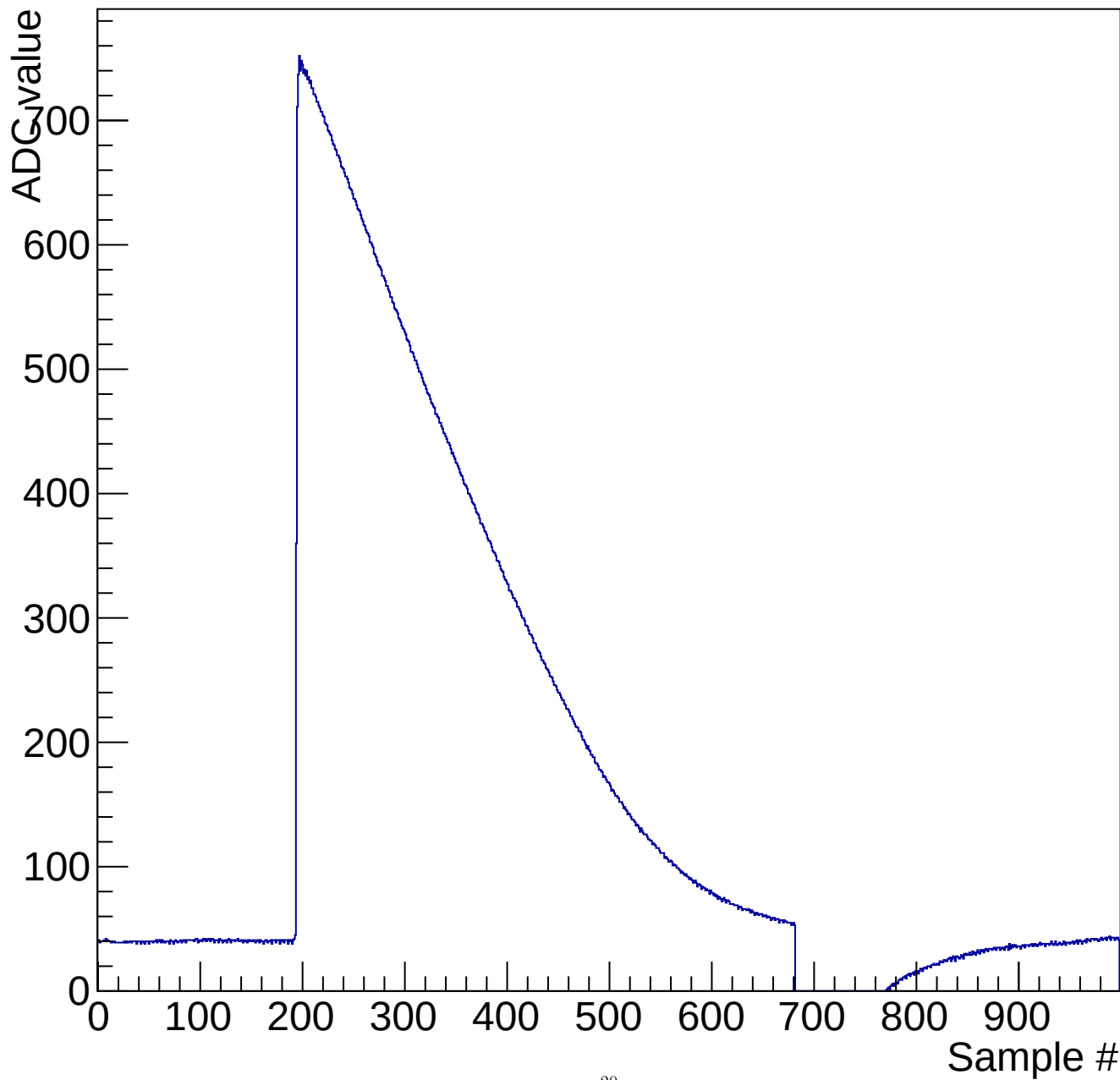
Run 34370 Event 1 Chip 55 Channel_15



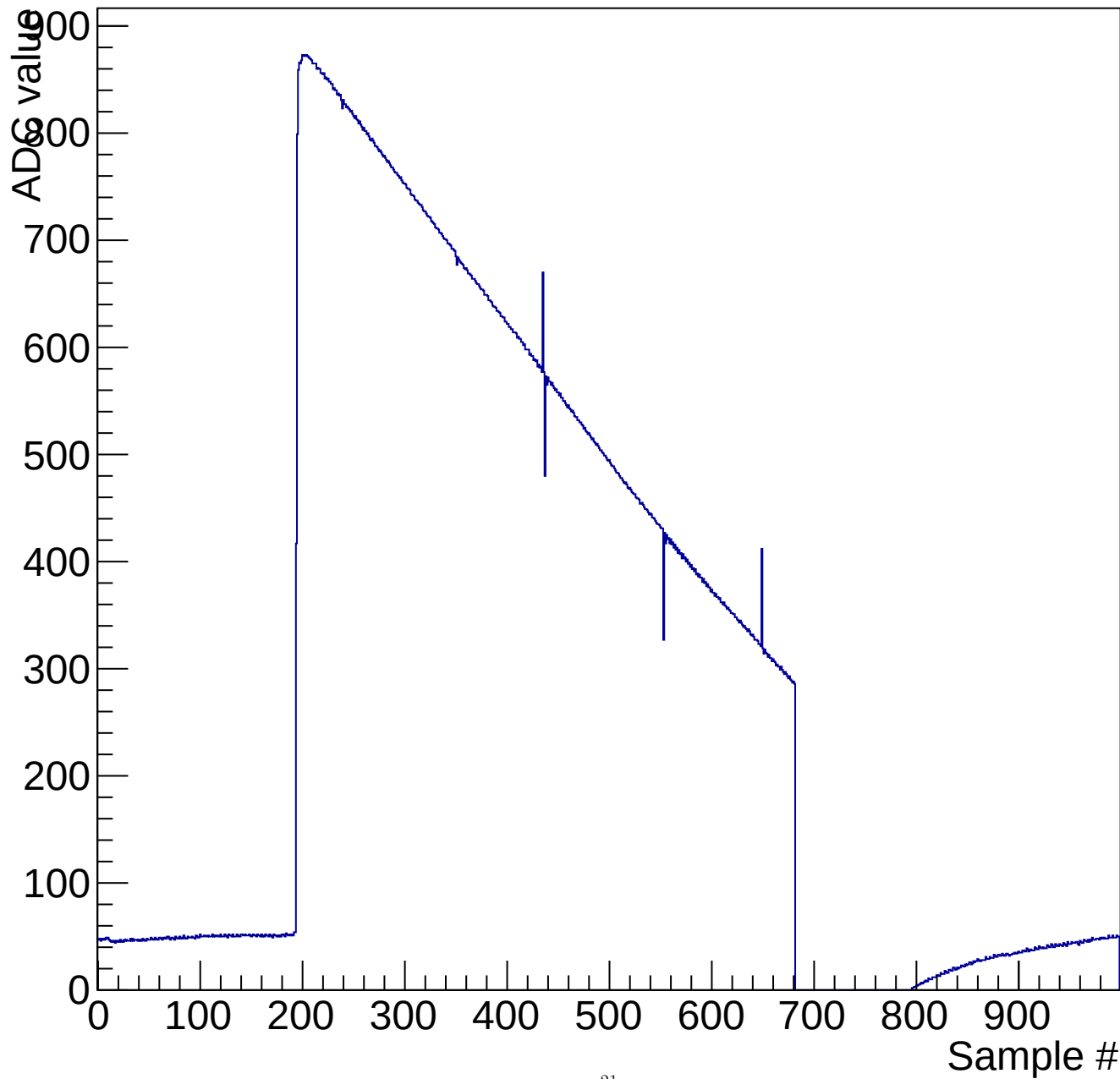
Run 34374 Event 1 Chip 55 Channel_15



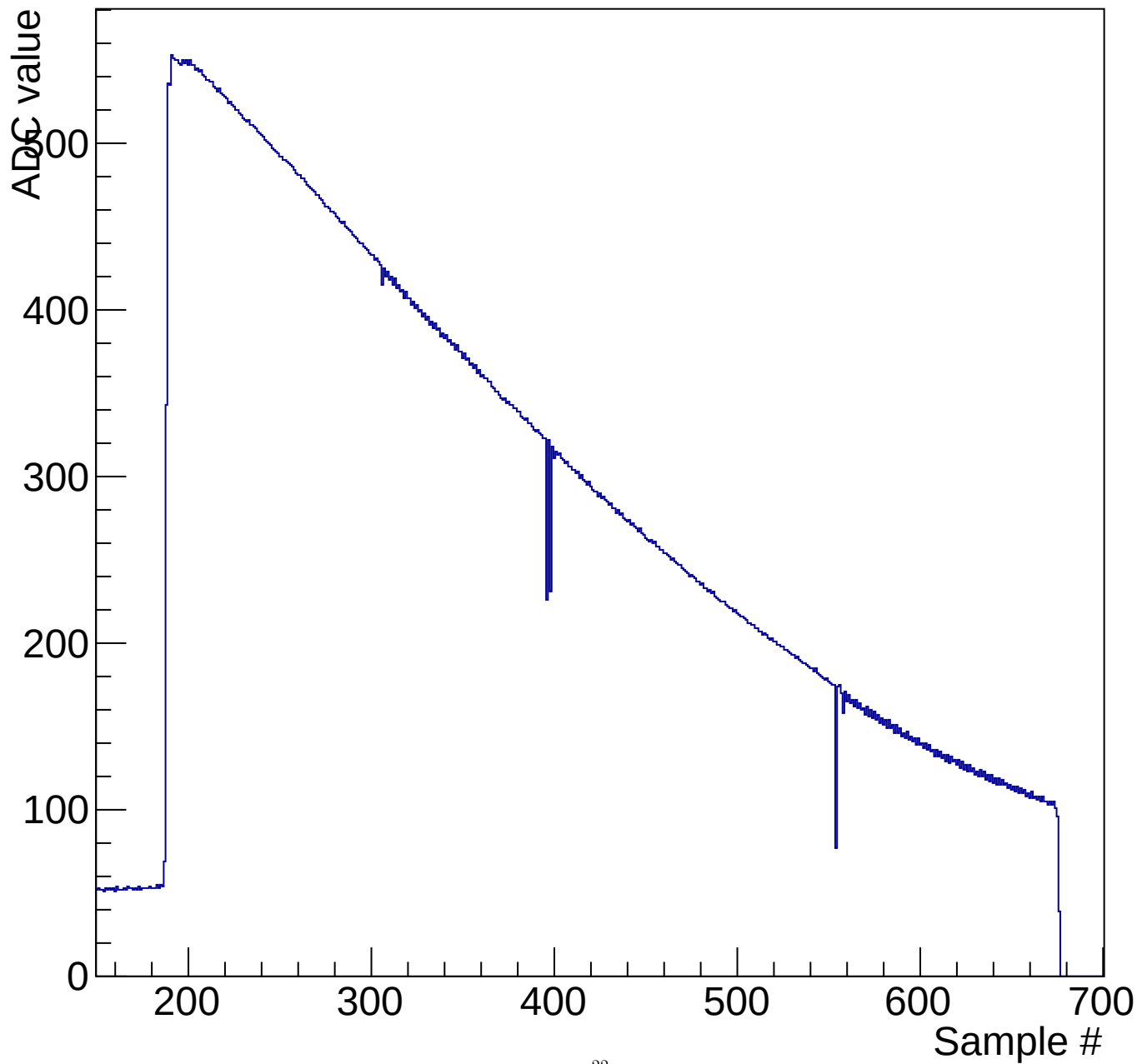
Run 34376 Event 134 Chip 52 Channel_8



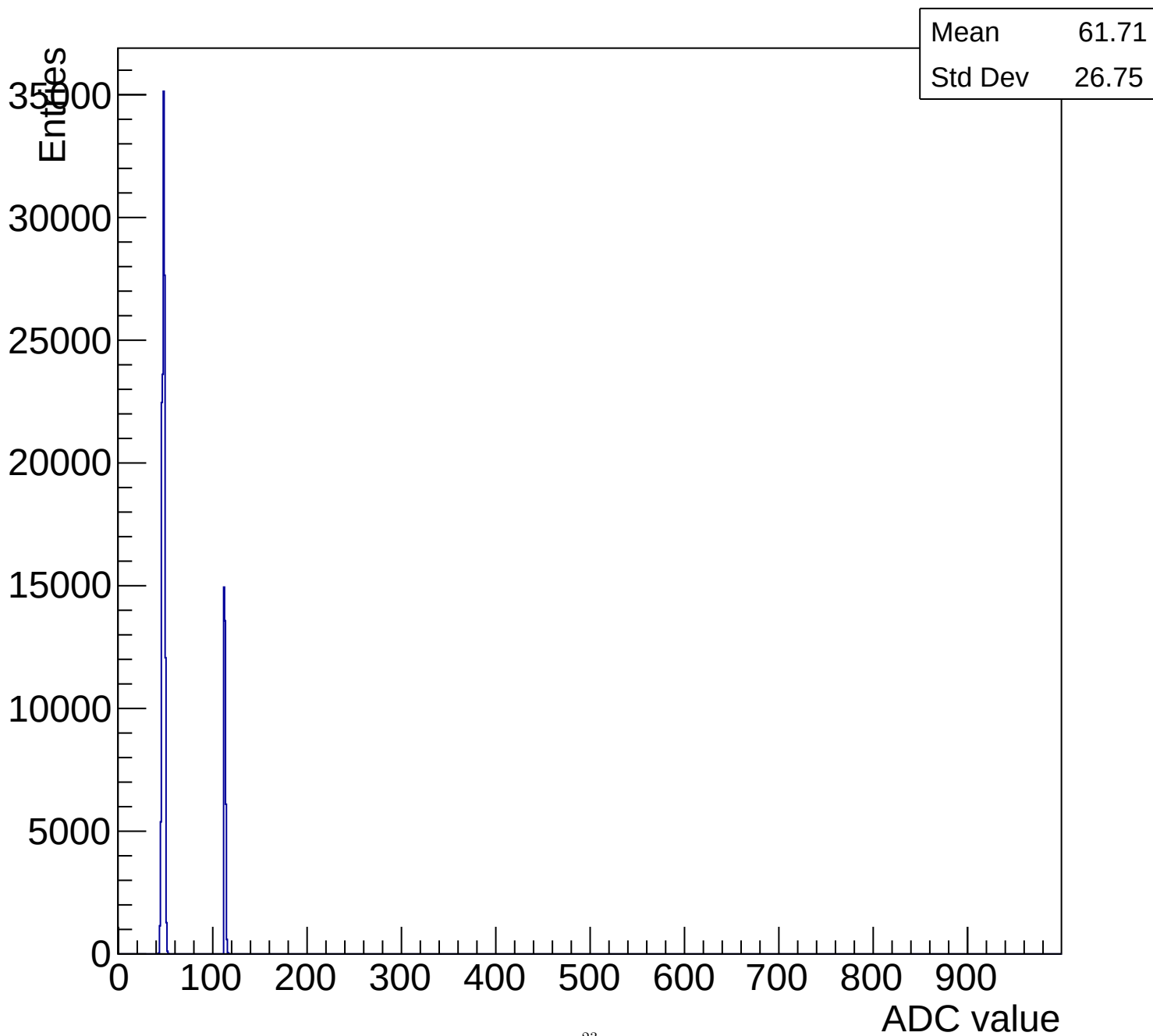
Run 34376 Event 134 Chip 52 Channel_9



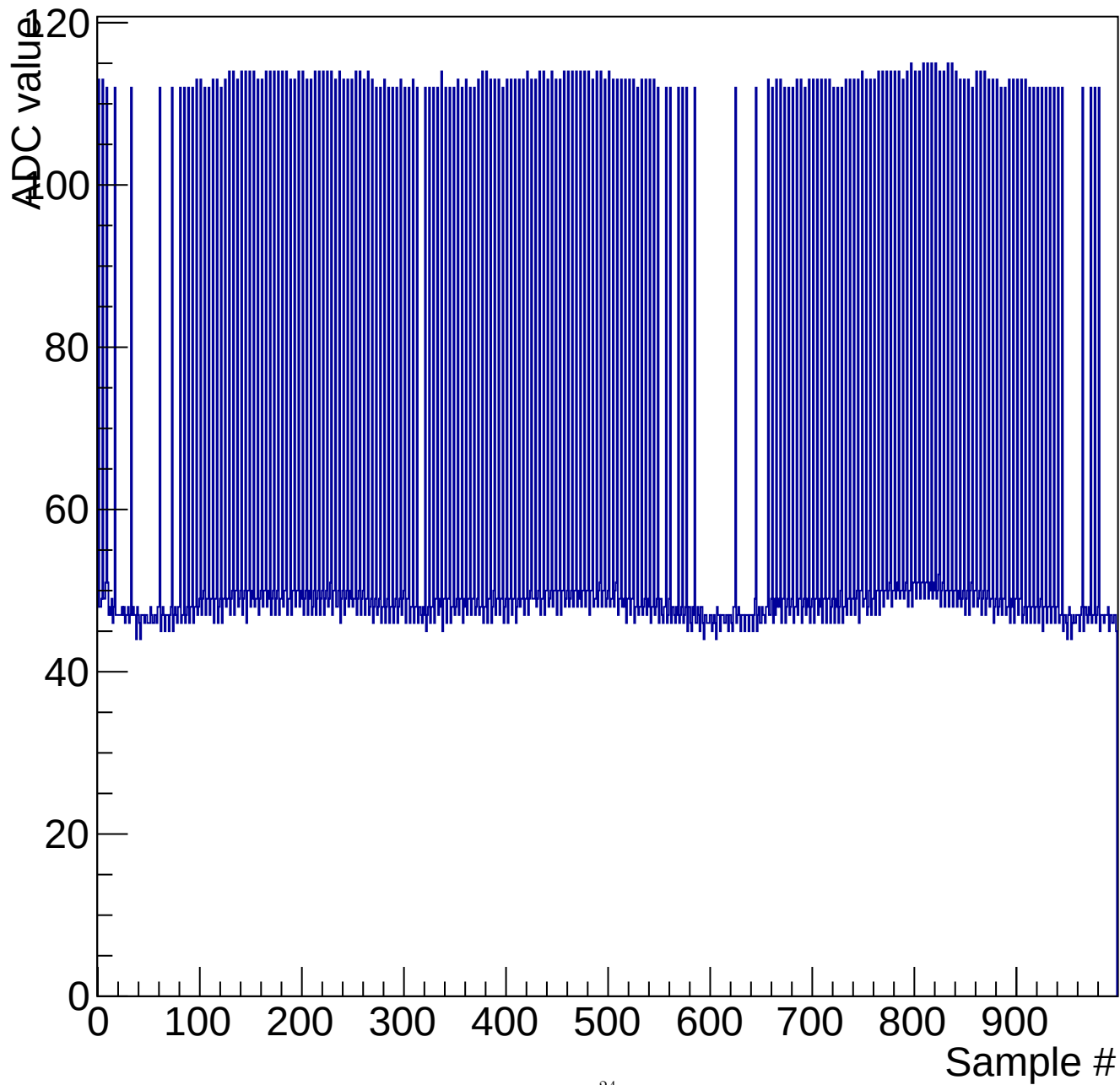
Run 34380 Event 1 Chip 52 Channel_9



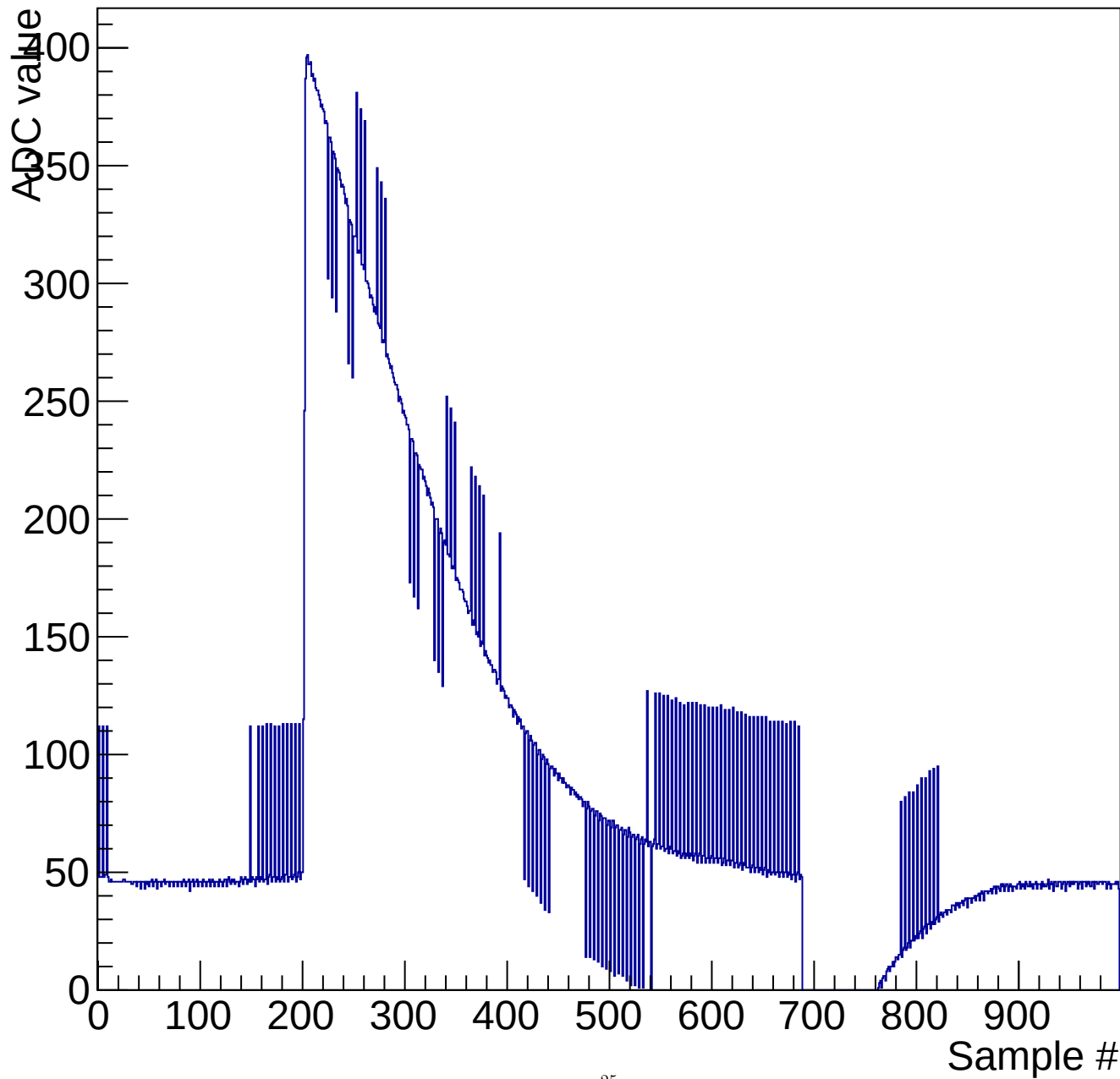
Pedestals ch 2 chip 38 run 34384 1



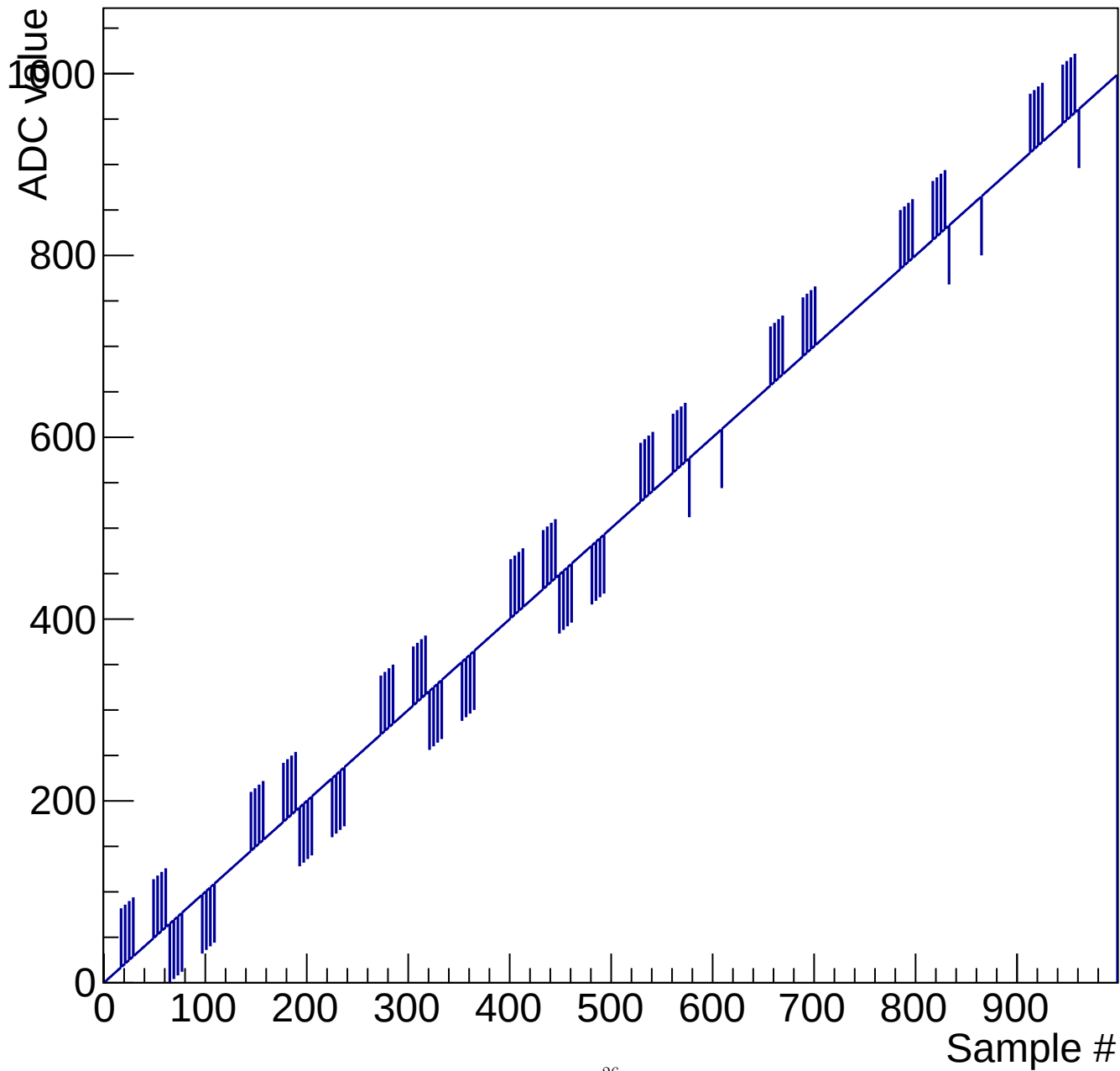
Run 34384 Event 211 Chip 38 Channel_2



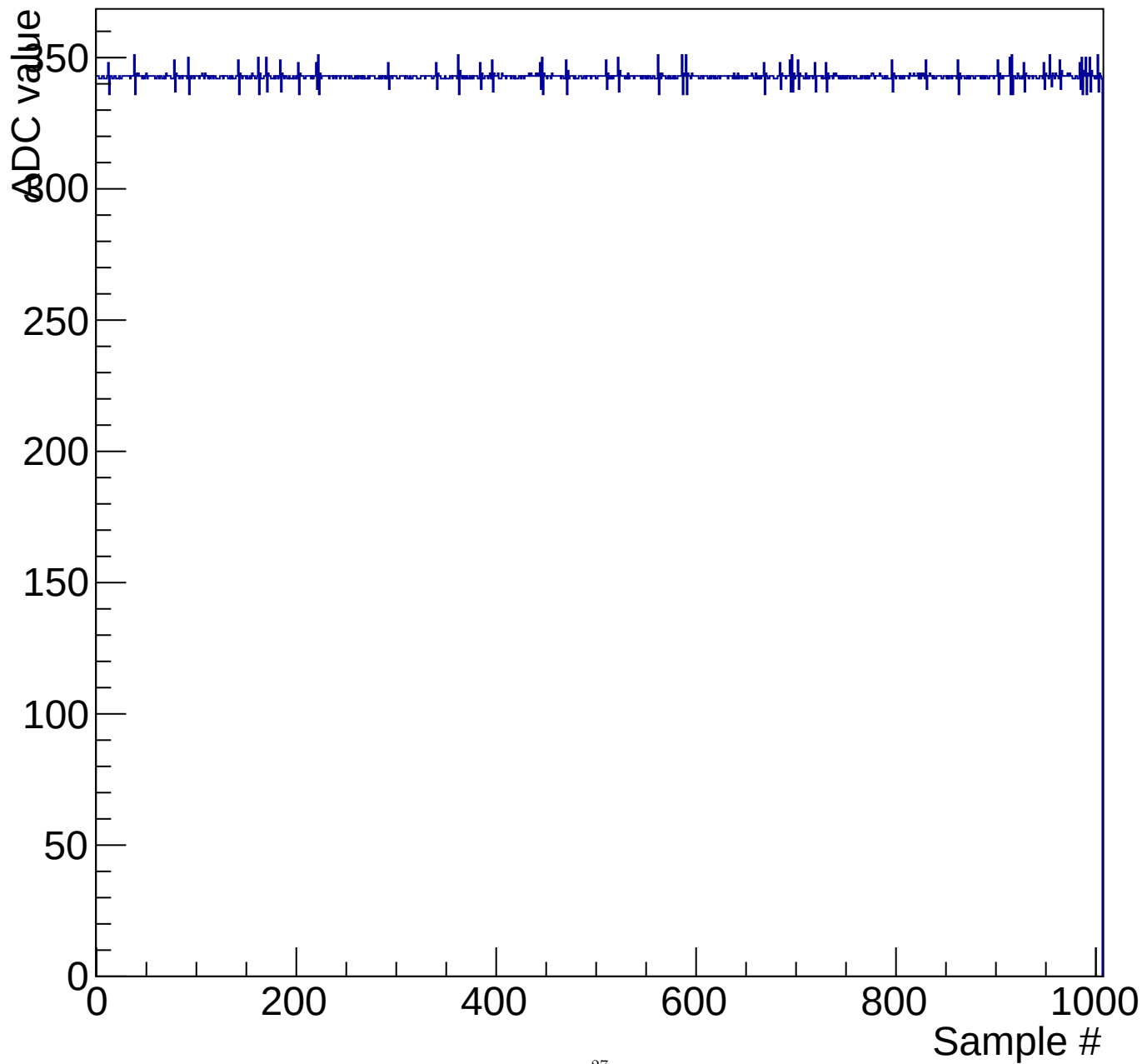
Run 34385 Event 2 Chip 38 Channel_2



Run 34386 Event 150 Chip 38 Channel_2



Run 26840 Event 5 Chip 39 Channel_7



Run 27785 Event 14 Chip 43 Channel_13

