

20180820

We have tested two batches (batch 1 with 34 and batch 2 with 50 chips) of Novapack packaged chips. Two test setups have been used, the CERN testboard which was used to characterize the chip, and the socketmcm board developed in Lund.

Test of batch 1 on CERN testboard and LUND socketmcm.

Summary of test results:

Chip	socketmcm	cern testboard
65	ch2 high-low	ch2 high low
63	ch9 high-low	ch9 high-low
62	ch1 high-low	ch1 high-low
61	OK	OK
60	ch11 high-low	ch11 high-low
57	ch12 high low (weak)	ch1 bit error(?)
55	ch15 bit error, also ramp	ch15 bit error, also ramp
52	ch9 high-low	ch9 bit error, high-low weak
40	ch14 bit error?	Chip not working, readout errors.
38	ch2 bit error, also ramp	ch2 bit error, also ramp. Ch4 suspect.

All other chips and channels seems OK. Chip 61 was tested on both setup as a “good” reference chip. *High-low* means that the time samples in pedestals is: low, high,low,high,low, etc. i.e. every second time slice has a high value, every second time slice has a low value.

Ramp means that data was written into the pedestal memory and was used as data.

Pulse is a capacitive coupled square pulse on the inputs to the chip. I.e there is in the plots with a pulse sometimes a positive going pulse, from the rising edge, and a negative going pulse, from the falling edge.

Software trigger was used. 20 MHz sampling. Did also try auxiliary clock on some chips. No change.

Nominal reference voltages (V):

	CERN testboard	LUND socketmcm
refp	1.365	1.25
refn	0.276	0.25
vcm	0.819	0.75
cmout	0.819	0.75

Below are summary plots. They show pedestals, time sweeps for the faulty channels and for various settings and pulsing. All to illustrate the particular problem.

Nominal setting was gain=0 (lowest), shaping = 120 ns, polarity=1.

gain3=highest gain.

Ch=channel.

Preampmode = shaper is not used. This was used to be able to get a pulse with long tail to get the full ADC scale in one event.

Ramp = pedestal memory used as data, 0-1000.

Not that channel 0 is noisy on the CERN testboard, this is not seen on LUND socketmcm.

Page 4-7 CHIP 63 (CERN testboard)

pedestals for all channels

pedestals for channel 9

time sweep of a pedestal event channel 9

time sweep for event with a pulse, highest gain and preampmode for channel 9

Page 8-12 CHIP 62 (CERN testboard)

pedestals for all channels

pedestals for channel 1

time sweep of a pedestal event channel 1, zoomed to show time sample 100 to 200.

time sweep of a pedestal event channel 1, all 1000 time samples.

time sweep for event with a pulse, highest gain and preampmode for channel 1:

→ The high low is seen both at large and small ADC value, in the central it is not seen.

Page 13-15 CHIP 60 (CERN testboard)

pedestals for all channels

time sweep in preampmode and second highest gain for channel 11.

time sweep for event with a pulse, highest gain and preampmode for channel 11.

Using different show that is not gain dependent.

Page 16-17 CHIP 57 (CERN testboard)

pedestals for all channels

pedestals channel 1: sometimes a bit (=512) is set. Not seen on Lund socketmcm.

Page 18-20 CHIP 55 (CERN testboard)

pedestals for channel 15: sometimes a bit (=256) is set.

time sweep for event with a pulse, highest gain and preampmode for channel 15.

Note the positive and negative going pulses are from induced signals of an incoming square pulse.

A bit is clearly flipping.

Time sweep for a ramp (auxiliary clock) channel 15. It should be a straight line 0-1000, clearly bit error.

Page 21-23 CHIP 52 (CERN testboard)

time sweep for event with a pulse, highest gain and preampmode for channel 8. All good.

time sweep for event with a pulse, highest gain and preampmode for channel 9. (high pulse height)
Some spikes.

time sweep for event with a pulse, highest gain and preampmode for channel 9. (low pulse height)
Some spikes.

CHIP 40 (CERN testboard)

Readout errors, not possible to read.

Not further investigated yet.

No plot.

Page 24-27 CHIP 38 (CERN testboard)

pedestals highest gain and preampmode for channel 2. A bit (=64) is sometimes set.

time sweep for pedestal event with highest gain and preampmode for channel 2. Some spikes.

time sweep for event with a pulse, highest gain and preampmode for channel 2. Some spikes.
time sweep for event with ramp data from pedestal memory for channel 2. Some spikes.
Should be a straight line 0-1000.

Test of batch 2 on LUND socketmcm

None of the above problems was seen. Summary:

Chip 16: Register test OK, do not get any events.

Chip 30: short between ground and iopower.

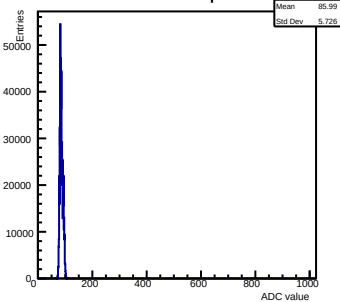
Chip 31: no connection with any pin (as measured over protection diod).

Chip 75: draw less current (0.36A expect 0.47A). Register test fails.

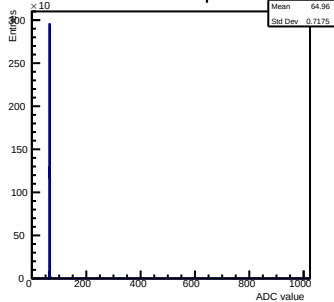
Page 28: Some chips are “nosit” for some settings (in preampmode)

Page 29: Some channel have some bit missing (also when using pedestal memory as data), always at time slice 504 for the channel shown.

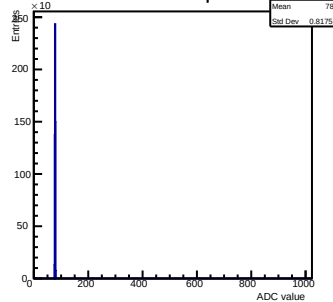
Pedestals ch 0 chip 63 nom



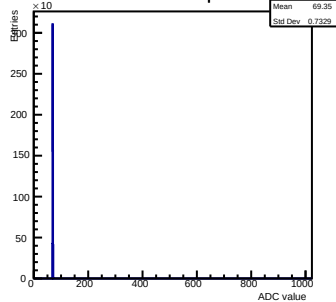
Pedestals ch 1 chip 63 nom



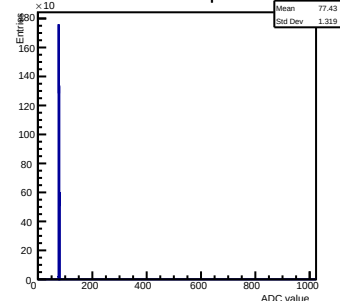
Pedestals ch 2 chip 63 nom



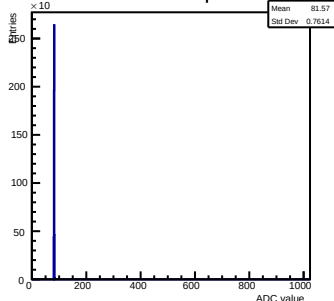
Pedestals ch 3 chip 63 nom



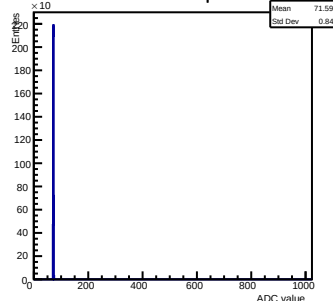
Pedestals ch 4 chip 63 nom



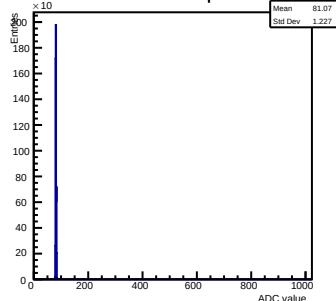
Pedestals ch 5 chip 63 nom



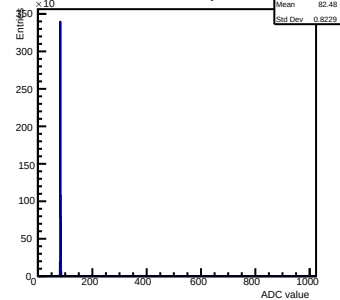
Pedestals ch 6 chip 63 nom



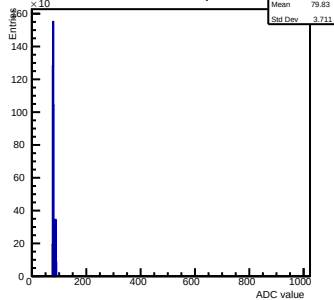
Pedestals ch 7 chip 63 nom



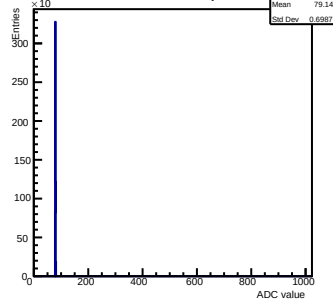
Pedestals ch 8 chip 63 nom



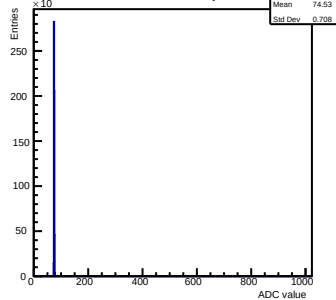
Pedestals ch 9 chip 63 nom



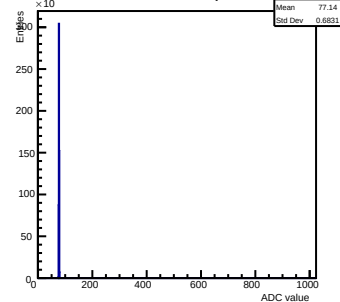
Pedestals ch 10 chip 63 nom



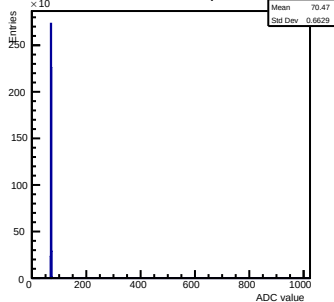
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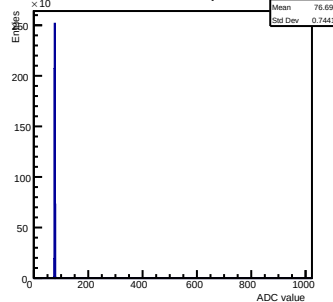
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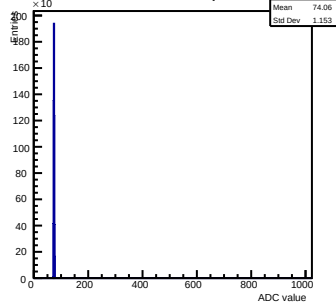
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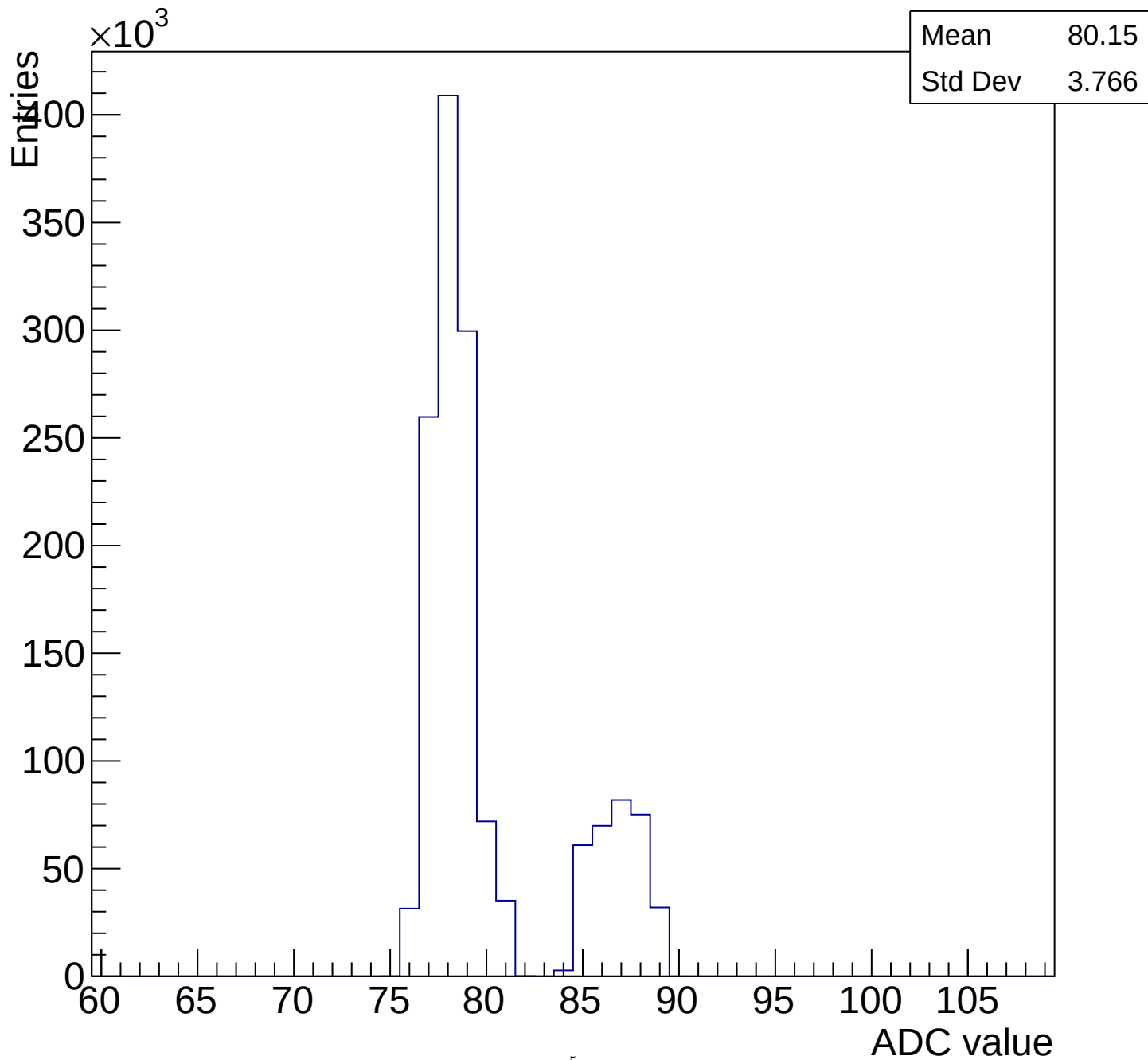
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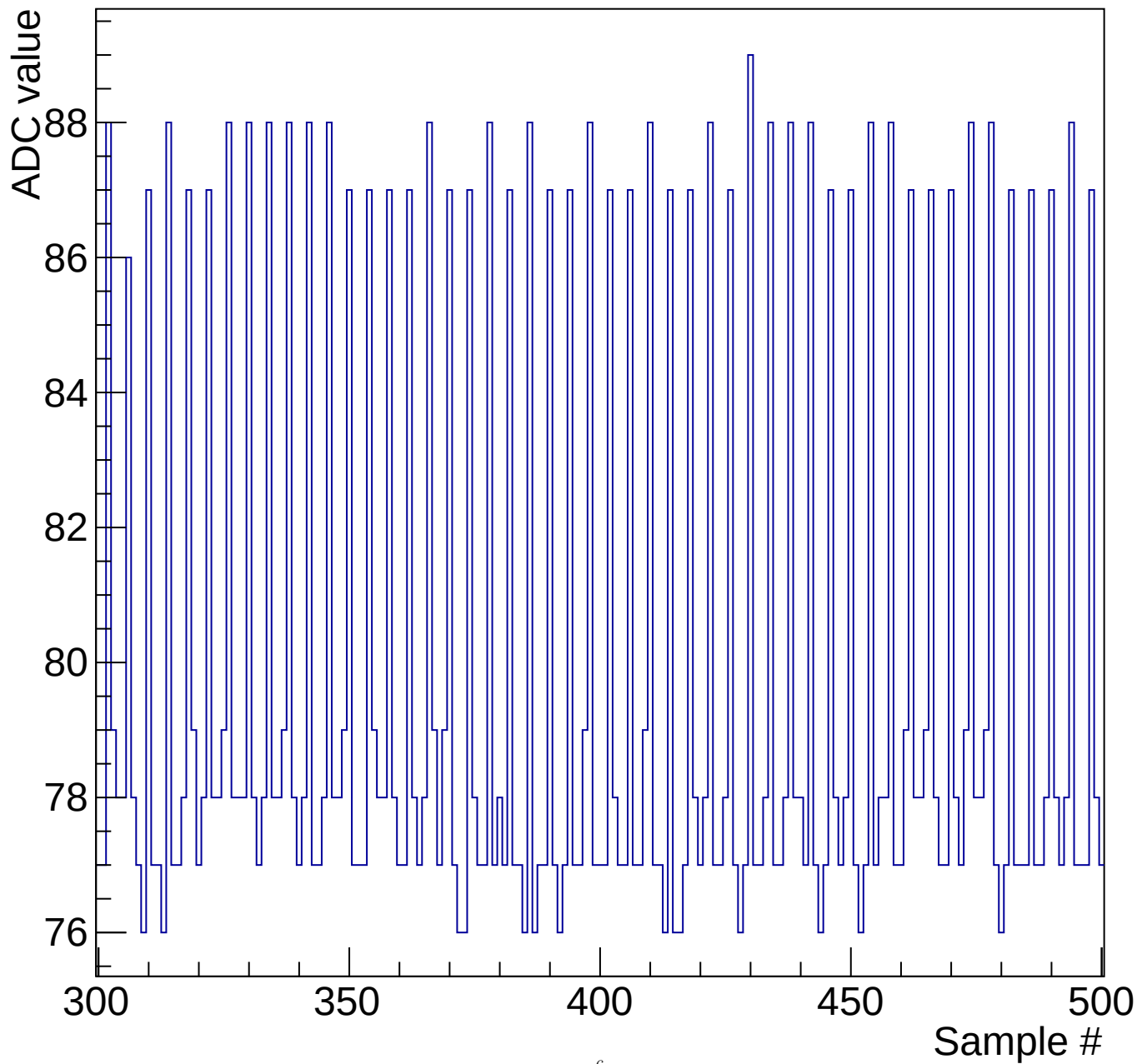
Pedestals ch 15 chip 63 nom



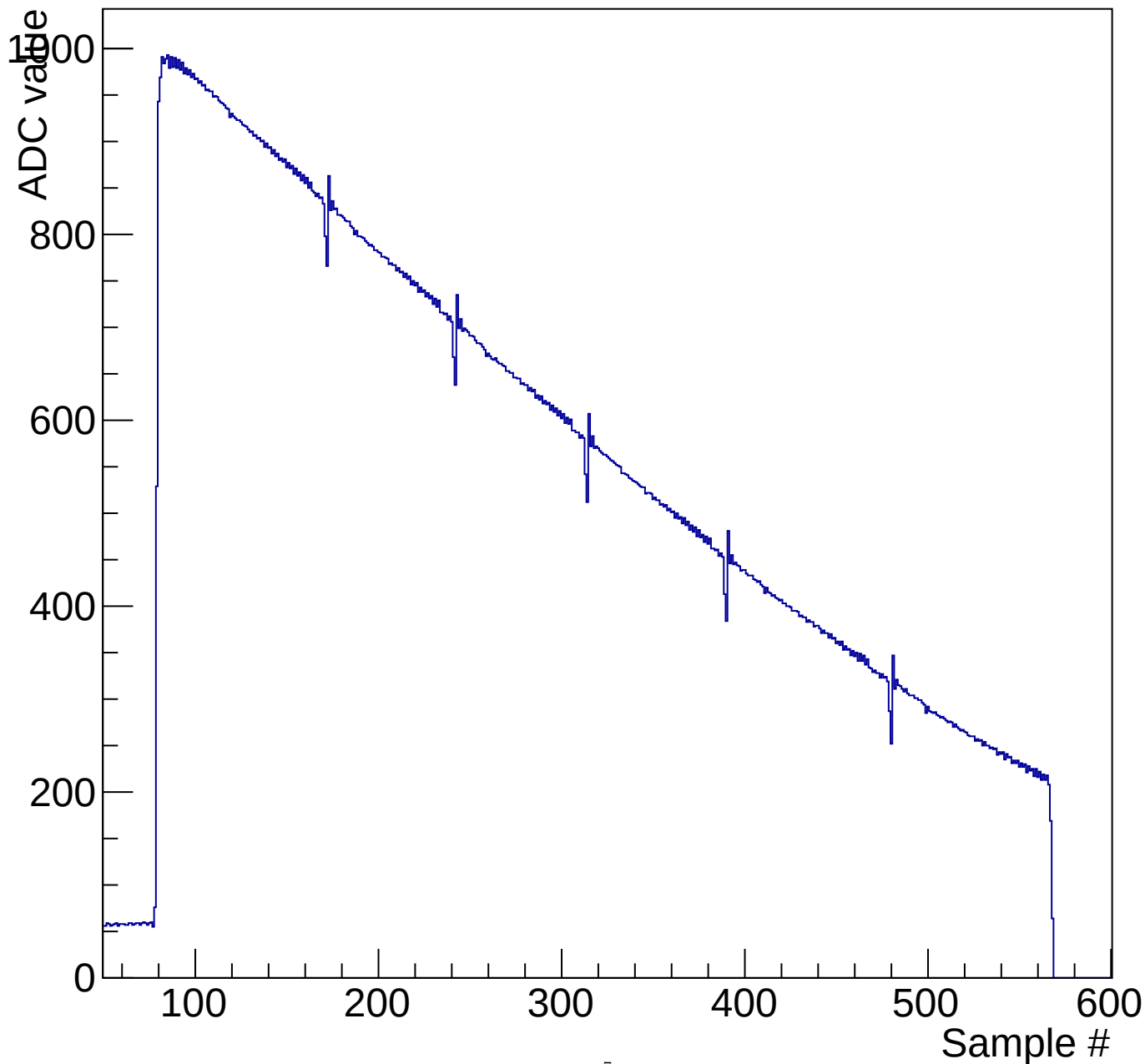
Pedestals ch 9 chip 63 run 34339 nom



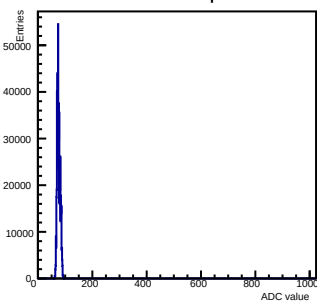
Run 34339 Event 2 Chip 63 Channel_9



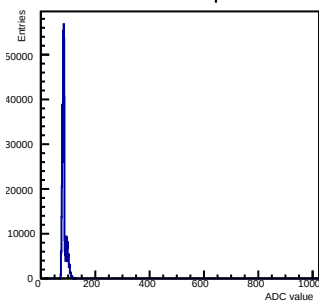
Run 34346 Event 7 Chip 63 Channel_9



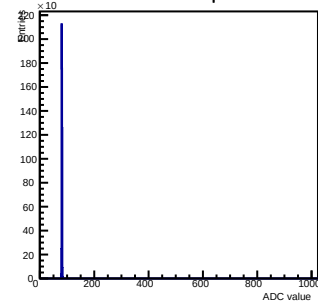
Pedestals ch 0 chip 62 nom



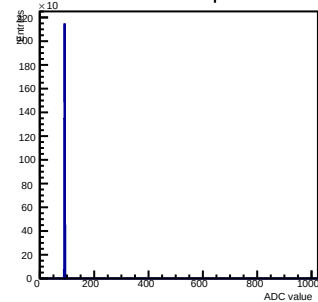
Pedestals ch 1 chip 62 nom



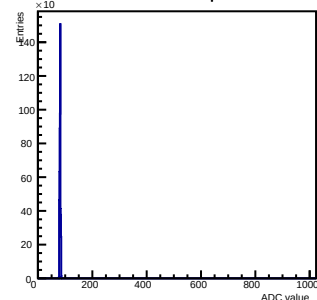
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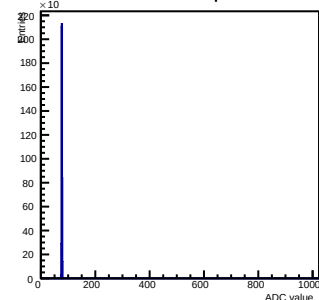
Pedestals ch 3 chip 62 nom



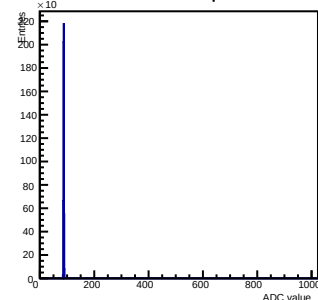
Pedestals ch 4 chip 62 nom



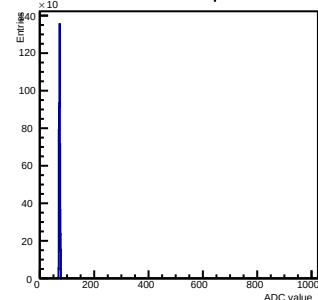
Pedestals ch 5 chip 62 nom



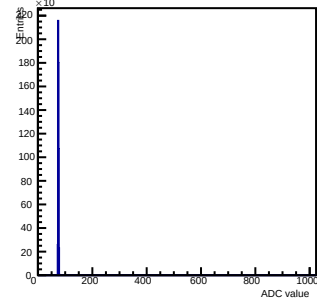
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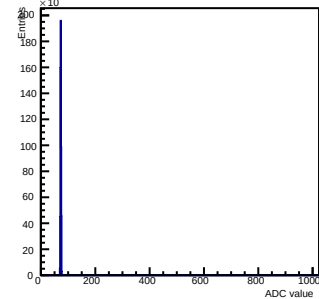
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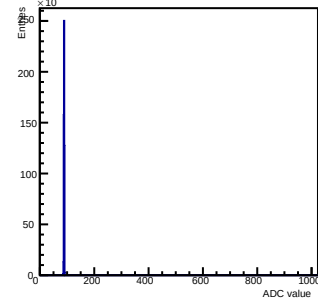
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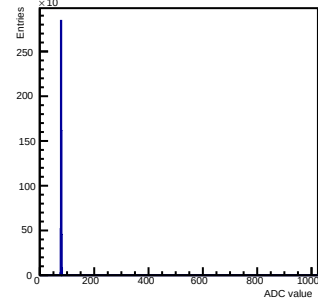
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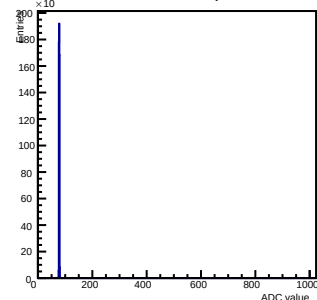
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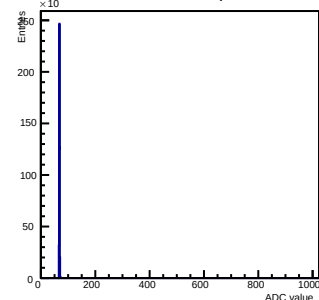
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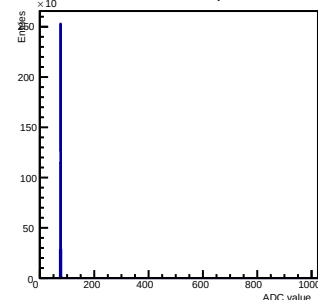
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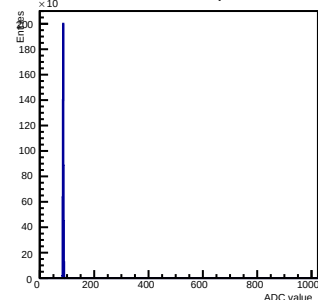
Pedestals ch 13 chip 62 nom



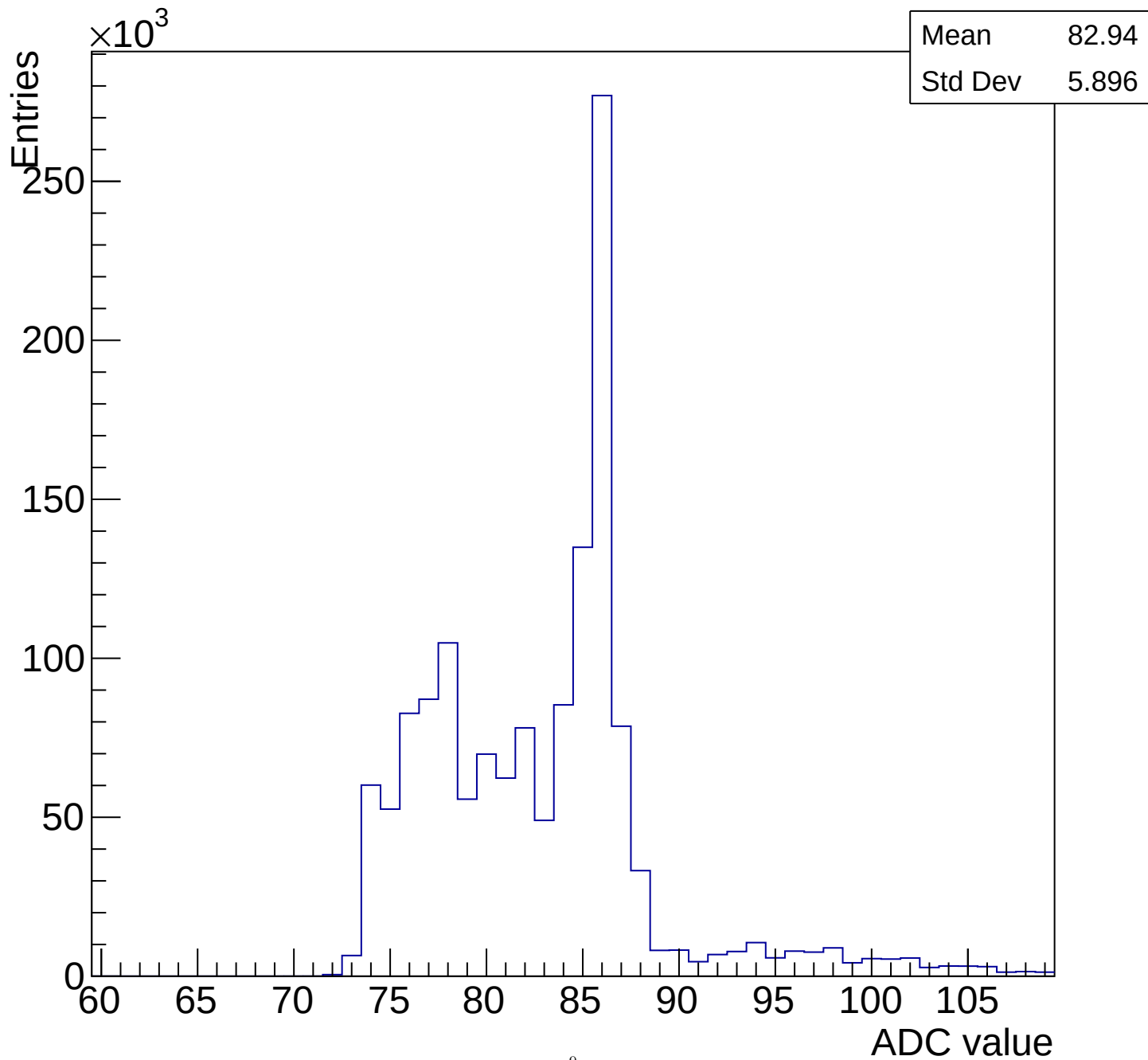
Pedestals ch 14 chip 62 nom



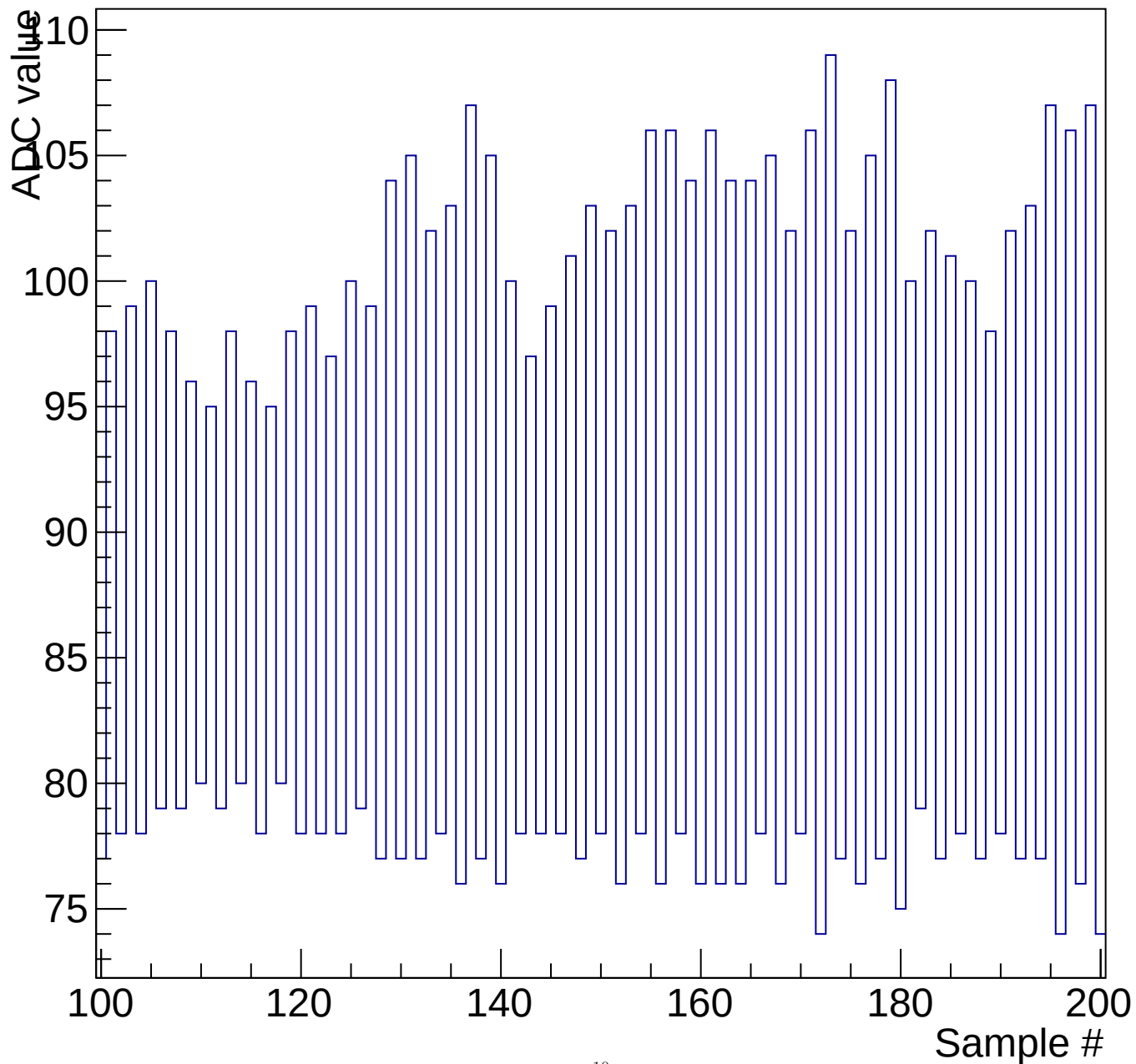
Pedestals ch 15 chip 62 nom



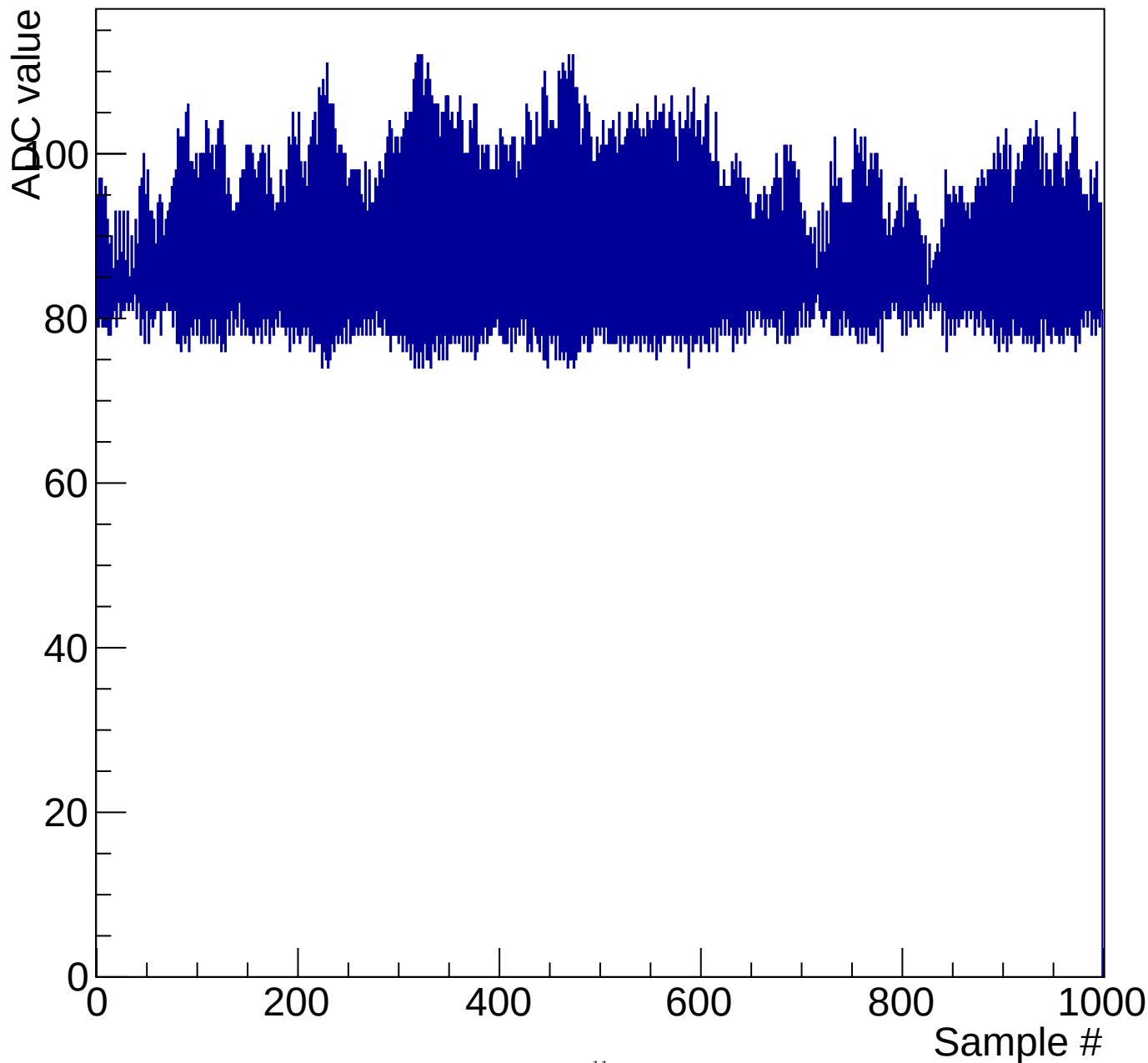
Pedestals ch 1 chip 62 run 34351 nom



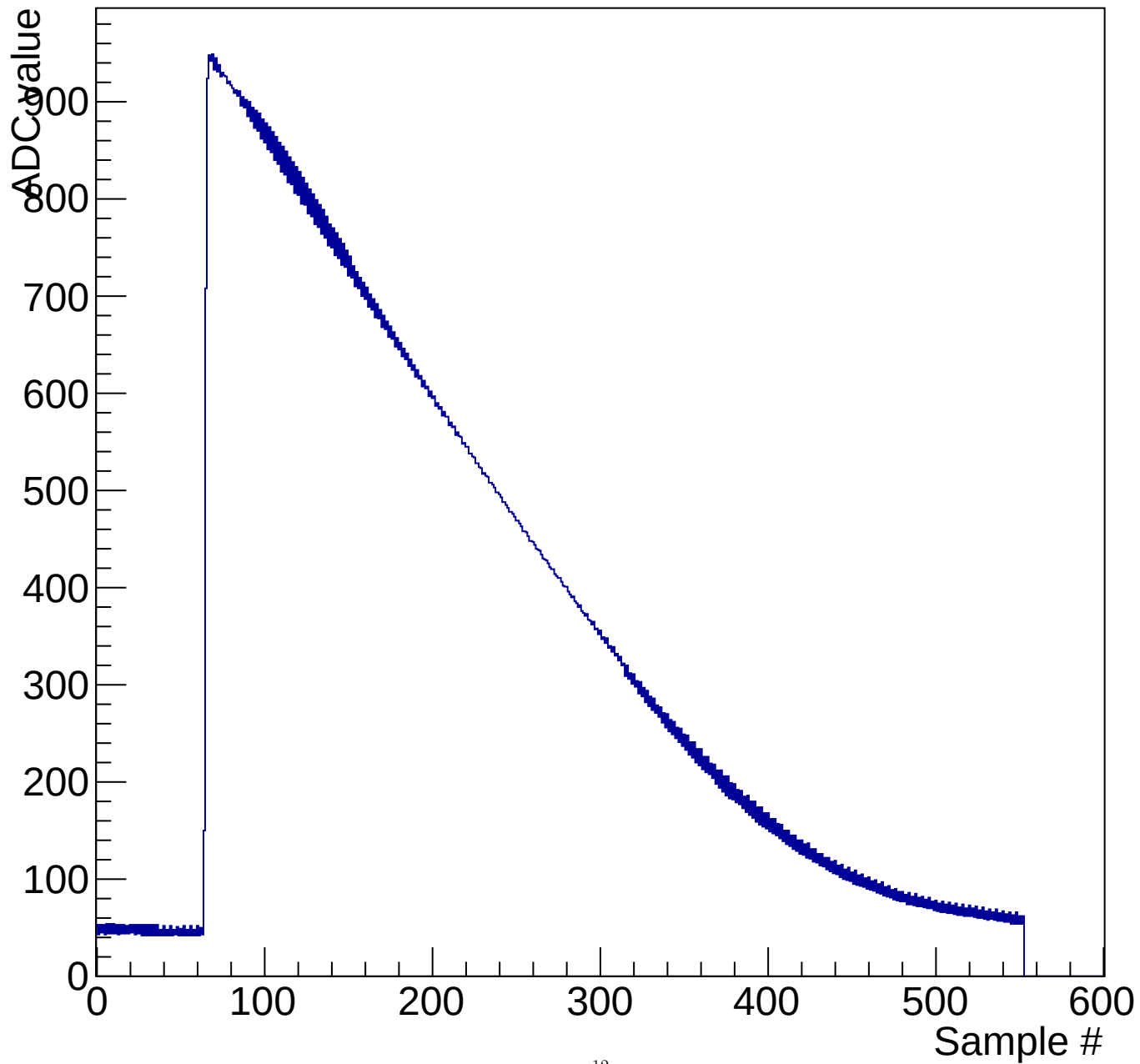
Run 34351 Event 1 Chip 62 Channel_1



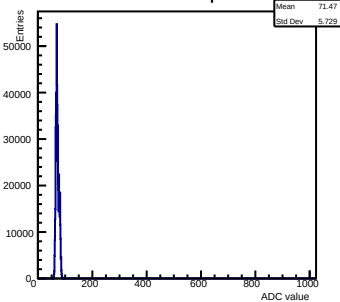
Run 34351 Event 2 Chip 62 Channel_1



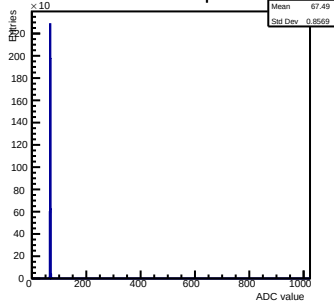
Run 34354 Event 126 Chip 62 Channel_1



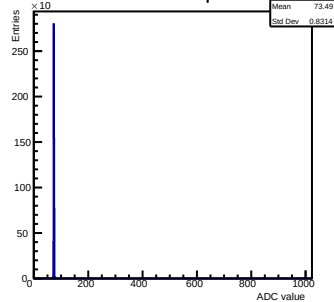
Pedestals ch 0 chip 60 nom



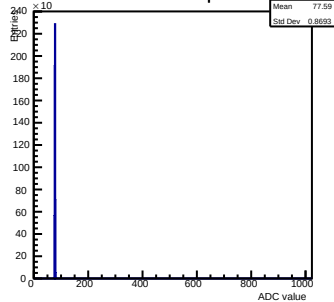
Pedestals ch 1 chip 60 nom



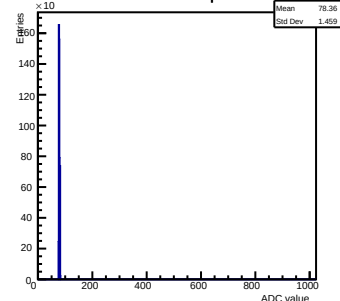
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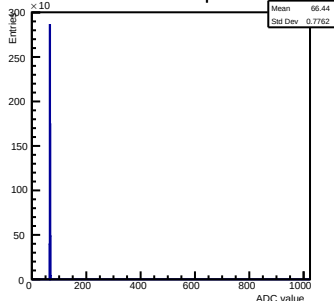
Pedestals ch 3 chip 60 nom



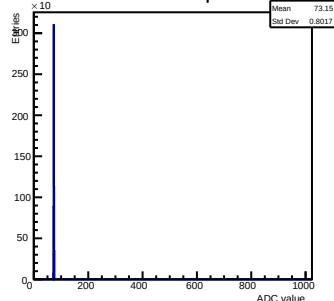
Pedestals ch 4 chip 60 nom



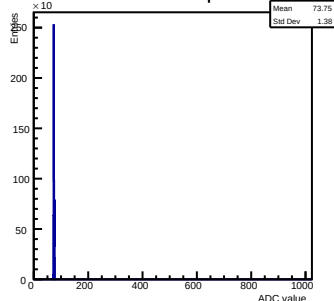
Pedestals ch 5 chip 60 nom



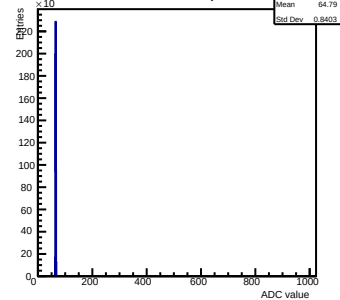
Pedestals ch 6 chip 60 nom



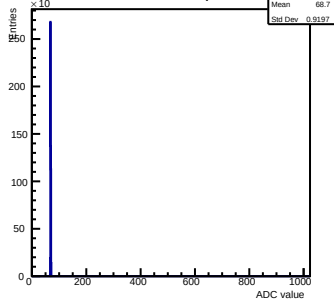
Pedestals ch 7 chip 60 nom



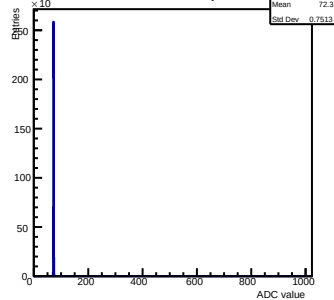
Pedestals ch 8 chip 60 nom



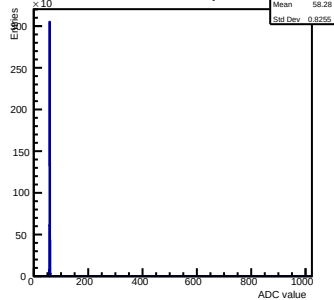
Pedestals ch 9 chip 60 nom



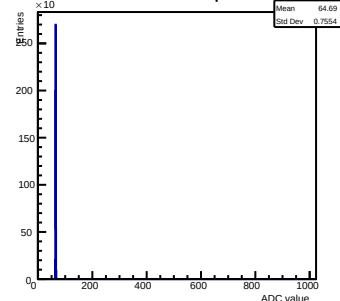
Pedestals ch 10 chip 60 nom



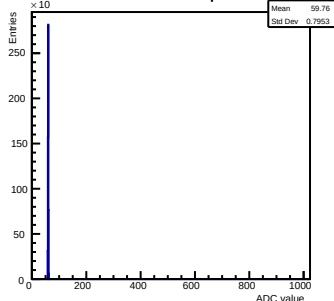
Pedestals ch 11 chip 60 nom



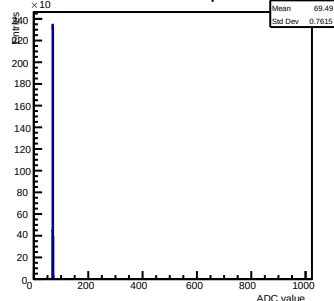
Pedestals ch 12 chip 60 nom



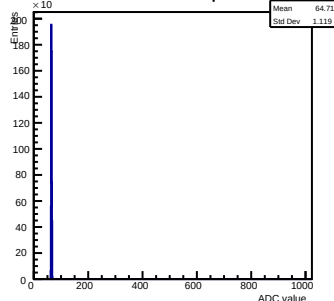
Pedestals ch 13 chip 60 nom



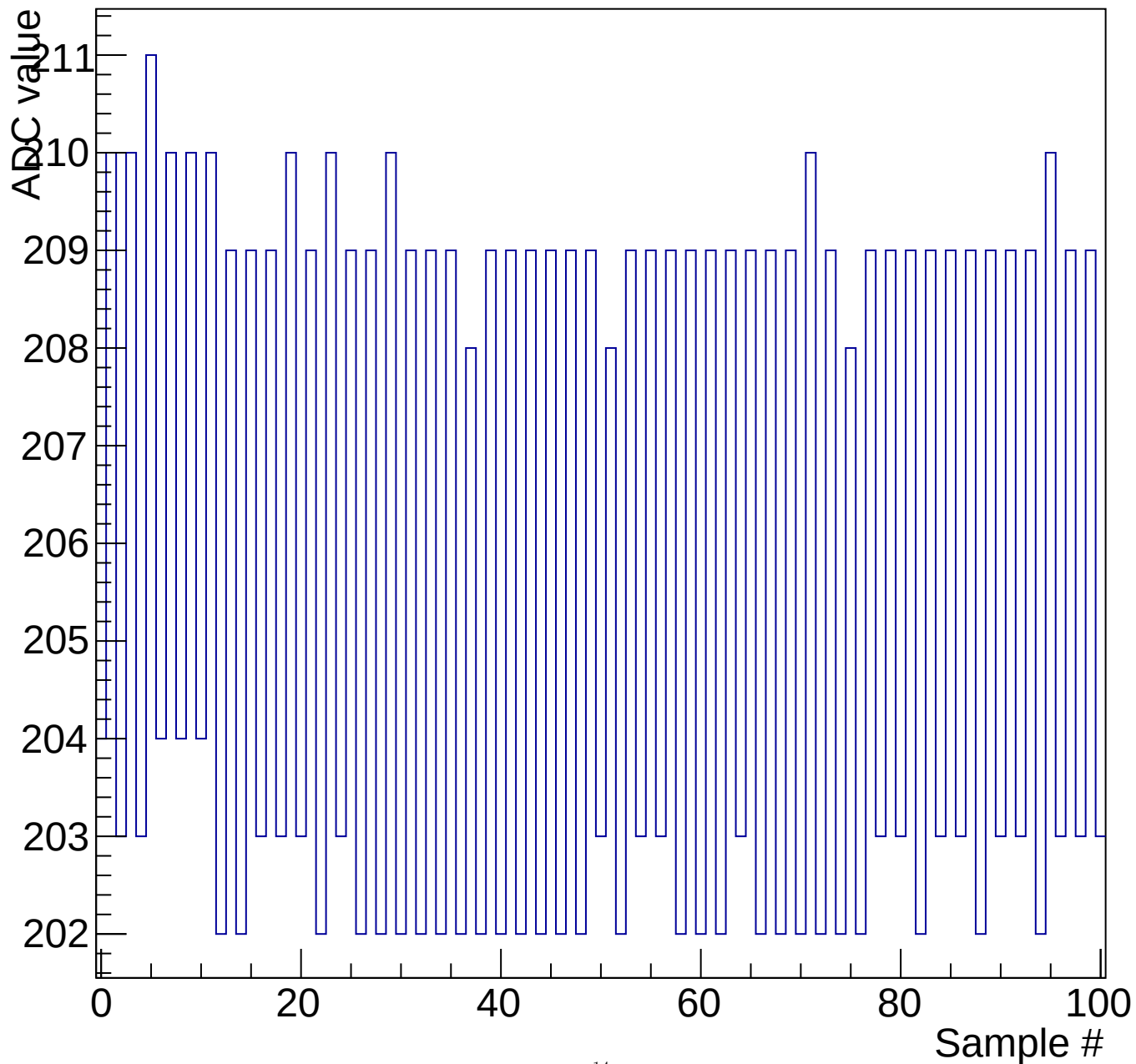
Pedestals ch 14 chip 60 nom



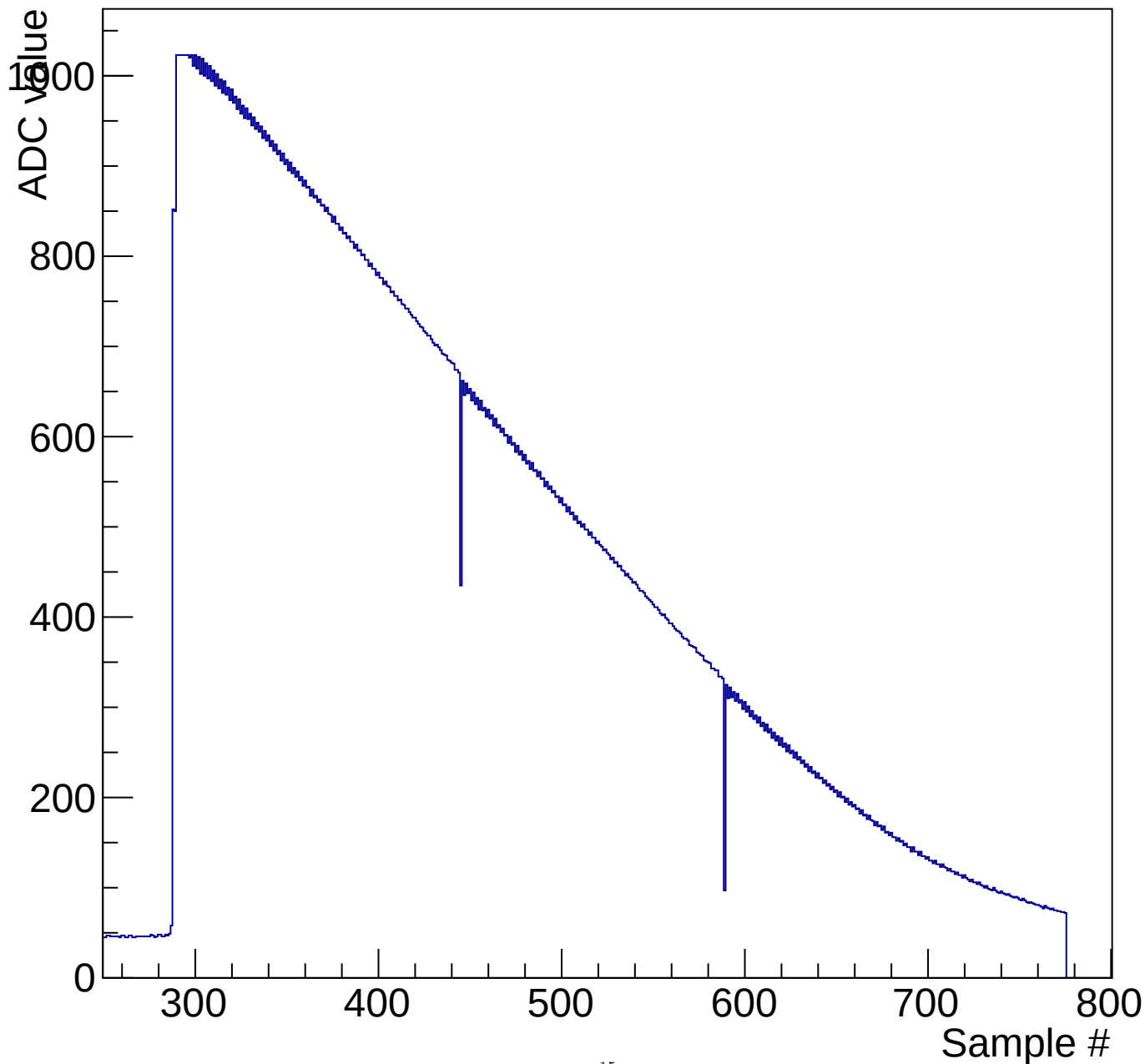
Pedestals ch 15 chip 60 nom

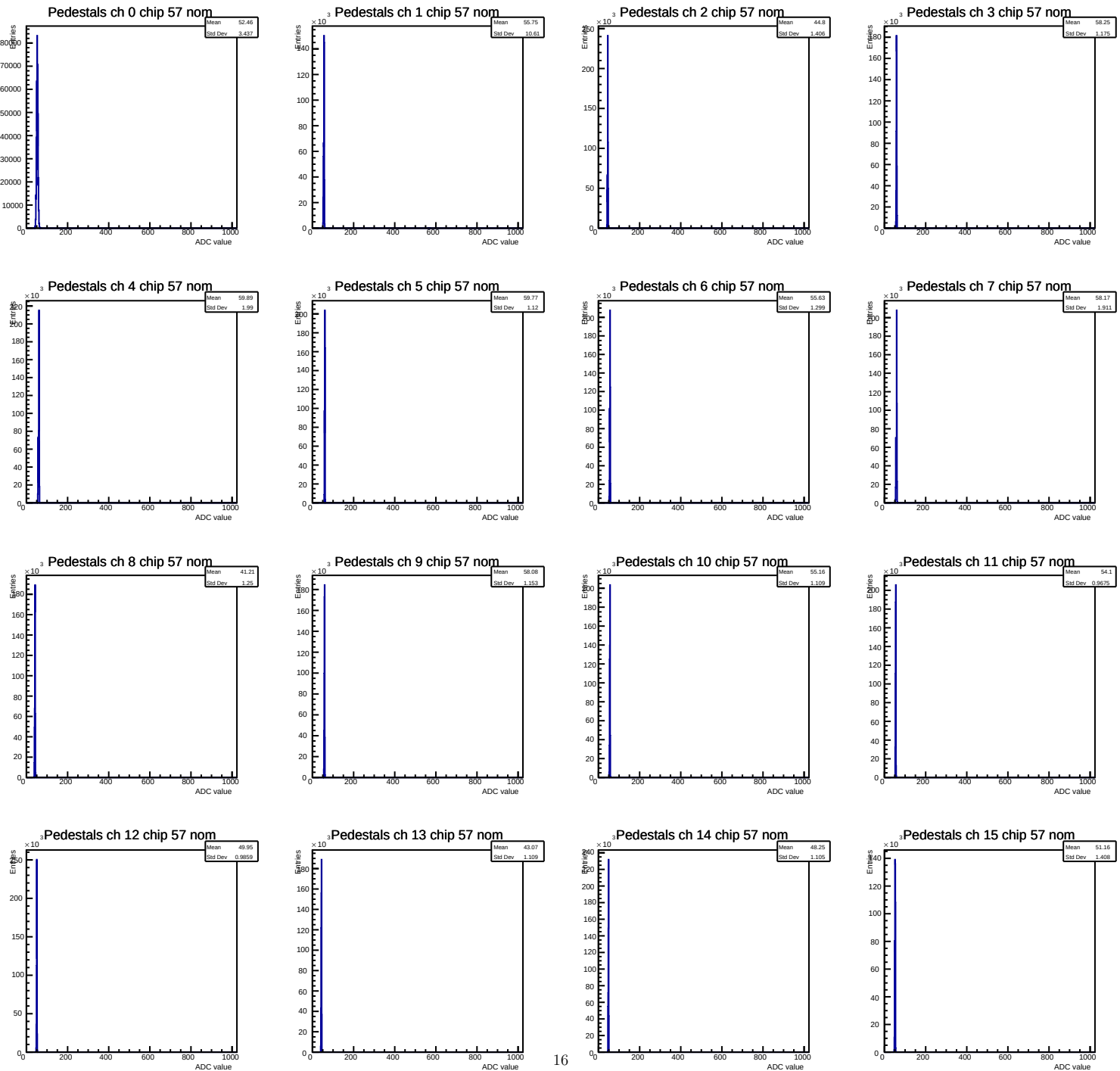


Run 34362 Event 1 Chip 60 Channel_11

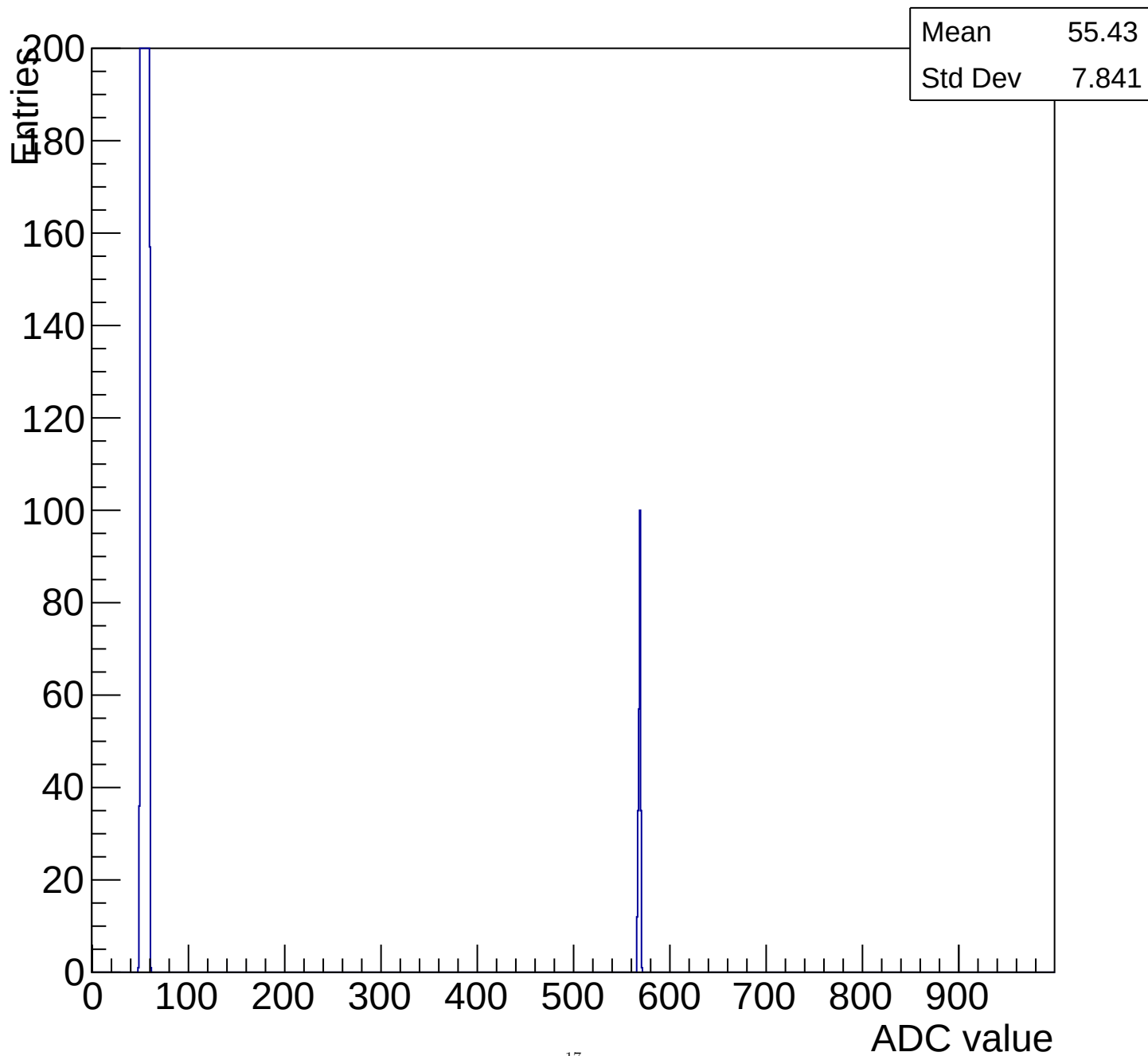


Run 34365 Event 95 Chip 60 Channel_11

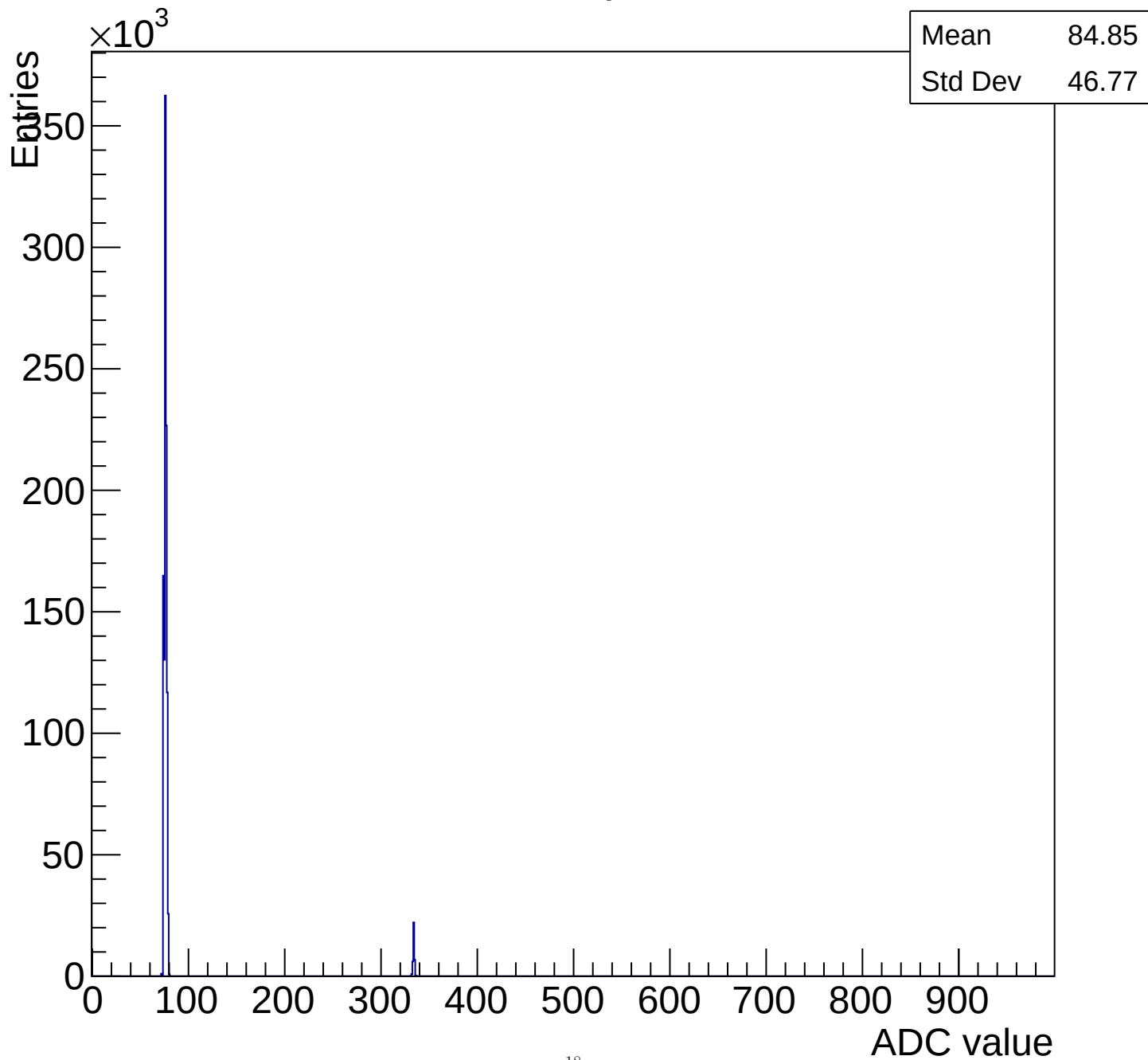




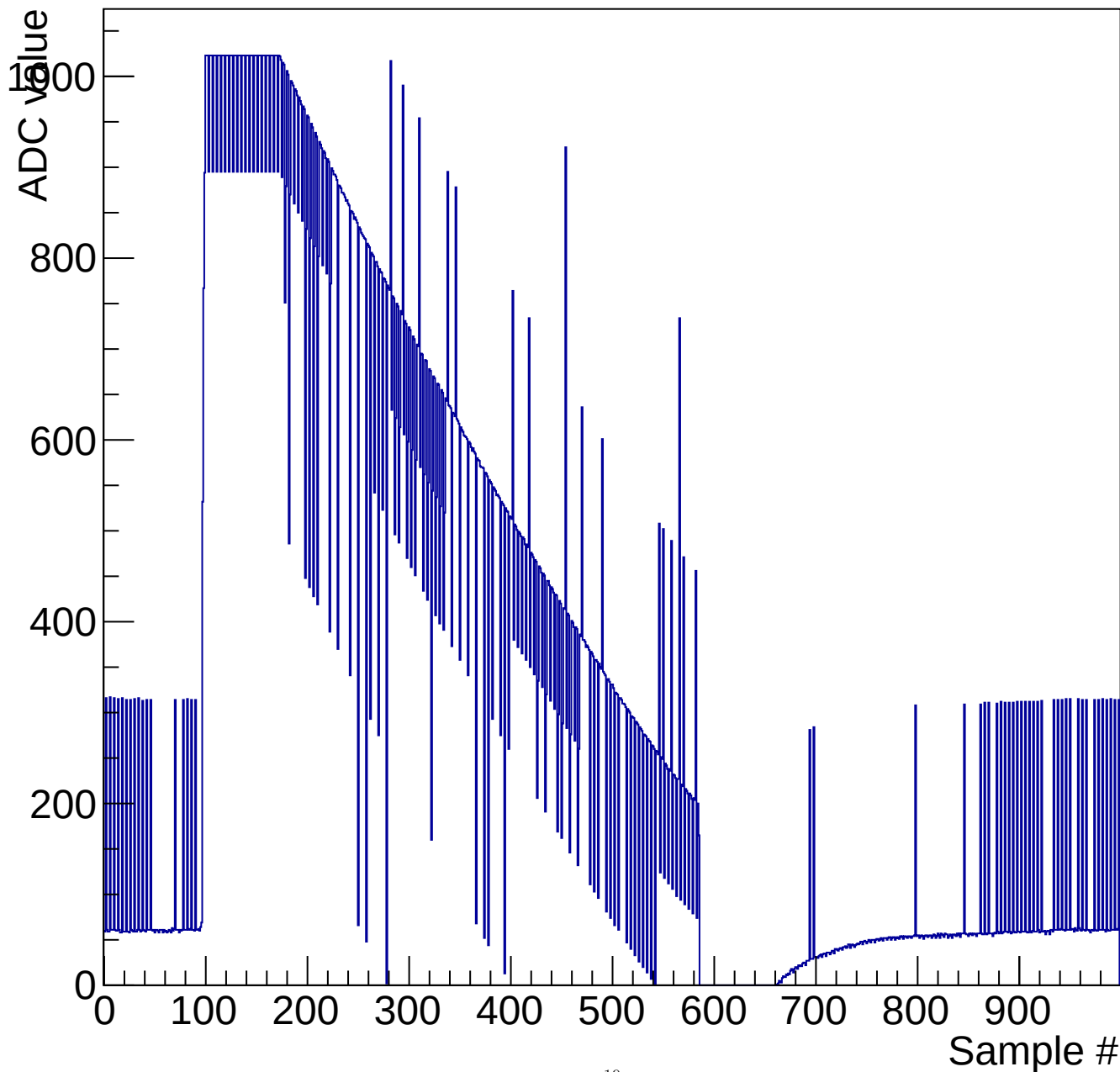
Pedestals ch 1 chip 57 run 34366 nom



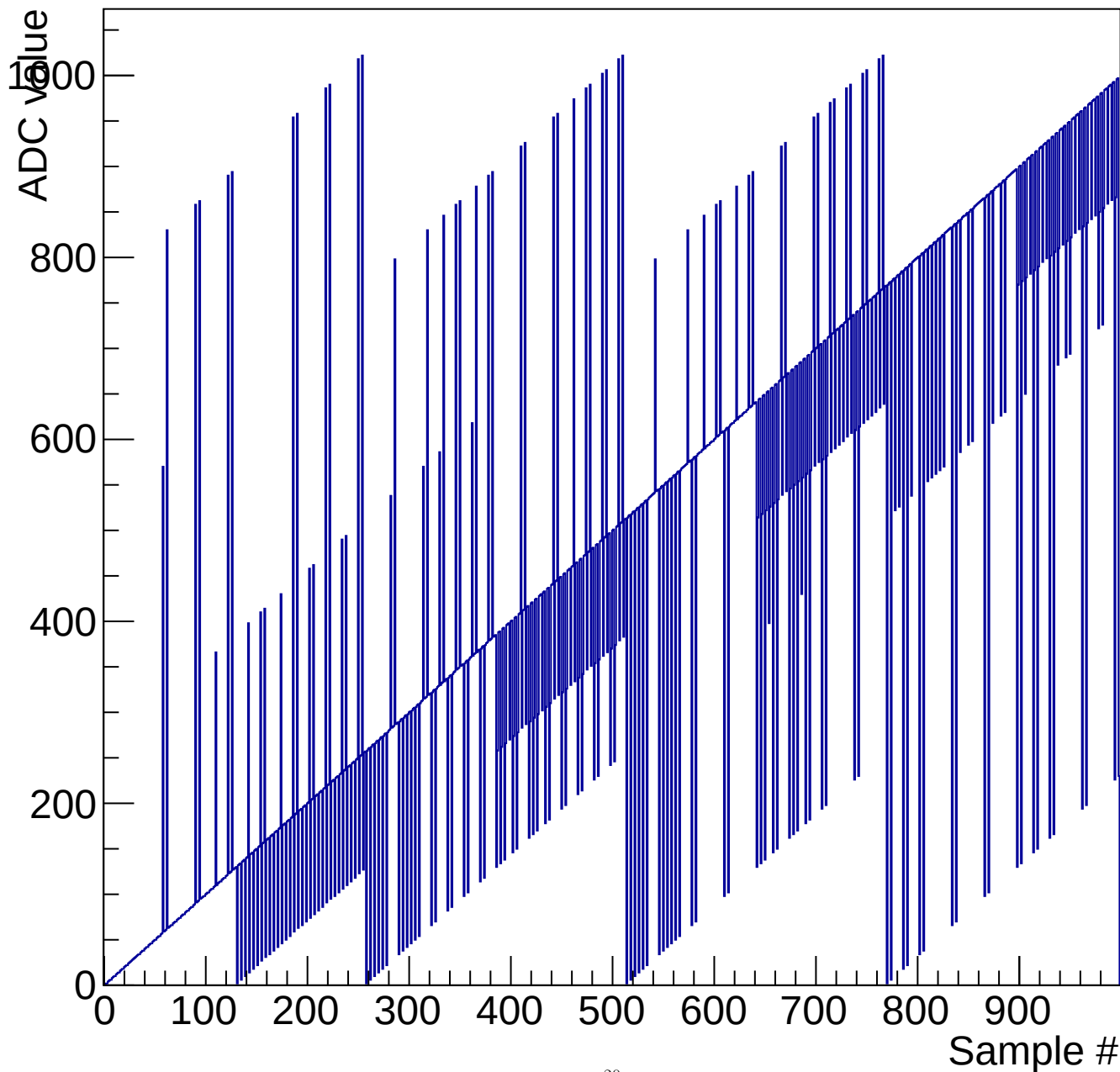
Pedestals ch 15 chip 55 run 34369 1



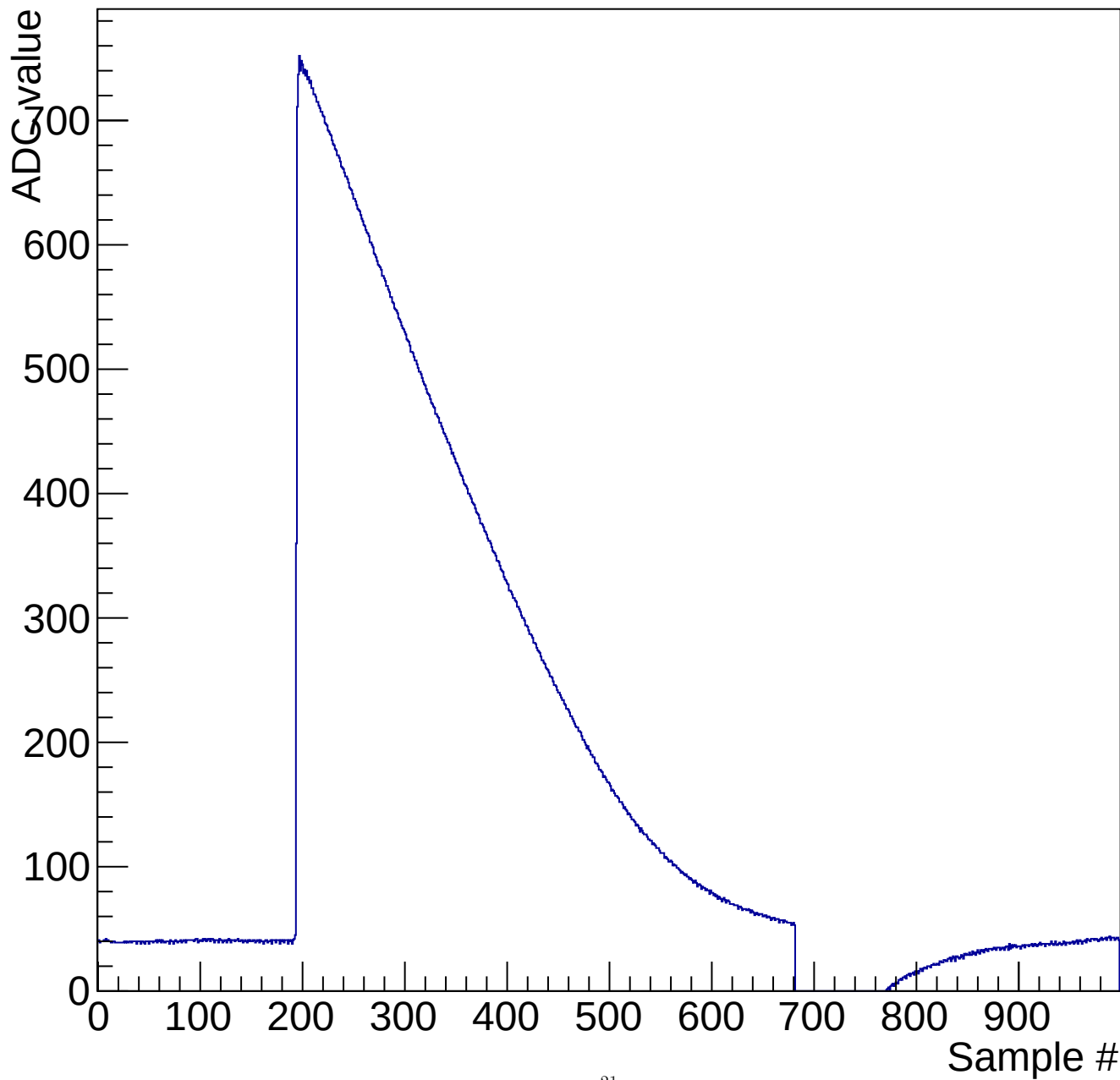
Run 34370 Event 1 Chip 55 Channel_15



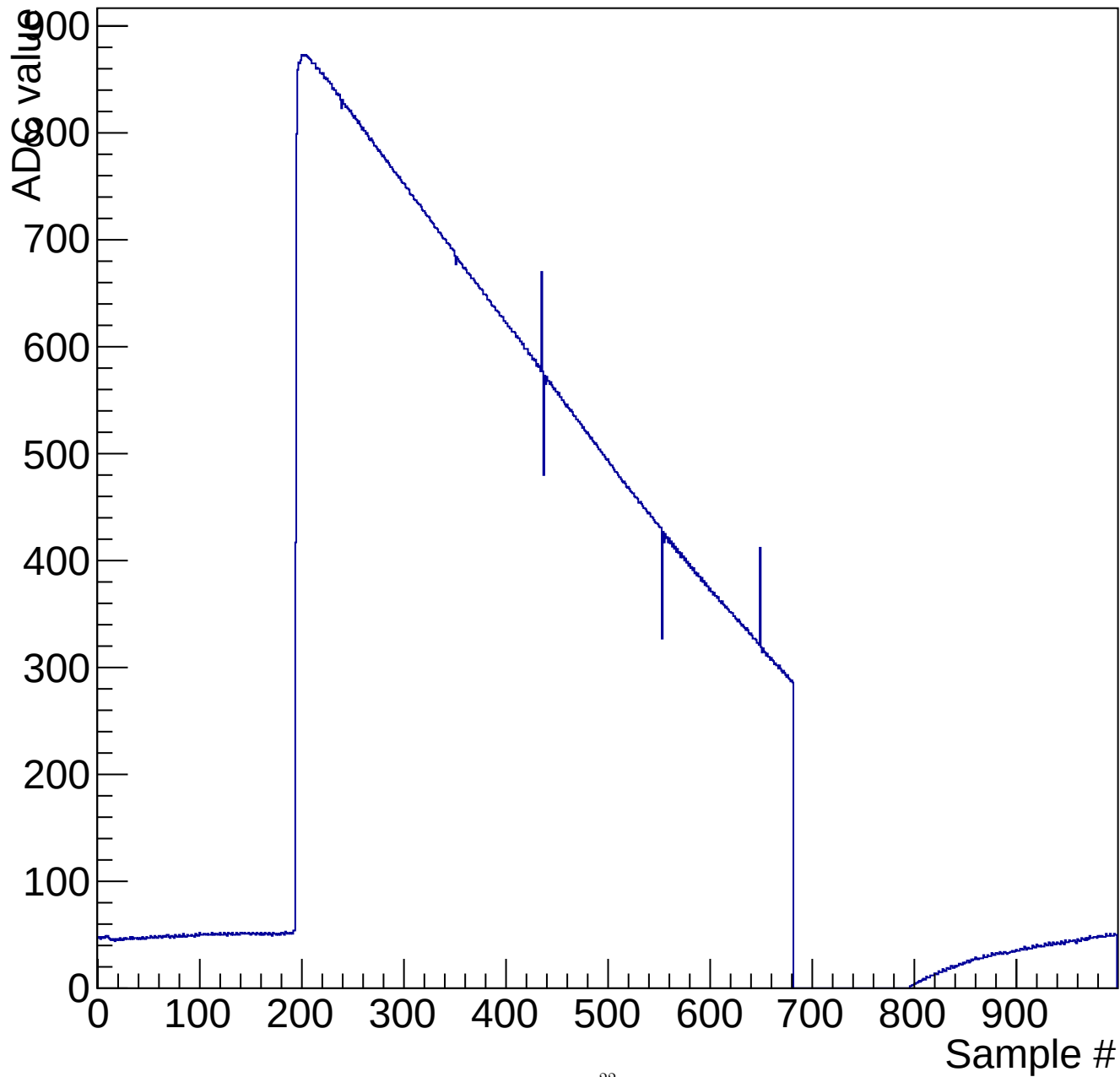
Run 34374 Event 1 Chip 55 Channel_15



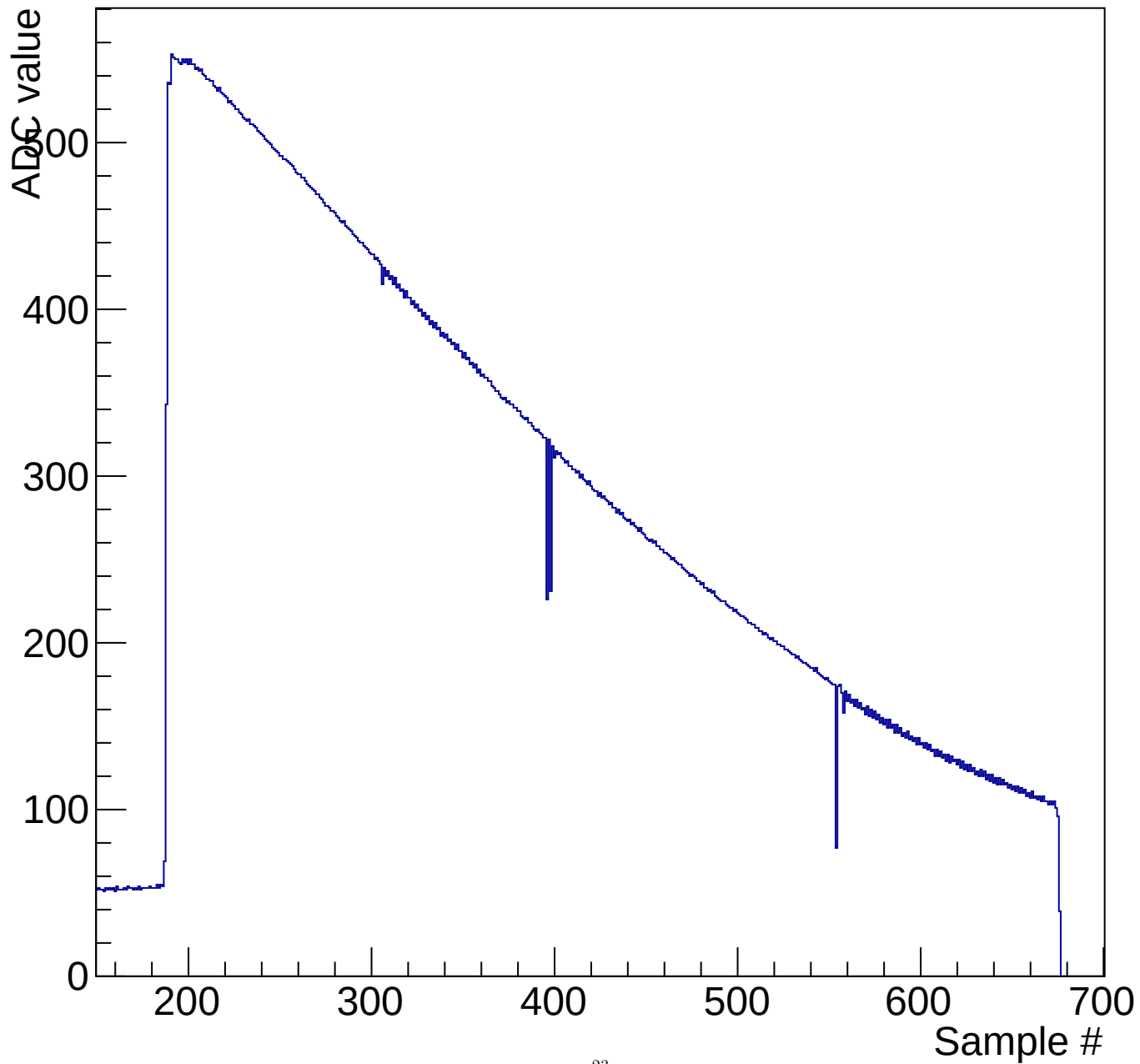
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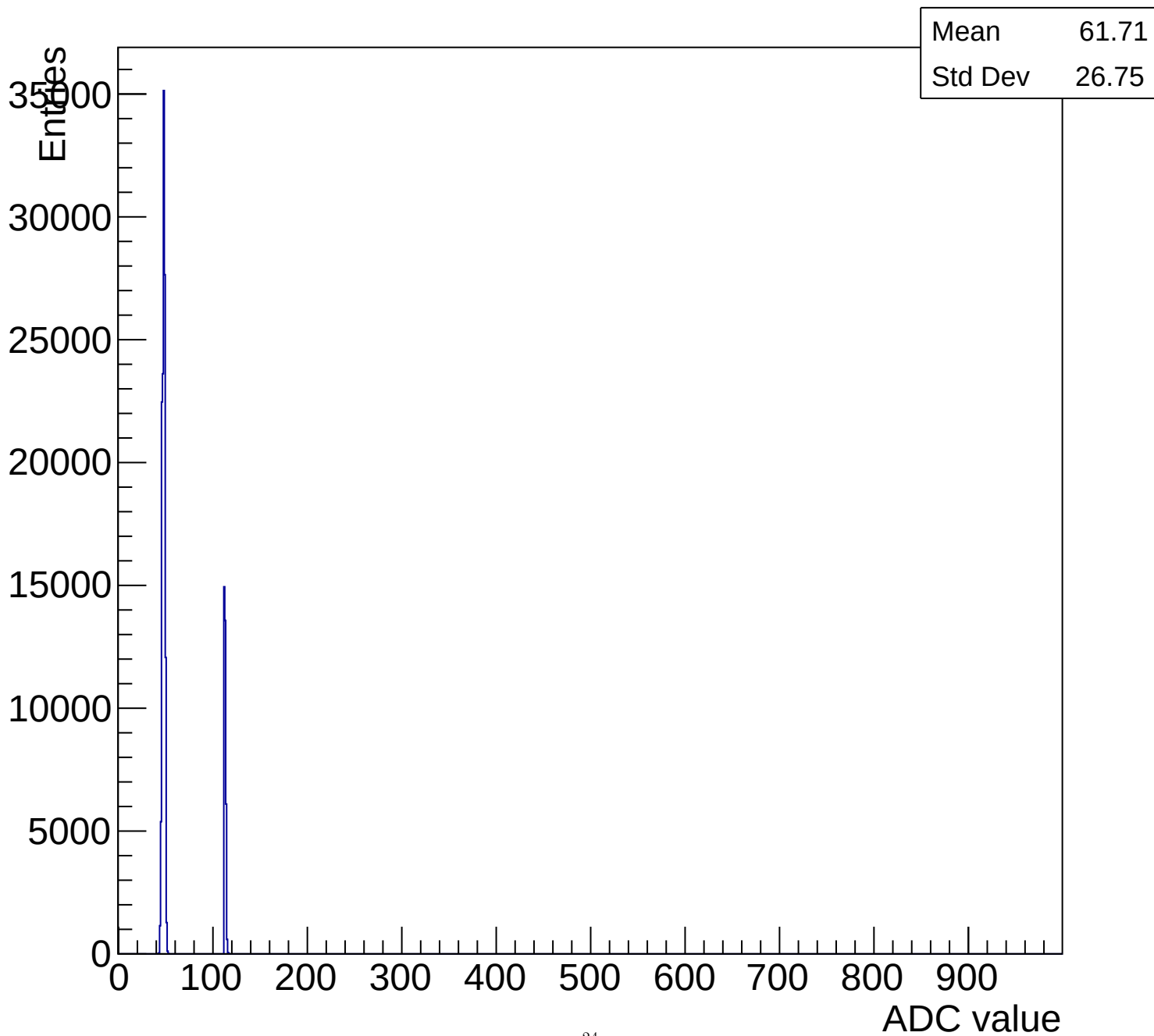
Run 34376 Event 134 Chip 52 Channel_9



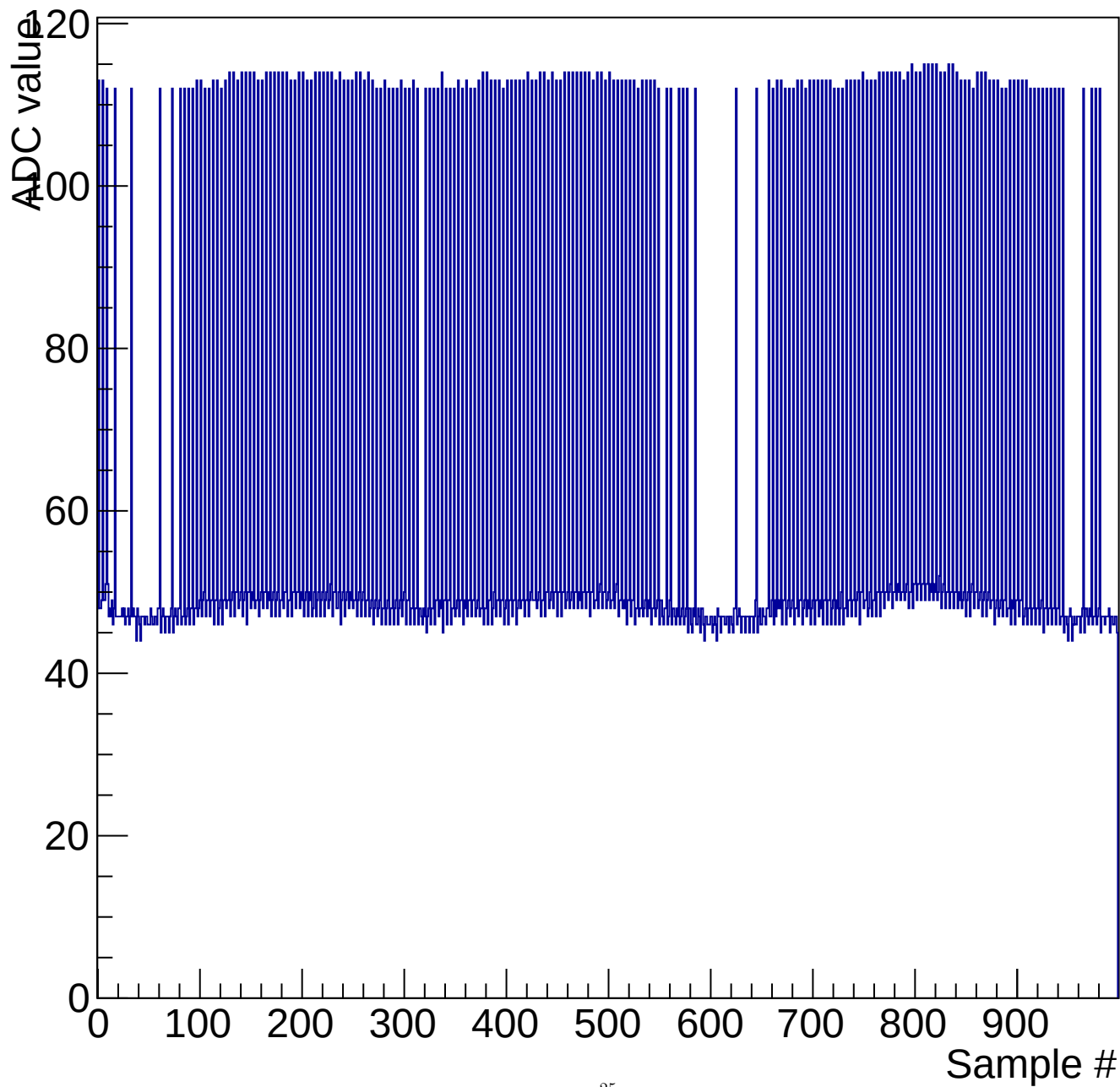
Run 34380 Event 1 Chip 52 Channel_9



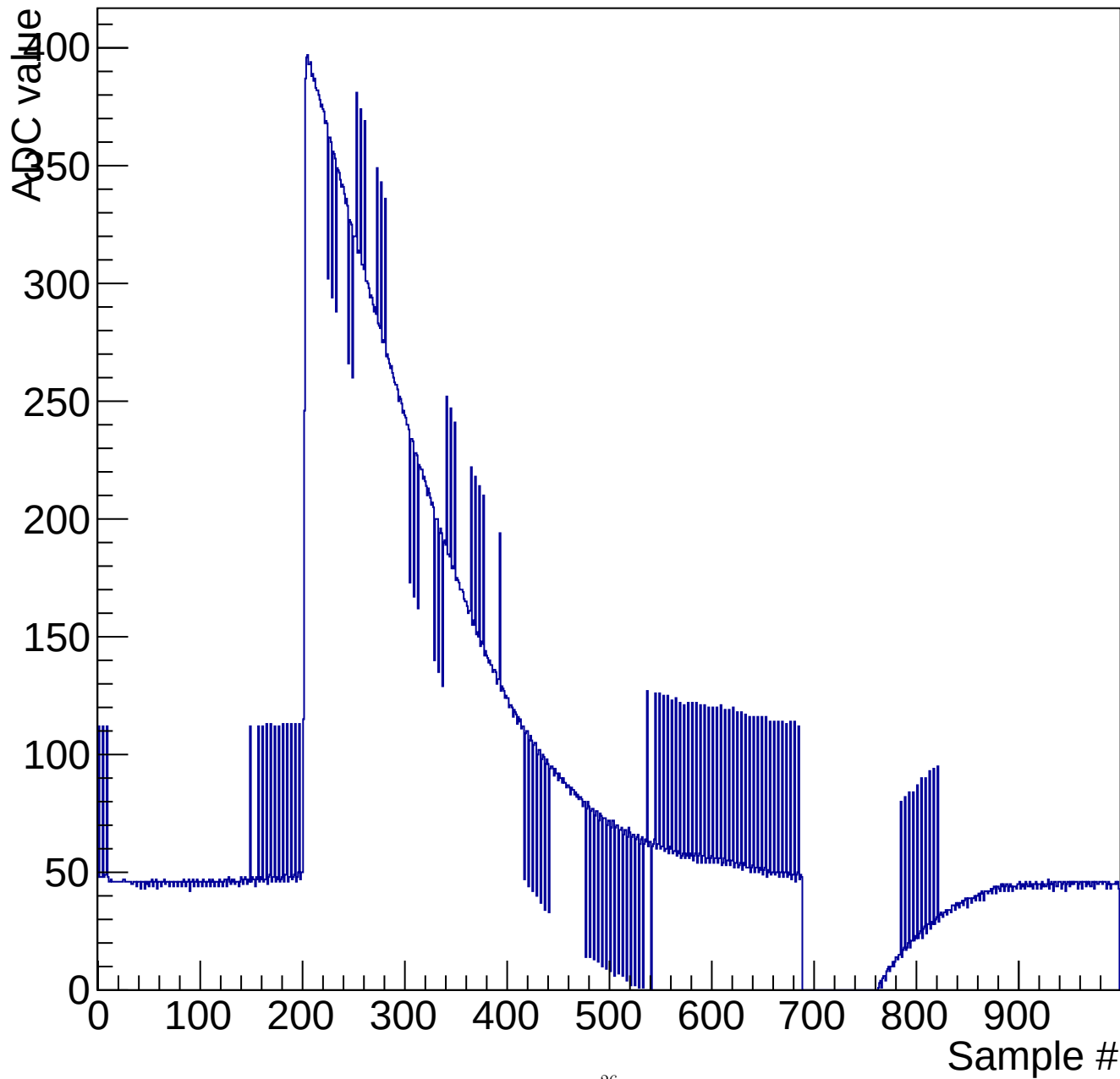
Pedestals ch 2 chip 38 run 34384 1



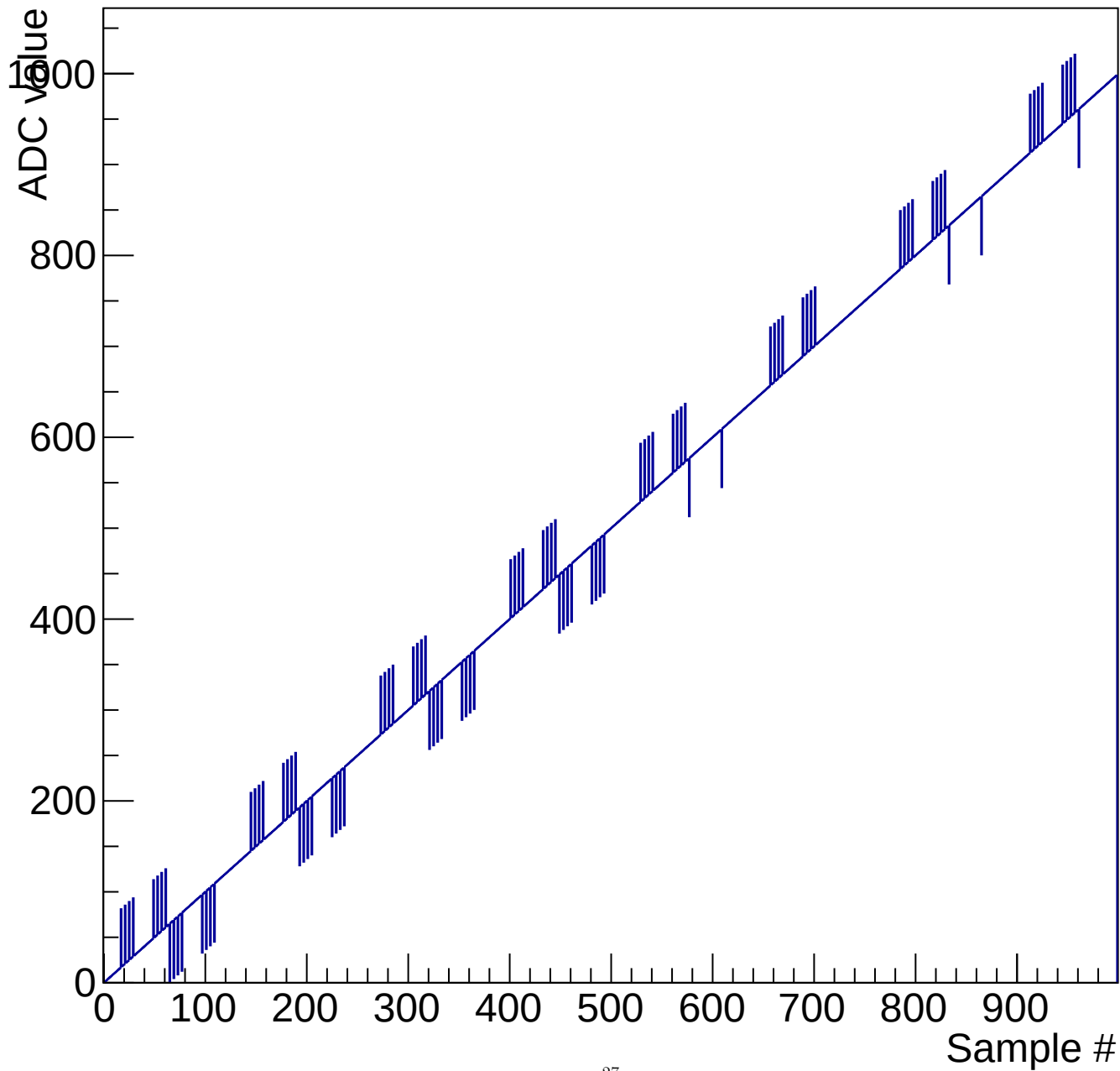
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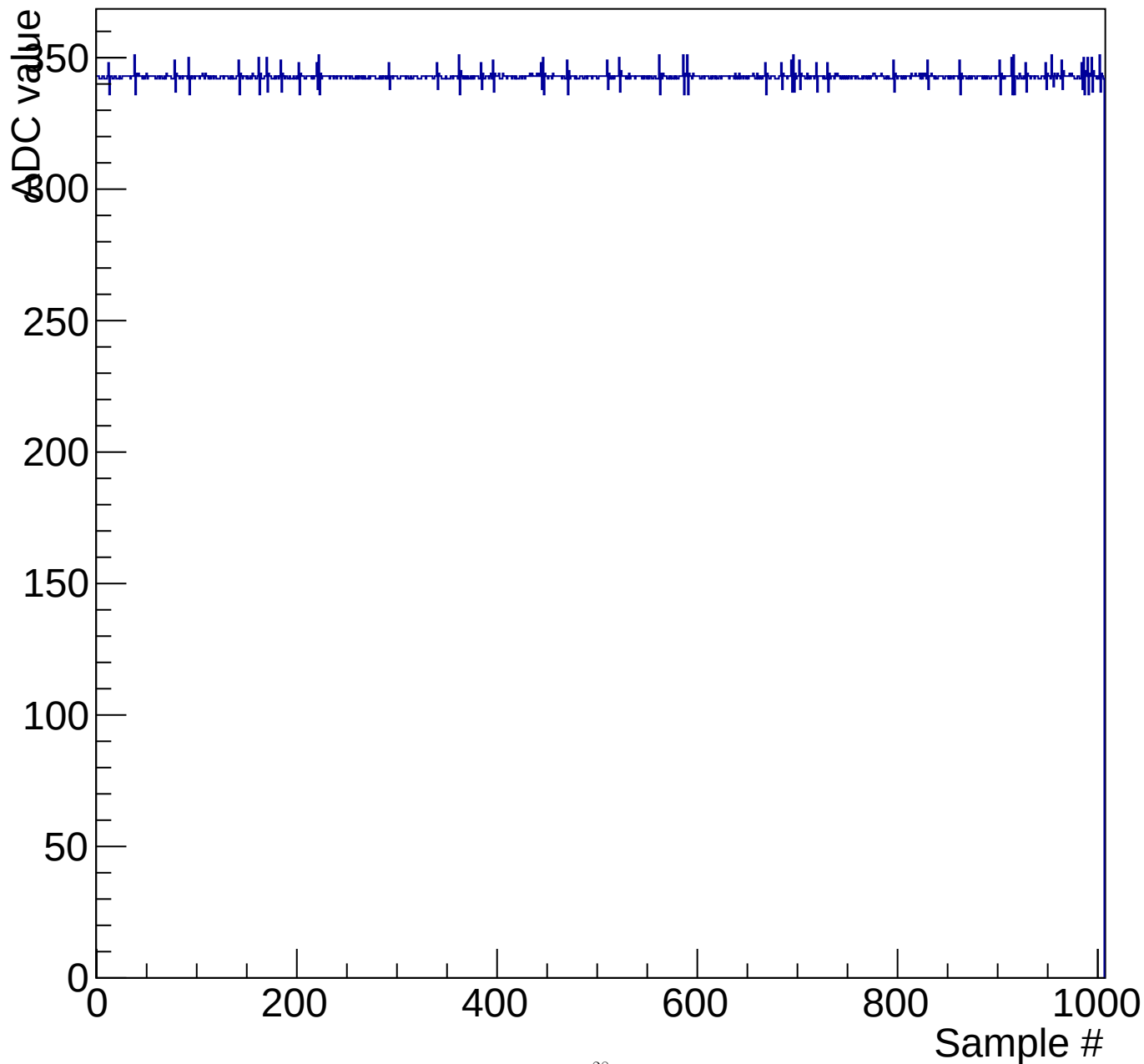
Run 34385 Event 2 Chip 38 Channel_2



Run 34386 Event 150 Chip 38 Channel_2



Run 26840 Event 5 Chip 39 Channel_7



Run 27785 Event 14 Chip 43 Channel_13

