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We have tested two batches (batch 1 with 34 and batch 2 with 50 chips) of Novapack packaged chips. Two test setups have been used, the CERN testboard which was used to characterize the chip, and the socketmcm board developed in Lund.

Test of batch 1 on CERN testboard and LUND socketmcm.

Summary of test results:

Four chips have no connection with the ball when measuring over the protection diode with respect to ground. One chip has a short between power and ground. Below is the result of chips with other problems.

Chip	socketmcm	cern testboard
65	ch2 high-low	ch2 high low
63	ch9 high-low	ch9 high-low
62	ch1 high-low	ch1 high-low
61	OK	OK
60	ch11 high-low	ch11 high-low
57	ch12 high low (weak)	ch1 bit error(?)
55	ch15 bit error, also ramp	ch15 bit error, also ramp
52	ch9 high-low	ch9 bit error, high-low weak
40	ch14 bit error?	Chip not working, readout errors.
38	ch2 bit error, also ramp	ch2 bit error, also ramp. Ch4 suspect.

All other chips and channels seems OK. Chip 61 was tested on both setups as a “good” reference chip. *High-low* means that the time samples in pedestals show the pattern: low, high, low, high, low, etc. i.e. every second time slice has a high value, every second time slice has a low value.

Ramp means that data was written into the pedestal memory and was used as data.

Pulse is a capacitive coupled square pulse on the inputs to the chip. I.e there is in the plots with a pulse sometimes a positive going pulse, from the rising edge, and a negative going pulse, from the falling edge.

Software trigger was used. 20 MHz sampling. Did also try auxiliary clock on some chips. No change.

Nominal reference voltages (V):

	CERN testboard	LUND socketmcm
refp	1.365	1.25
refn	0.276	0.25
vcm	0.819	0.75
cmout	0.819	0.75

Below are summary plots. They show pedestals, time sweeps for the faulty channels and for various settings and pulsing. All to illustrate the particular problem.

Nominal setting was gain=12mV/fC (lowest), shaping time = 120 ns, polarity=1.

The other possible gains are: 15, 19, 27 mV/fC

Ch=channel.

Preampmode = the shaper is not used. This was used to be able to get a pulse with long tail

to get the full ADC scale in one event.
Ramp = pedestal memory used as data, 0-1000.

Note that channel 0 is noisy with the CERN testboard, this is not seen with the LUND socketmcm. This is probably noise problem in the setup with the CERN testboard.

Page 4-7 CHIP 63 (CERN testboard)

pedestals for all channels
pedestals for channel 9
time sweep of a pedestal event for channel 9
time sweep for an event with a pulse input, highest gain (27 mV/fC) and preampmode for channel 9

Page 8-12 CHIP 62 (CERN testboard)

pedestals for all channels
pedestals for channel 1
time sweep of a pedestal event channel 1, zoomed to show time samples 100 to 200.
time sweep of a pedestal event channel 1, with all 1000 time samples.
time sweep for event with a pulse, highest gain (27mV/fC) and preampmode for channel 1:
→ The high low is seen both at large and small ADC value, for the central ADC values it is not seen.

Page 13-15 CHIP 60 (CERN testboard)

pedestals for all channels
time sweep in preampmode and second highest gain (15mV/fC) for channel 11.
time sweep for event with a pulse input, highest gain (27mV/fC) and preampmode for channel 11.
Using different gains show that is not gain dependent.

Page 16-17 CHIP 57 (CERN testboard)

pedestals for all channels
pedestals channel 1: sometimes a bit (=512) is set. Not seen on Lund socketmcm.

Page 18-20 CHIP 55 (CERN testboard)

pedestals for channel 15: There is a second peak about 256 higher than the first peak.
time sweep for event with a pulse, highest gain (27mV/fC) and preampmode for channel 15.
Note the positive and negative going pulses are from induced signals of an incoming square pulse.
Time sweep for a ramp (auxiliary clock) channel 15. It should be a straight line 0-1000.
Clearly bit error.

Page 21-23 CHIP 52 (CERN testboard)

time sweep for event with a pulse, highest gain (27 mV/fC) and preampmode for channel 8. All good.
time sweep for event with a pulse, highest gain (27 mV/fC) and preampmode for channel 9. (high pulse height) Some spikes.
time sweep for event with a pulse, highest gain and preampmode for channel 9. (low pulse height)
Some spikes are seen.

CHIP 40 (CERN testboard)

Readout errors, not possible to read.
Not further investigated yet.
No plot.

Page 24-27 CHIP 38 (CERN testboard)

pedestals for highest gain ((27mV/fC) and preampmode for channel 2. There are two peaks with a difference of 64.

time sweep for pedestal event with highest gain (27 mV/fC) and preampmode for channel 2. Some spikes.

time sweep for event with a pulse, highest gain (27 mV/fC) and preampmode for channel 2. Some spikes.

time sweep for event with ramp data from pedestal memory for channel 2. Some spikes.

Should be a straight line 0-1000.

Test of batch 2 on LUND socketmcm

None of the above problems was seen. Summary:

Chip 16: Register test OK, do not get any events.

Chip 30: short between ground and iopower.

Chip 31: no connection with any pin (as measured over protection diode).

Chip 75: draw less current (0.36A expect 0.47A). Register test fails.

Page 28: Some chips are “noisy” for some settings (in preampmode)

Page 29: Some channels have some bit missing (also when using pedestal memory as data), always at time slice 504 for the channel shown.