

Data taken with no shaper and the decay = 0.9V in order to see the long tail of a pulse and to study if there is a problem with higher bits and ADC values. Previous plots in plots-20171130.pdf show plots for this. There is a hint that the “high-low” problem may be a function of ADC value. Here we have tried to understand if there is any change in behaviour that depends on ADC value. To do this are the values of the “bad” channel subtracted with the values from a “good” channel from the same event (they should see the “same” pulse) sample by sample. Ideally should all be a flat distribution.

Plot1:

Chip 52 with channel 9 with “high-low problem” subtracted with channel 0.

Plot2:

Same as Plot1 but expanded around 550-950. Two observations: one is that the tails of channel 9 and 0 are different, ideally should it be a flat distribution. Second, there is a structure that the “high-low” is not there for all ADC values.

Plot3: Same as plot 1 for a different event.

Plot4 and 5: Same as Plot1 and 2 but for a different event.

Plot6: Chip number 65, channel 0 (“good”).

Plot7: Chip number 65, channel 2 (“high-low”). At ADC values around 500 is the “high-low” less pronounced?

Plot8: Difference chip 65 channel 2 – channel 0.

Plot9: Chip 33 channel 8 – channel 0. Considered to be good channels in good chip.

Study of ADC distributions.

Plot10: For protomcm with qfp packet.

Plot11: Chip 65 channel 0, considered as “good” channel. A clear dip is at 701 and 702.

Plot12: Looking at single pulses show that there is a small structure at these ADC values.

Plot 13: Chip 52 channel 9. Many dips here and there.

Grounding studies

All digital grounds was connected (as was done before). Many corrupted events (ca 1%), mainly the channel length was wrong. The first word should contain length; the length is either a pedestal value, then also the channel number is a pedestal value; or 0x2AA (ALTRO padding pattern) which is followed by correct length and channel number. Not studied in detail.

Connected analog and digital grounds. Number of corrupted events decreased to a few permille, after some time did they disappear?! No change to “high-low” problem.

Reference voltages

on chip:

Refp1 – refp2: 0 ohm

refn1 – refn2: 0 ohm

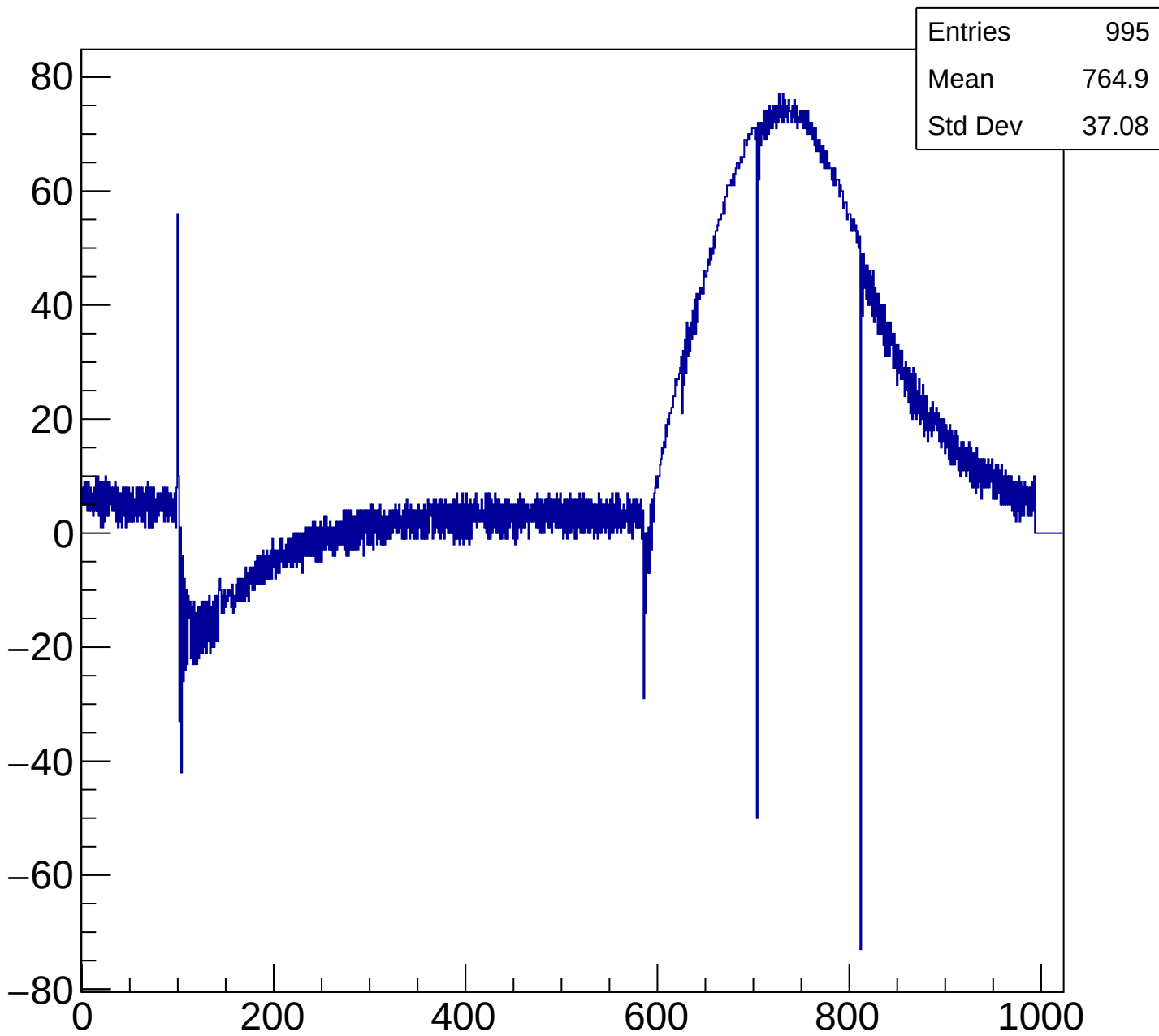
incm1 – incm2: 0 Ohm

outcm1 – outcm2: 200 Ohm

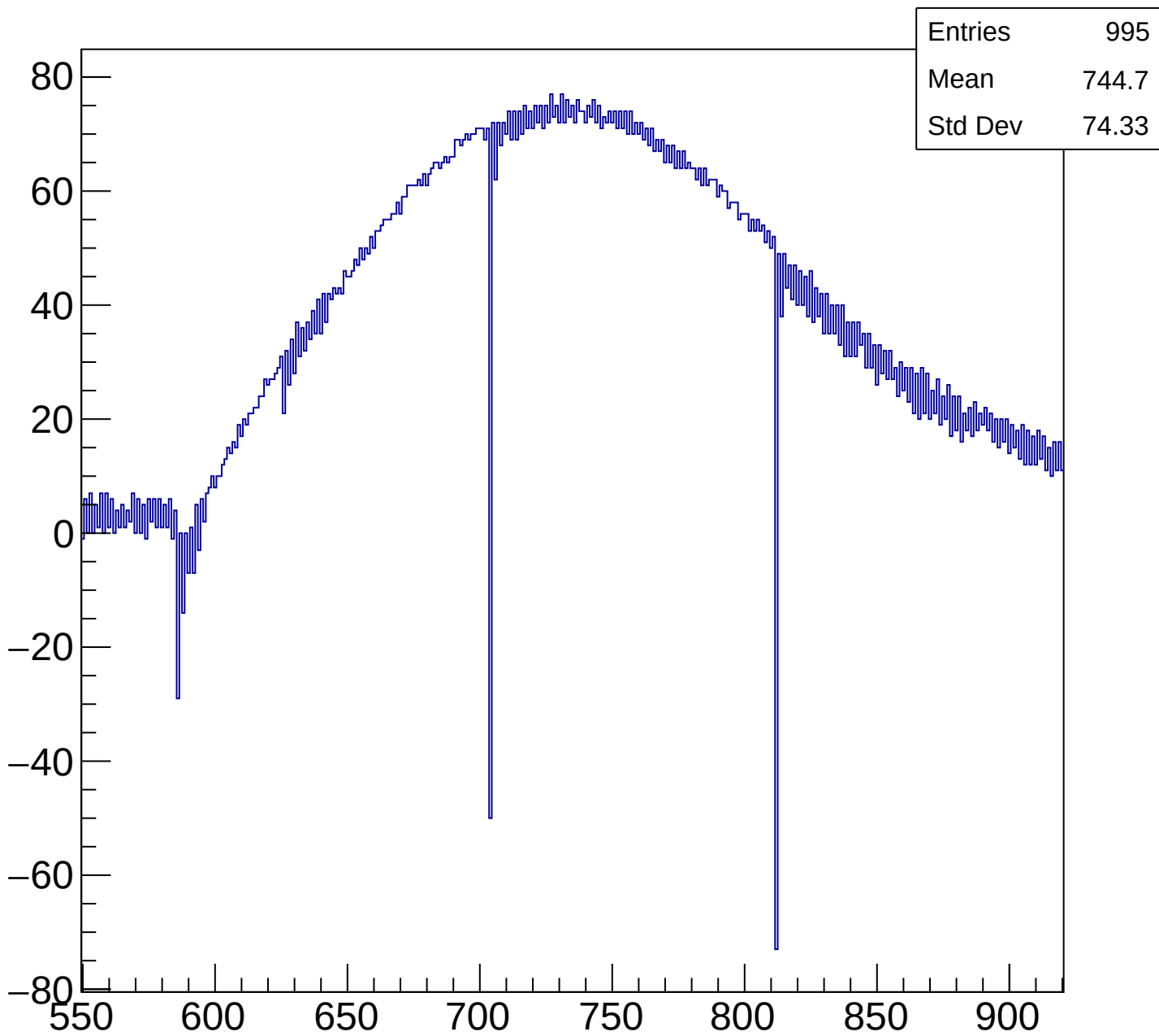
on socketmcm:

contact from testpoint to footprint of socket: OK

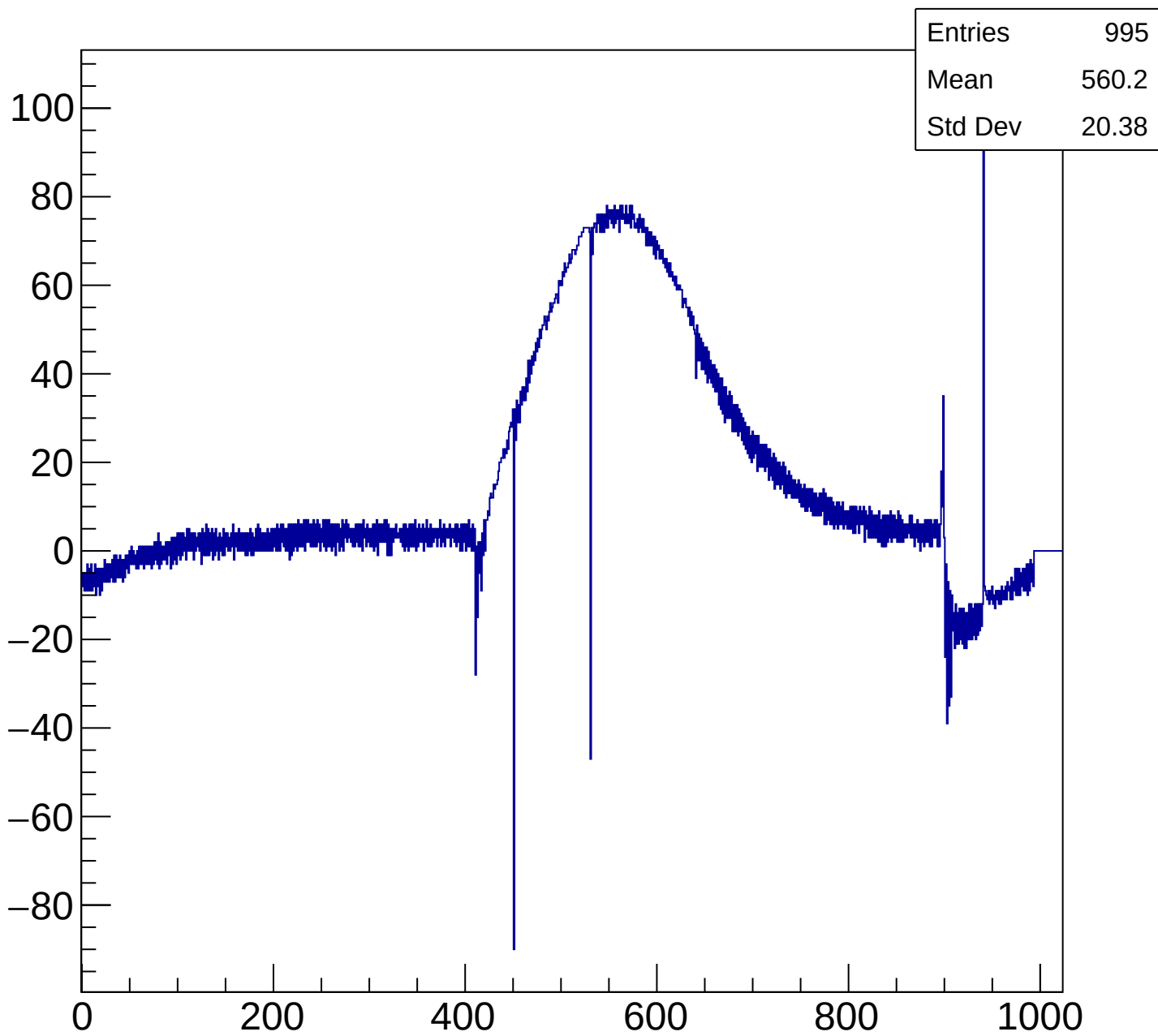
Run 20646 Event 11 Chip 52 Channel_9



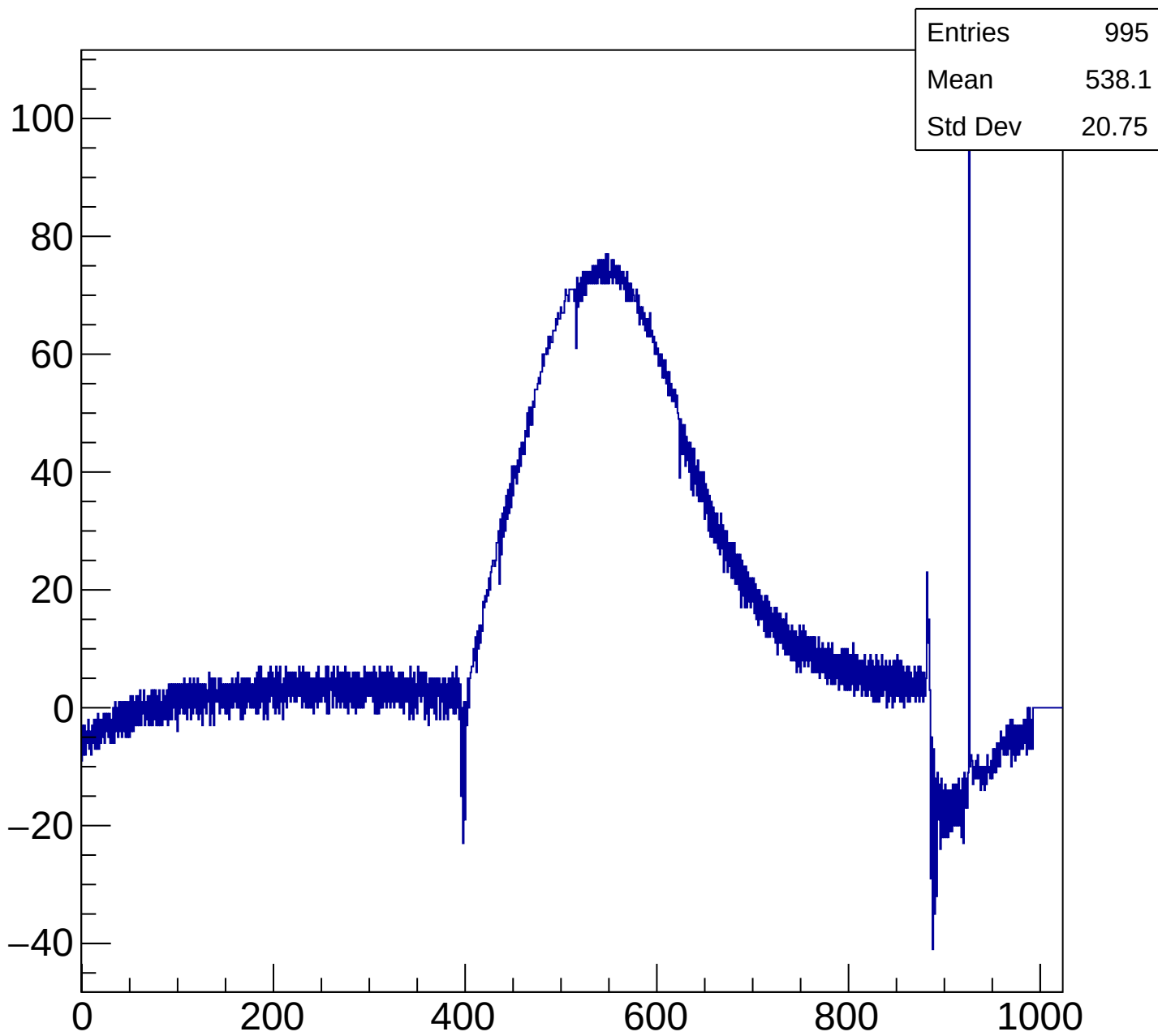
Run 20646 Event 11 Chip 52 Channel_9



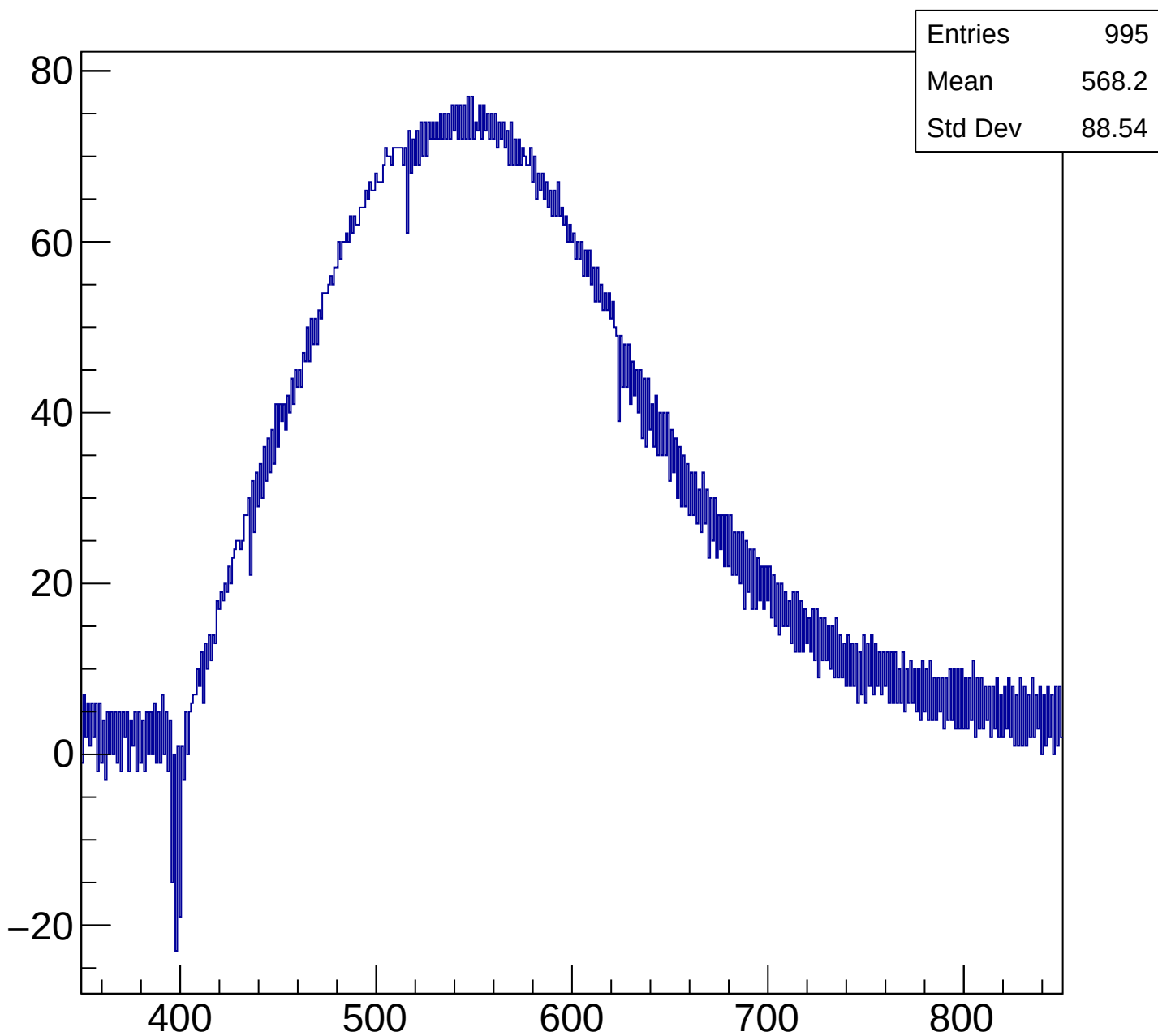
Run 20646 Event 12 Chip 52 Channel_9



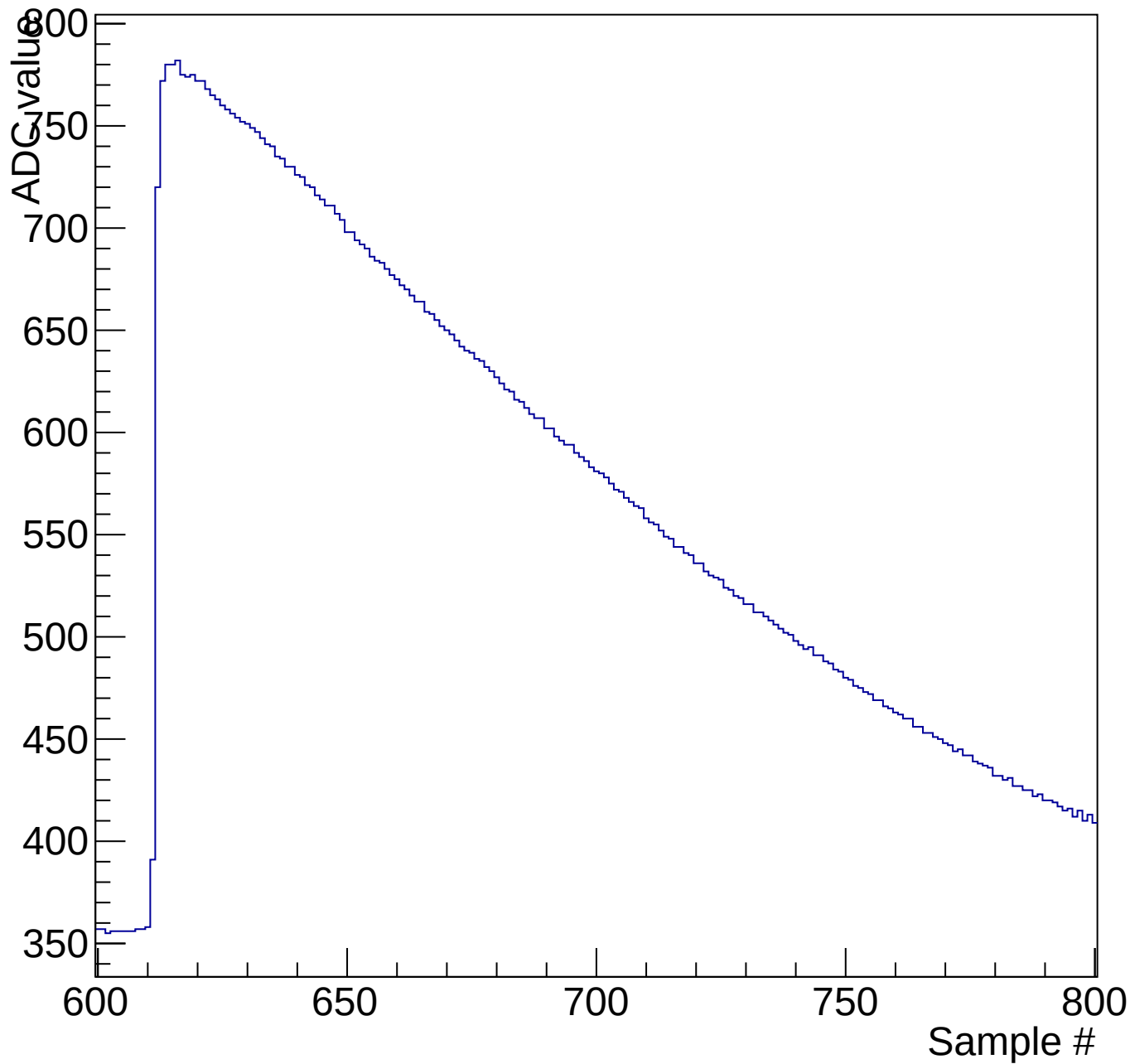
Run 20646 Event 13 Chip 52 Channel_9



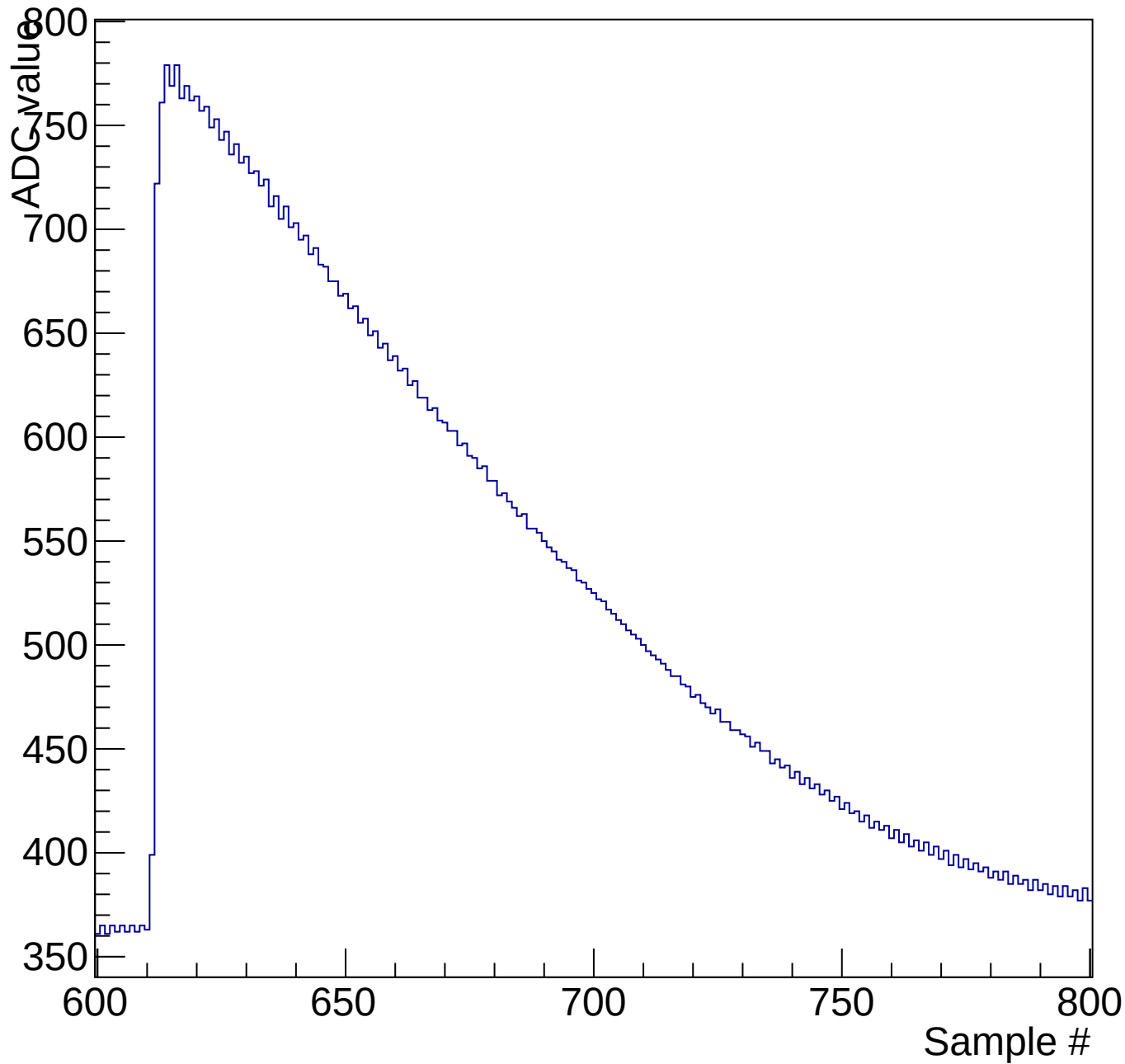
Run 20646 Event 13 Chip 52 Channel_9



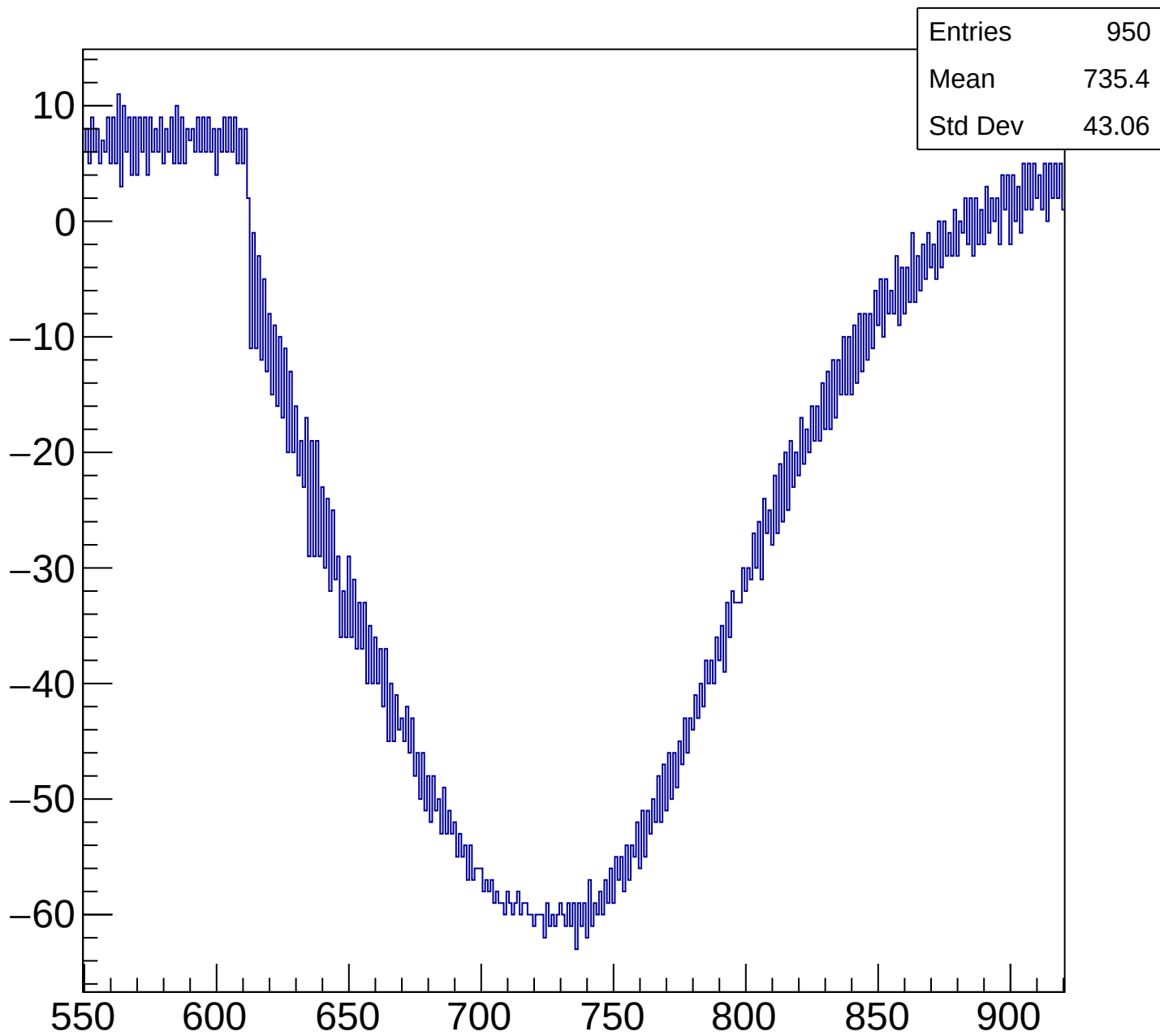
Run 21035 Event 4 Chip 65 Channel_0



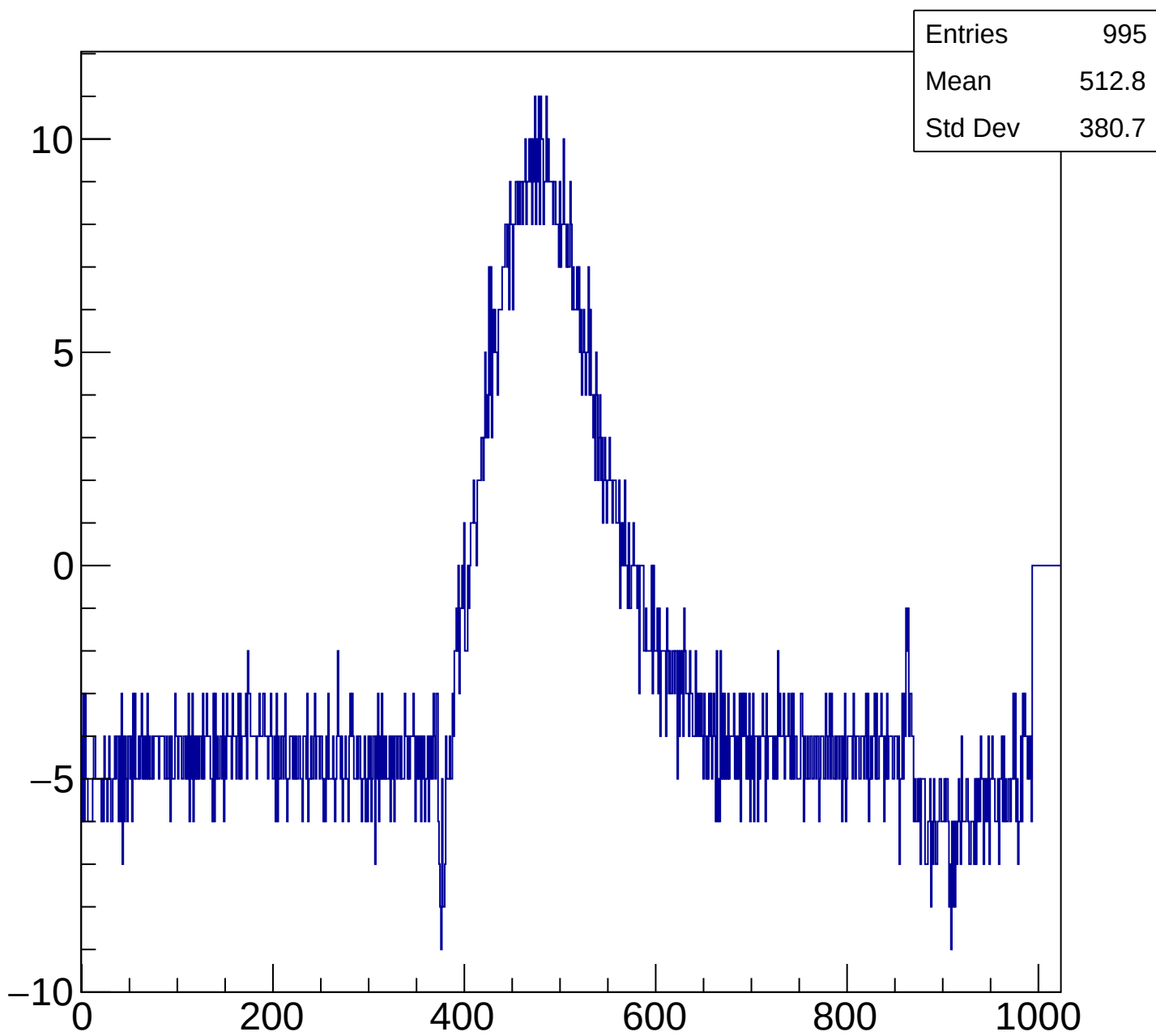
Run 21035 Event 4 Chip 65 Channel_2



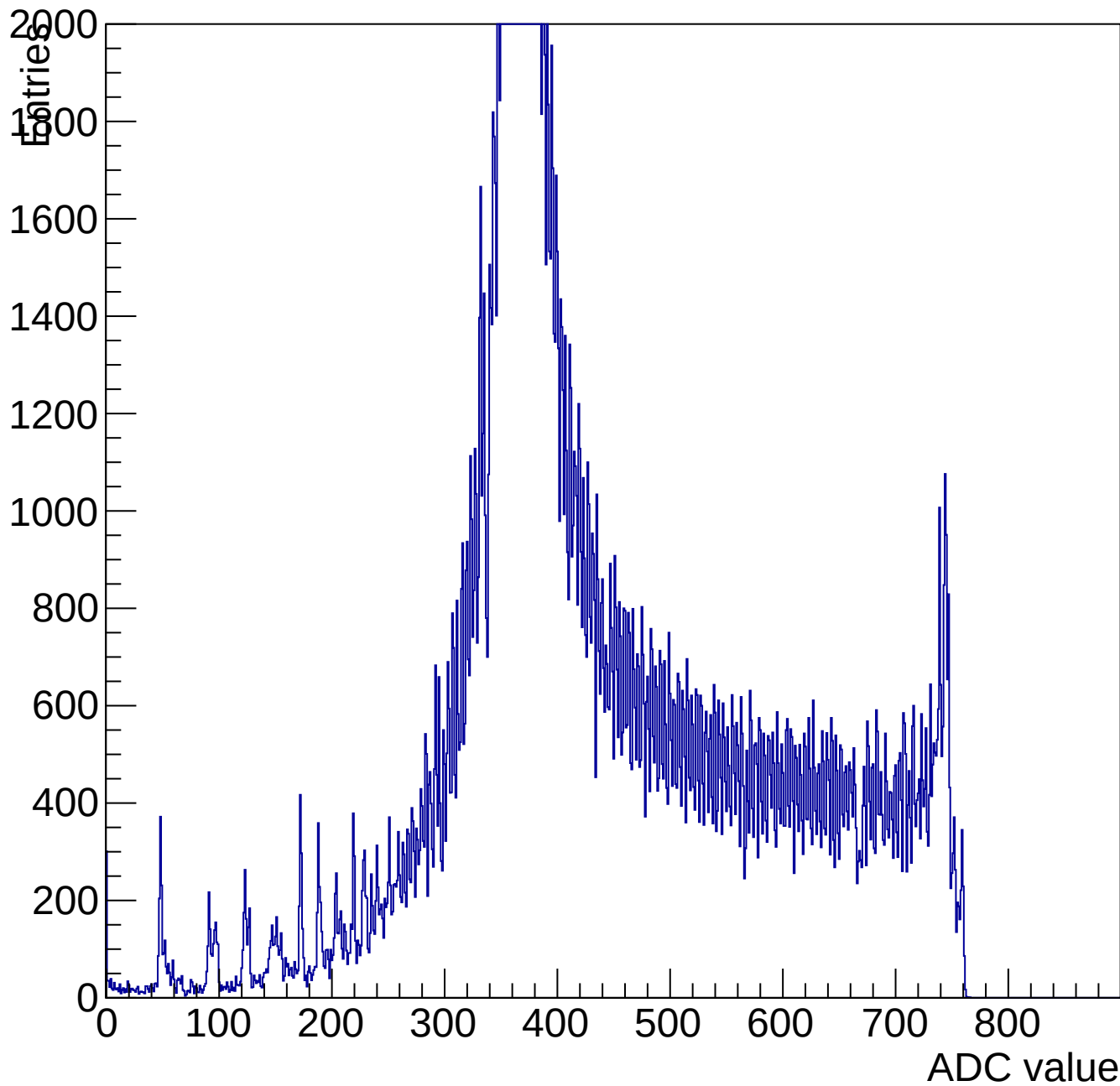
Run 21035 Event 4 Chip 65 Channel_2



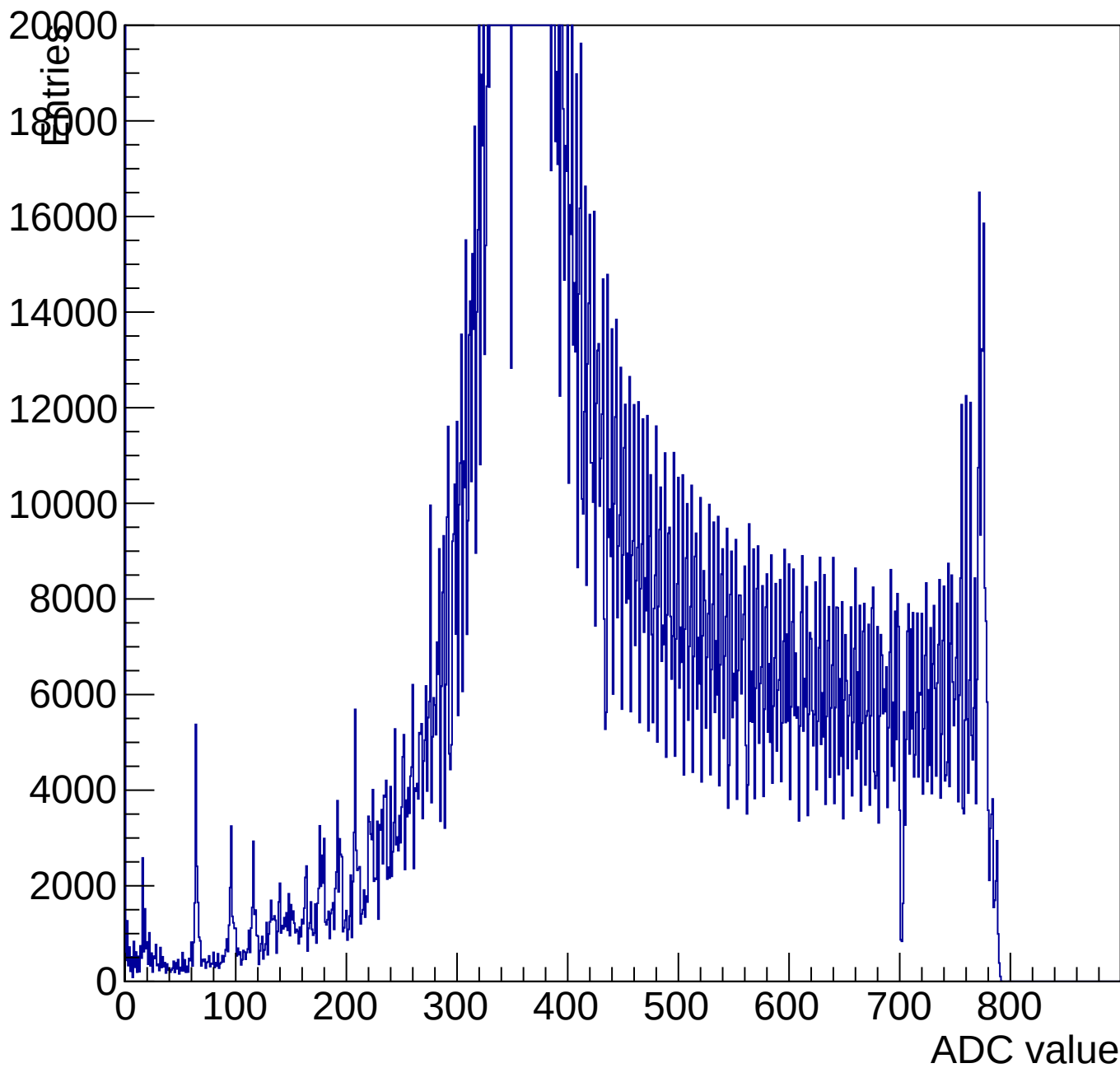
Run 20834 Event 1 Chip 33 Channel_8



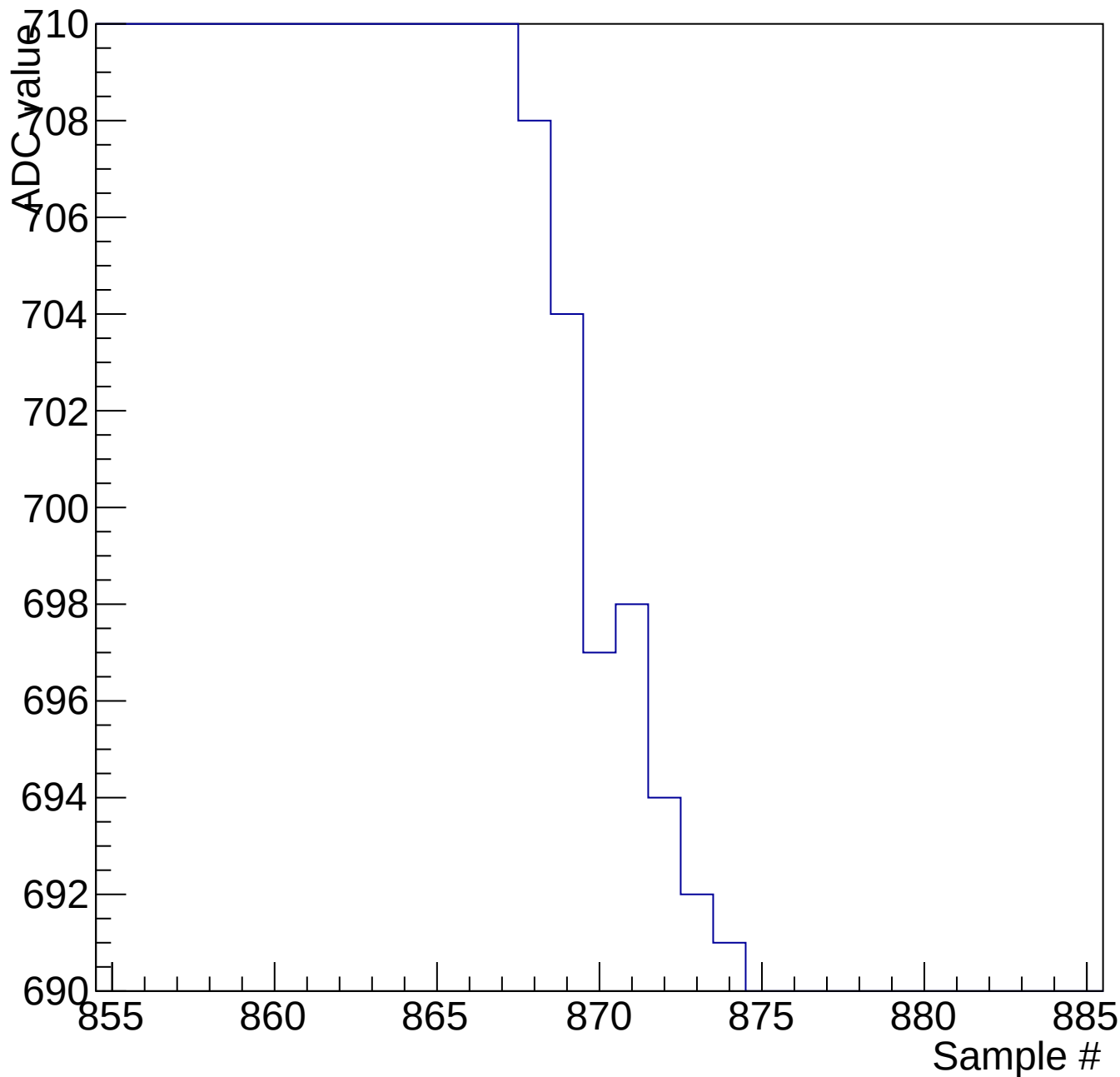
Pulse height ch 0 chip 36 runnb 20859



Pulse height ch 0 chip 65 runnb 21035



Run 21035 Event 35 Chip 65 Channel_0



Pulse height ch 9 chip 52 runnb 20646

