

20180313

This test is with Novapack packaged chip 65 on CERN testboard.
Chip 65 had in previous test high-low problem in channel 2.

Software trigger.
20 MHz sampling.

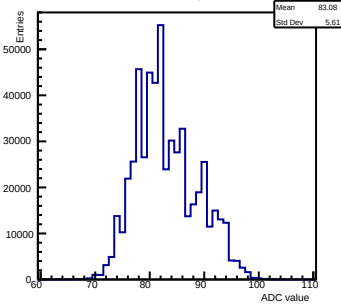
Plot 1: pedestals.
Nominal settings (low gain, long shaping, no preampmode)
Channel 0: very noisy. This was also the case for PGA package 2 tested 20180306.
Channel 2: two peaks in pedestal.

Plot 2: time sweep for a single event for channel 2. No pulse in.
High-low clearly seen.
There is no sign of a trigger pickup in this plot.

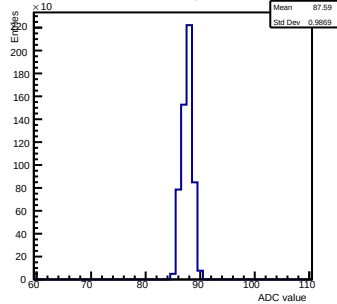
Plot 3: time sweep for a single event for channel 2. Pulse in.
Preampmode, gain is set to highest. This will give values in almost full ADC range.
One can see high-low is seen at high ADC values, then gone at around 600, and then appear in lower ADC values.

Conclusion about chip 65: Same behaviour in the test with CERN testboard as for socketmcm test.

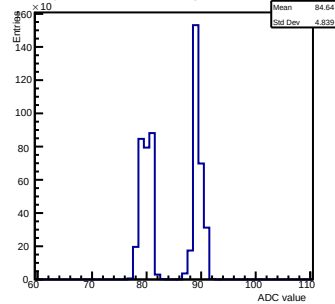
Pedestals ch 0 chip 65 tbnom



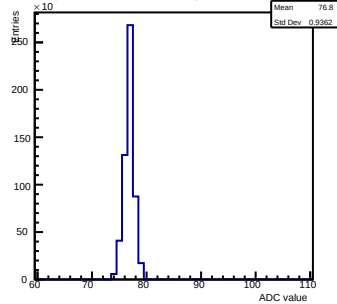
Pedestals ch 1 chip 65 tbnom



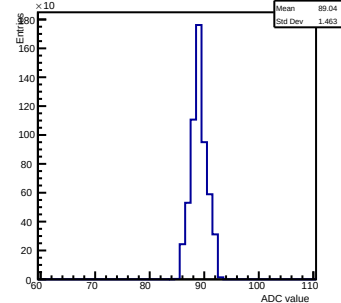
Pedestals ch 2 chip 65 tbnom



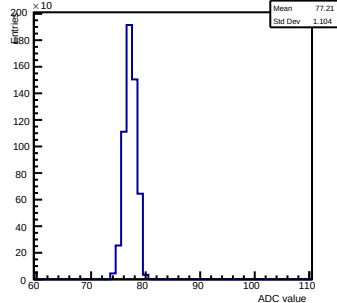
Pedestals ch 3 chip 65 tbnom



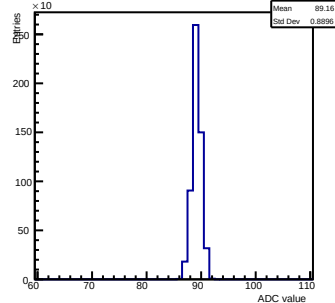
Pedestals ch 4 chip 65 tbnom



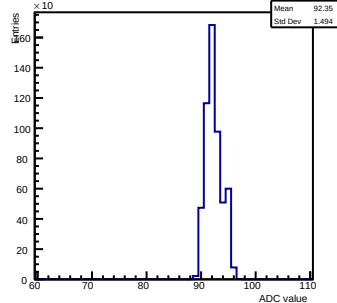
Pedestals ch 5 chip 65 tbnom



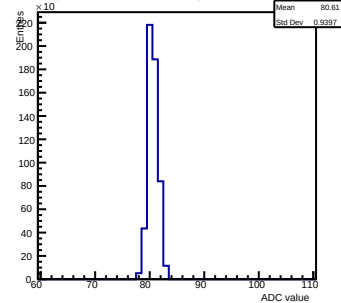
Pedestals ch 6 chip 65 tbnom



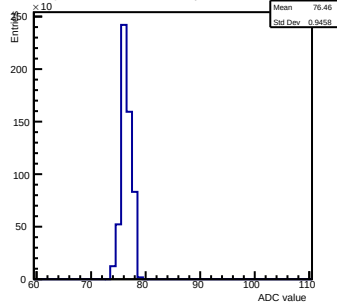
Pedestals ch 7 chip 65 tbnom



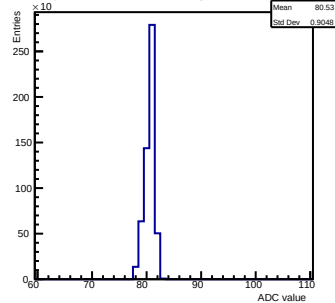
Pedestals ch 8 chip 65 tbnom



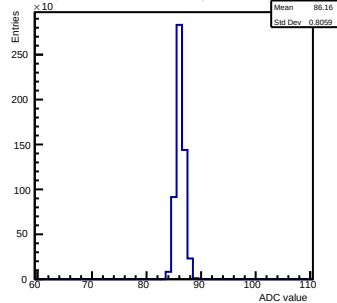
Pedestals ch 9 chip 65 tbnom



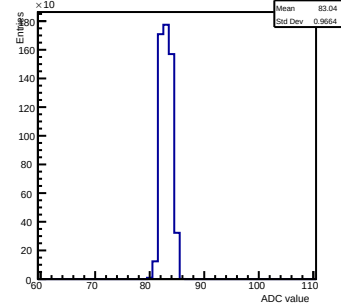
Pedestals ch 10 chip 65 tbnom



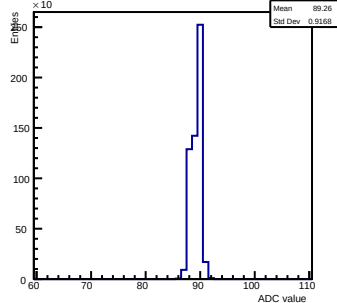
Pedestals ch 11 chip 65 tbnom



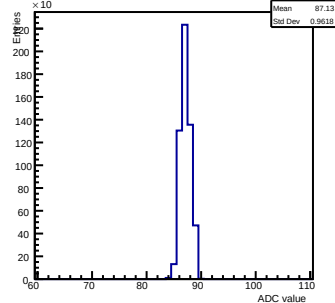
Pedestals ch 12 chip 65 tbnom



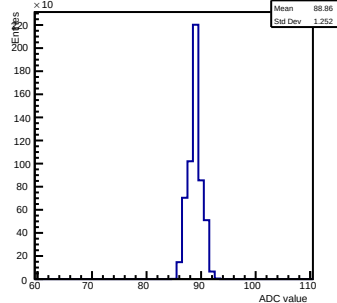
Pedestals ch 13 chip 65 tbnom



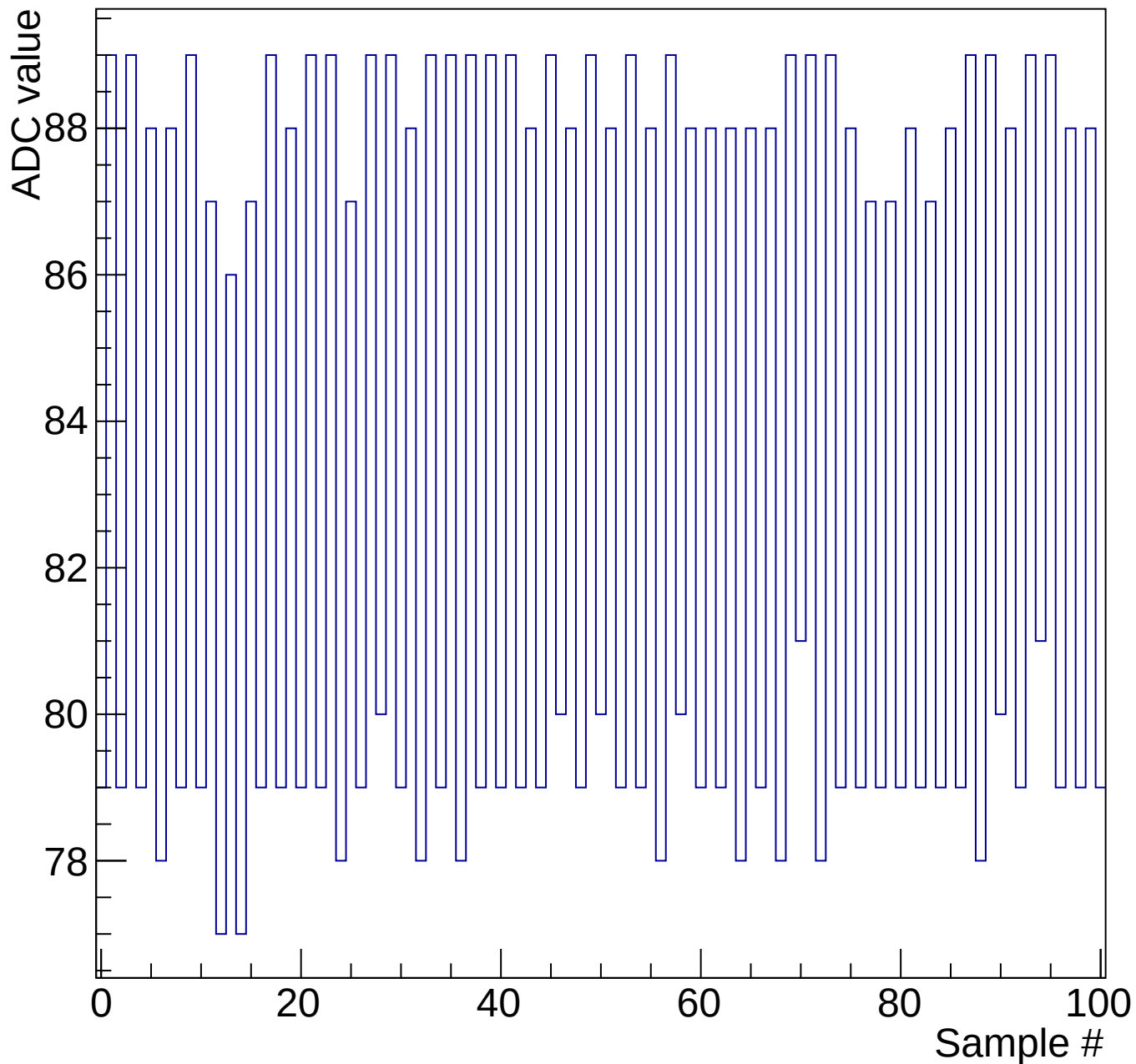
Pedestals ch 14 chip 65 tbnom



Pedestals ch 15 chip 65 tbnom



Run 34320 Event 1 Chip 65 Channel_2



Run 34325 Event 962 Chip 65 Channel_2

