

20180319

This test is with Novapack packaged chips on CERN testboard.

Summary of test results:

Chip	socketmcm	cern testboard
65	ch2 high-low	ch2 high low (see plots-20180313)
63	ch9 high-low	ch9 high-low
62	ch1 high-low	ch1 high-low
61	OK	OK
60	ch11 high-low	ch11 high-low
57	ch12 high low (weak)	ch1 bit error(?)
55	ch15 bit error, also ramp	ch15 bit error, also ramp
52	ch9 high-low	ch9 bit error, high-low weak
40	ch14 bit error?	Chip not working, readout errors.
38	ch2 bit error, also ramp	ch2 bit error, also ramp. Ch4 suspect.

Software trigger.

20 MHz sampling. Did also try auxilliary clock on some chips. No change.

Nominal reference voltages (V):

	CERN testboard	socketmcm
refp	1.365	1.25
refn	0.276	0.25
vcm	0.819	0.75
cmout	0.819	0.75
decay	1.02	1.00

Did not measure the voltages on the CERN testboard until a few chips was tested. Could change the voltages on the CERN testboard to be the same as on the socketmcm, then one need to dismount the testboard setup to adjust the potentiometers. I doubt it will make much of a change.

Below are summary plots. They show pedestals, time sweeps for the faulty channel and for various settings and pulsing. All to illustrate the particular problem. gain3=highest gain. Ch=channel. Preampmode = shaper is not used.

Plots 1-4 CHIP 63

pedestals
pedestals ch9
time sweep pedestal ch9
time sweep pulser+gain3+preampmode ch9

Plots 5-9 CHIP 62

pedestals
pedestal ch1
time sweep detail ch1
time sweep full ch1
time sweep pulser+gain3+preampmode ch1

Plots 10-12 CHIP 60

pedestals

time sweep preamp+gain1 ch11

time sweep pulser+gain3+preampmode ch11

Plots 13-14 CHIP 57

pedestals

pedestals ch1

Plots 15-17 CHIP 55

pedestals

time sweep preamp+gain3+pulser ch15

time sweep ramp+auxclk ch15

Plots 18-20 CHIP 52

time sweep preamp+gain3+pulser ch8

time sweep preamp+gain3+pulser ch9 (high pulse)

time sweep preamp+gain3+pulser ch9 (low pulse)

Plots CHIP 40

Readout errors, not possible to read.

Not further investigated yet.

No plot.

Plots 21-24 CHIP 38

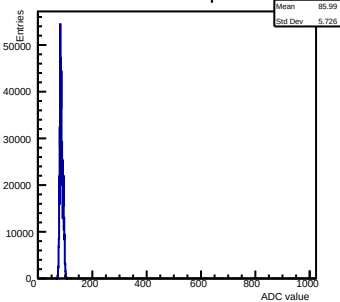
pedestal preamp+gain3 ch2

time sweep preamp+gain3 ch2

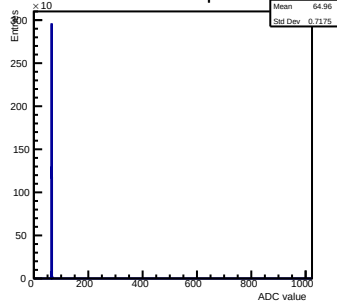
time sweep preamp+gain3+pulser ch2

time sweep ramp ch2

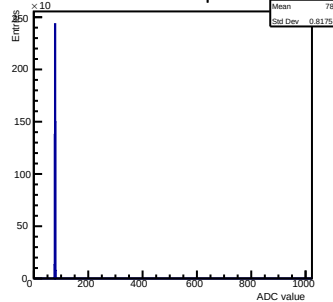
Pedestals ch 0 chip 63 nom



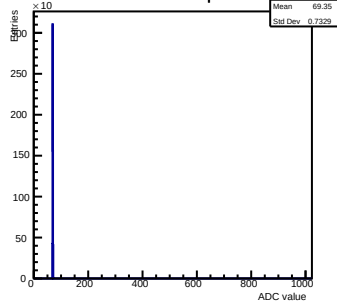
Pedestals ch 1 chip 63 nom



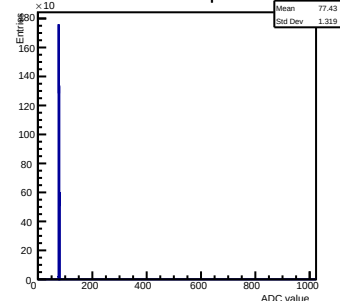
Pedestals ch 2 chip 63 nom



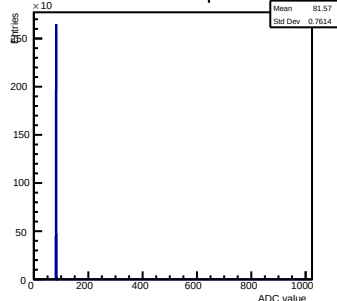
Pedestals ch 3 chip 63 nom



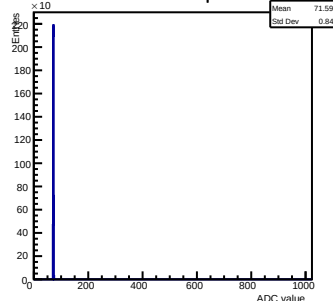
Pedestals ch 4 chip 63 nom



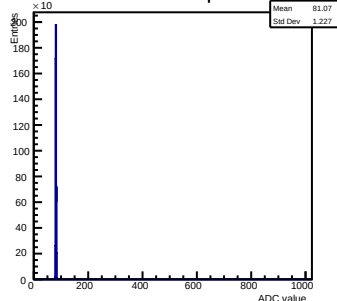
Pedestals ch 5 chip 63 nom



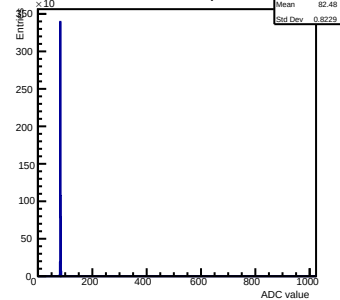
Pedestals ch 6 chip 63 nom



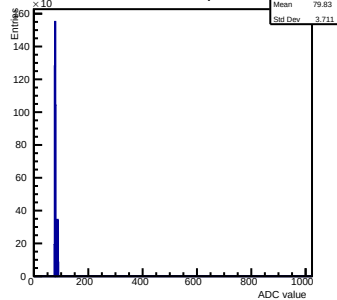
Pedestals ch 7 chip 63 nom



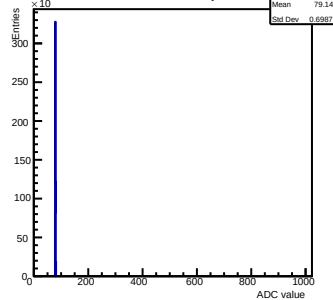
Pedestals ch 8 chip 63 nom



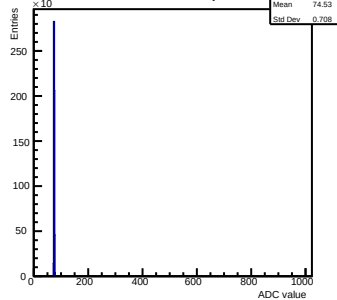
Pedestals ch 9 chip 63 nom



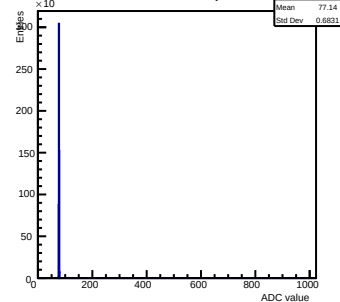
Pedestals ch 10 chip 63 nom



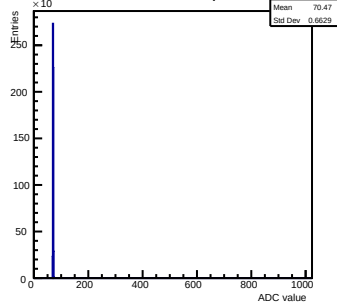
Pedestals ch 11 chip 63 nom



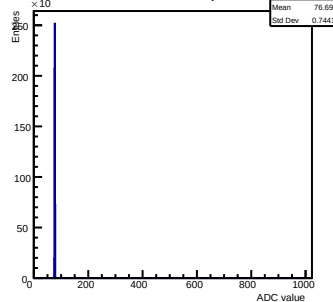
Pedestals ch 12 chip 63 nom



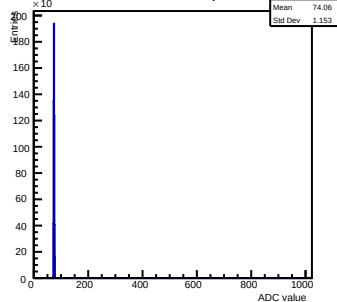
Pedestals ch 13 chip 63 nom



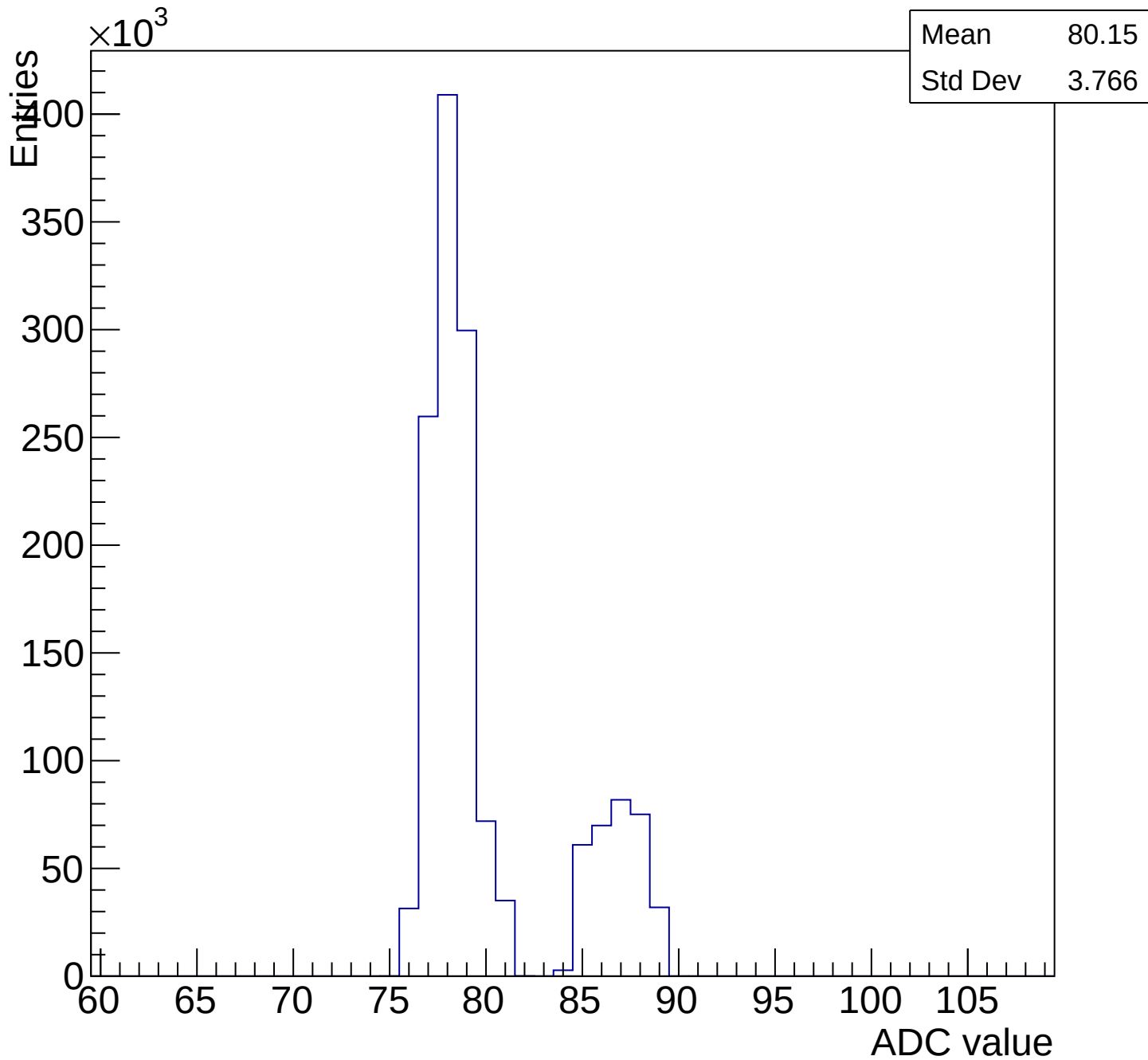
Pedestals ch 14 chip 63 nom



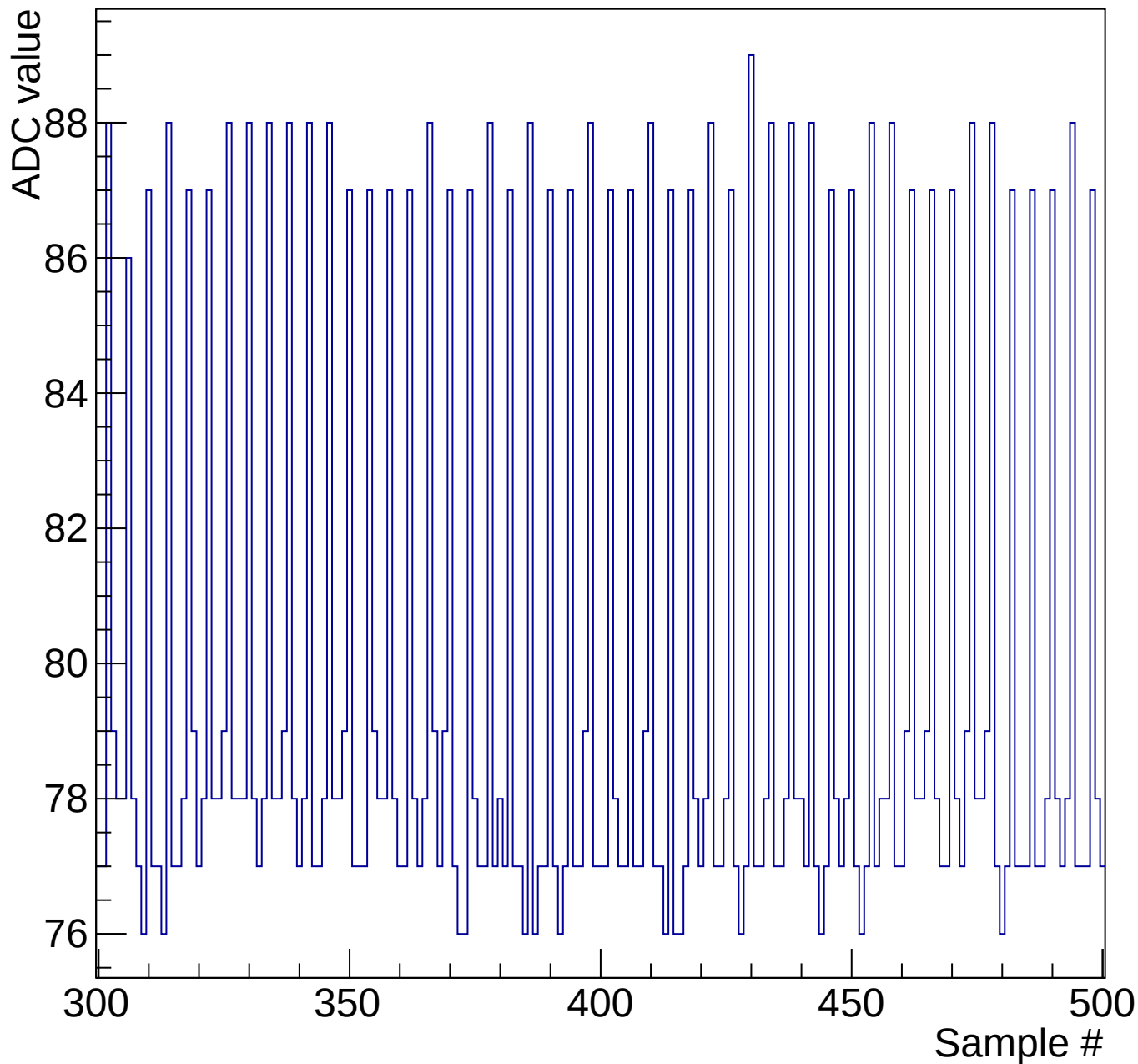
Pedestals ch 15 chip 63 nom



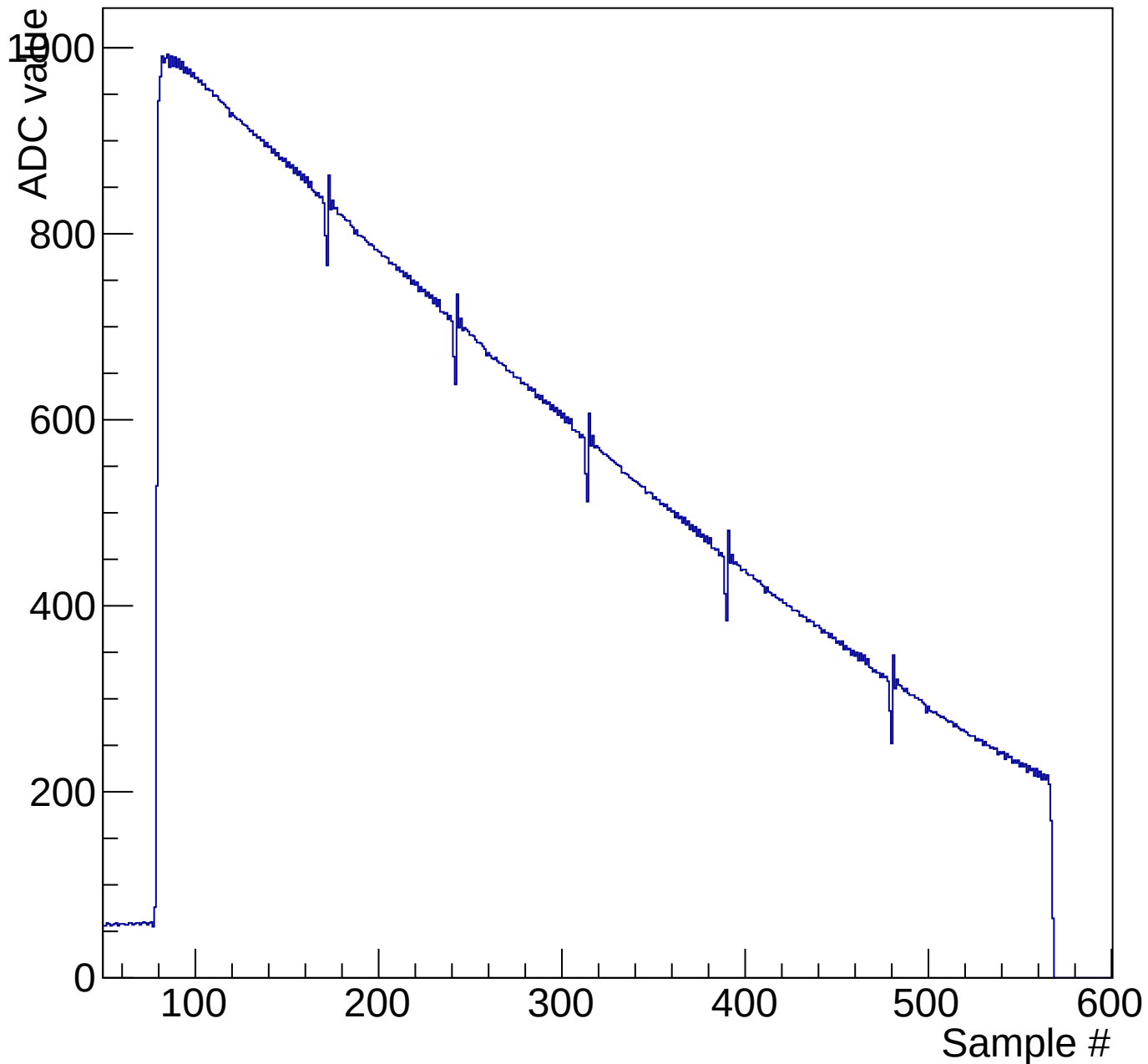
Pedestals ch 9 chip 63 run 34339 nom



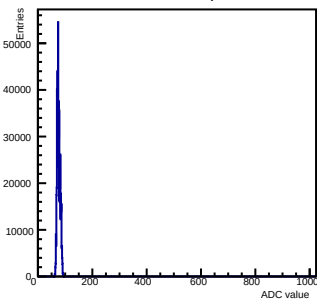
Run 34339 Event 2 Chip 63 Channel_9



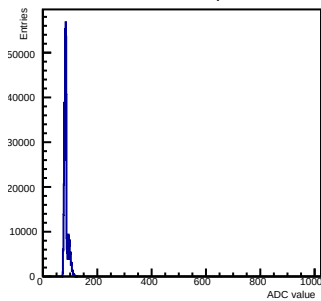
Run 34346 Event 7 Chip 63 Channel_9



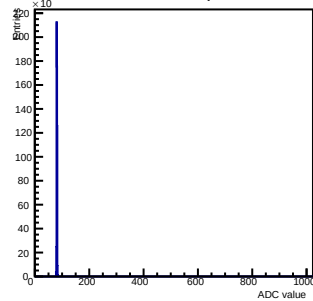
Pedestals ch 0 chip 62 nom



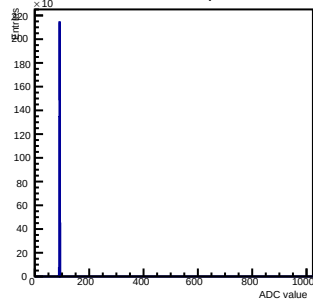
Pedestals ch 1 chip 62 nom



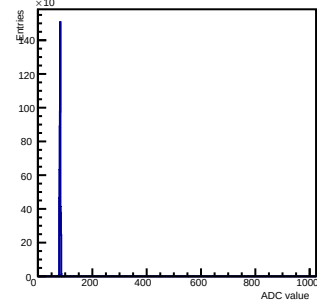
Pedestals ch 2 chip 62 nom



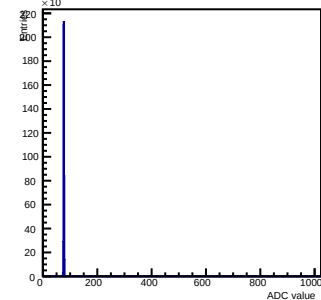
Pedestals ch 3 chip 62 nom



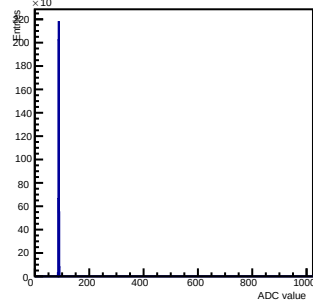
Pedestals ch 4 chip 62 nom



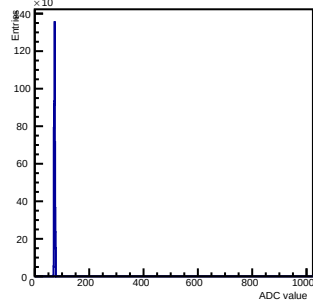
Pedestals ch 5 chip 62 nom



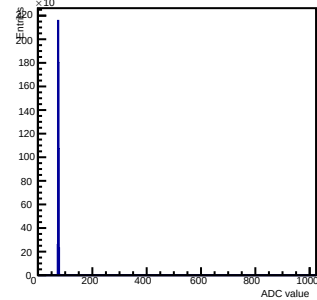
Pedestals ch 6 chip 62 nom



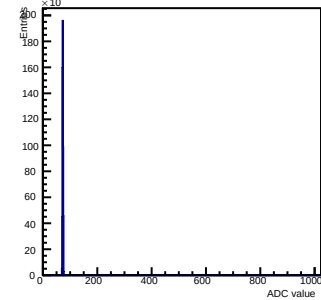
Pedestals ch 7 chip 62 nom



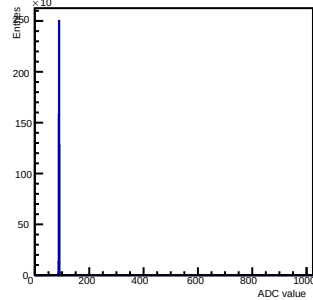
Pedestals ch 8 chip 62 nom



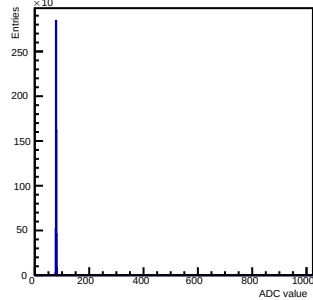
Pedestals ch 9 chip 62 nom



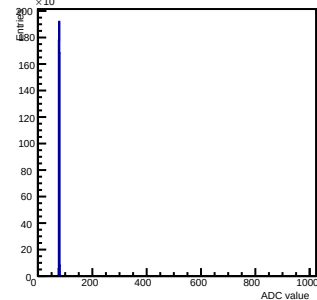
Pedestals ch 10 chip 62 nom



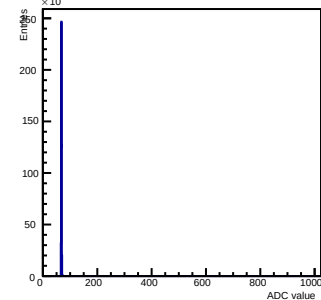
Pedestals ch 11 chip 62 nom



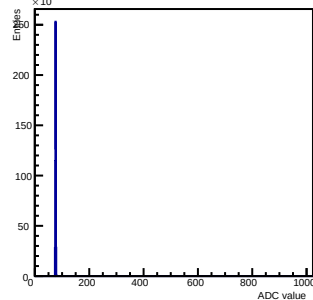
Pedestals ch 12 chip 62 nom



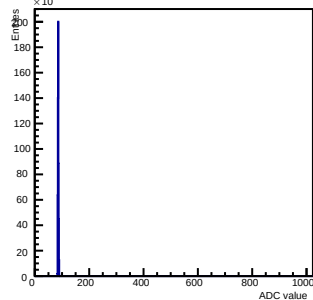
Pedestals ch 13 chip 62 nom



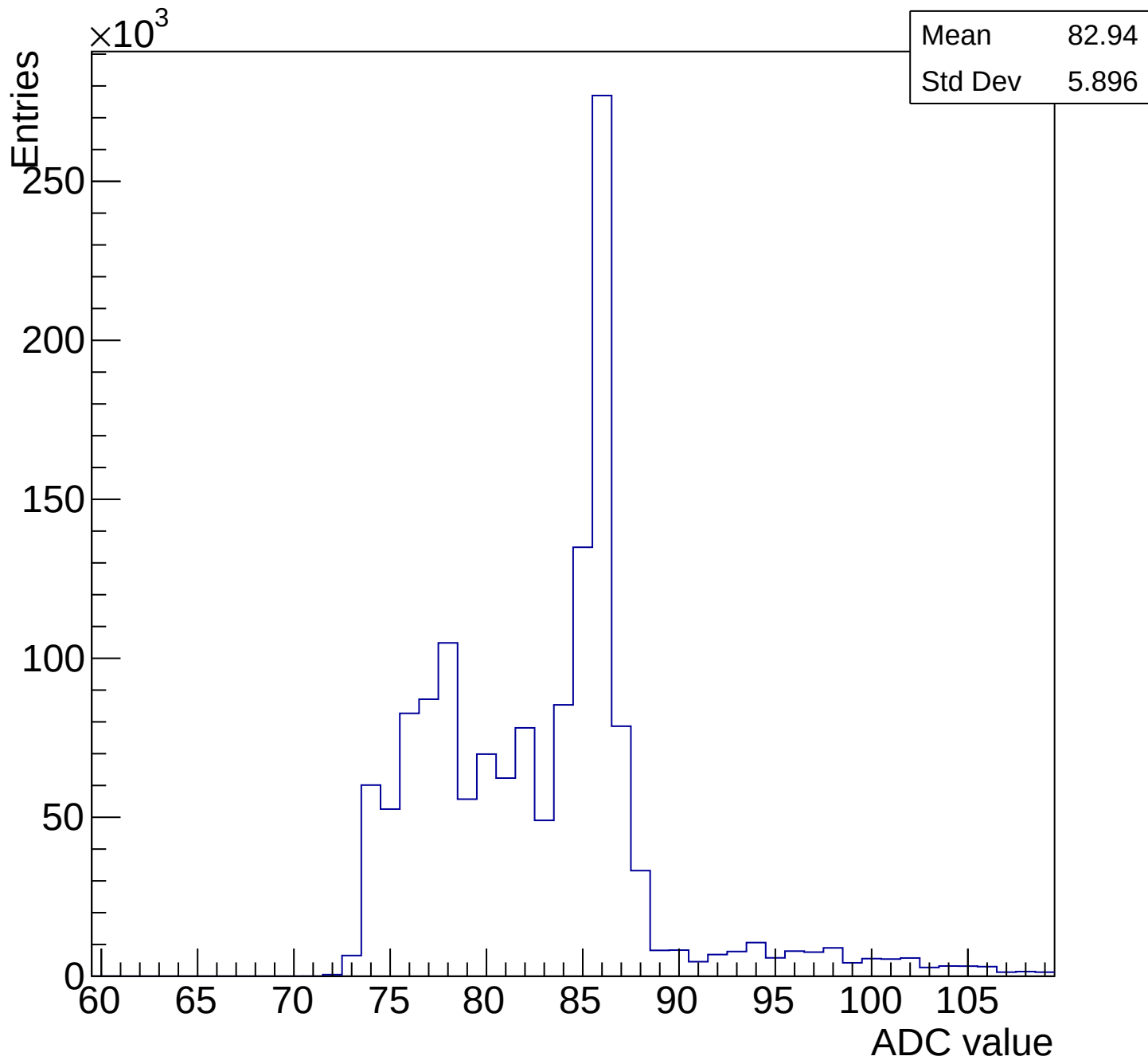
Pedestals ch 14 chip 62 nom



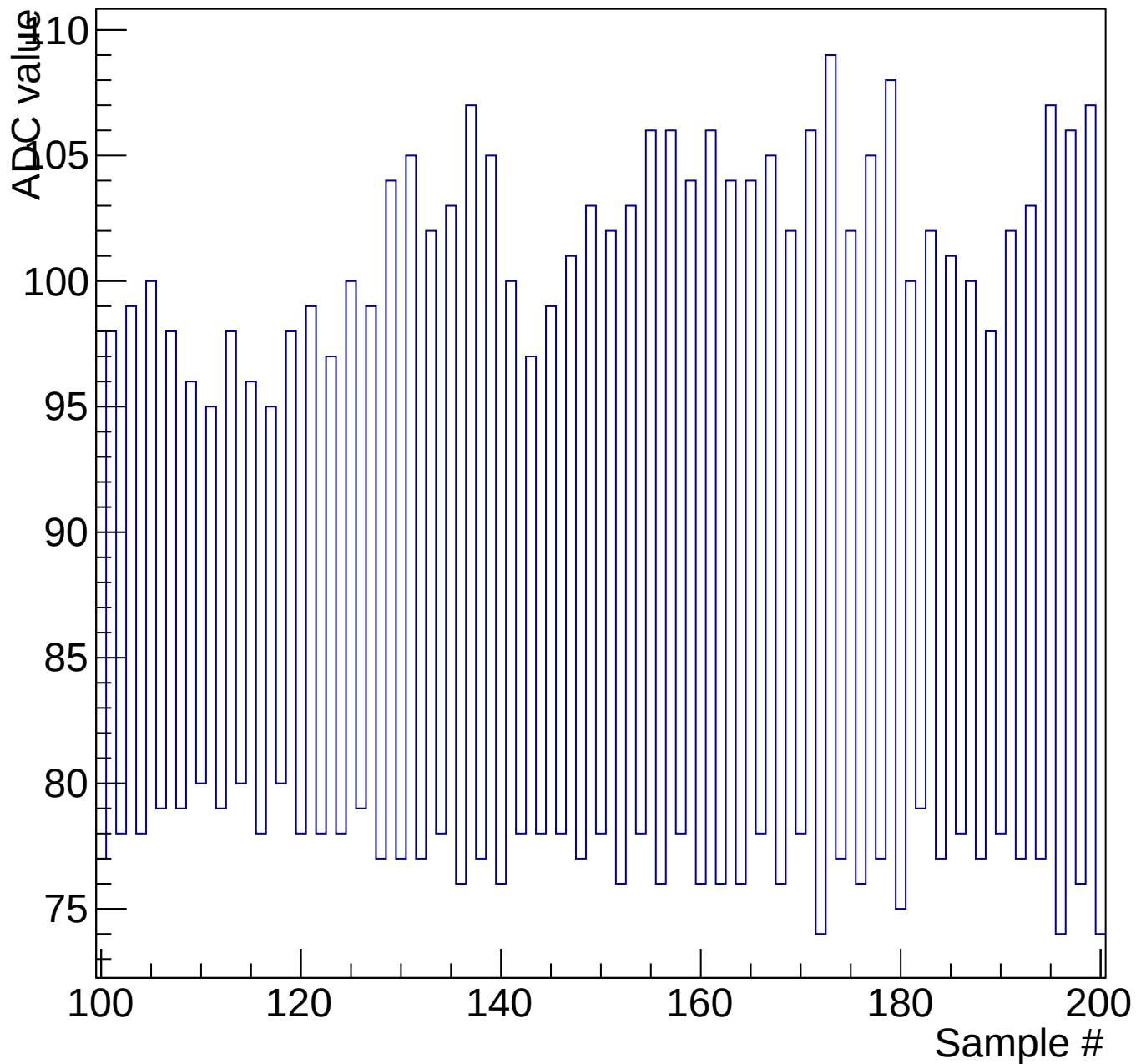
Pedestals ch 15 chip 62 nom



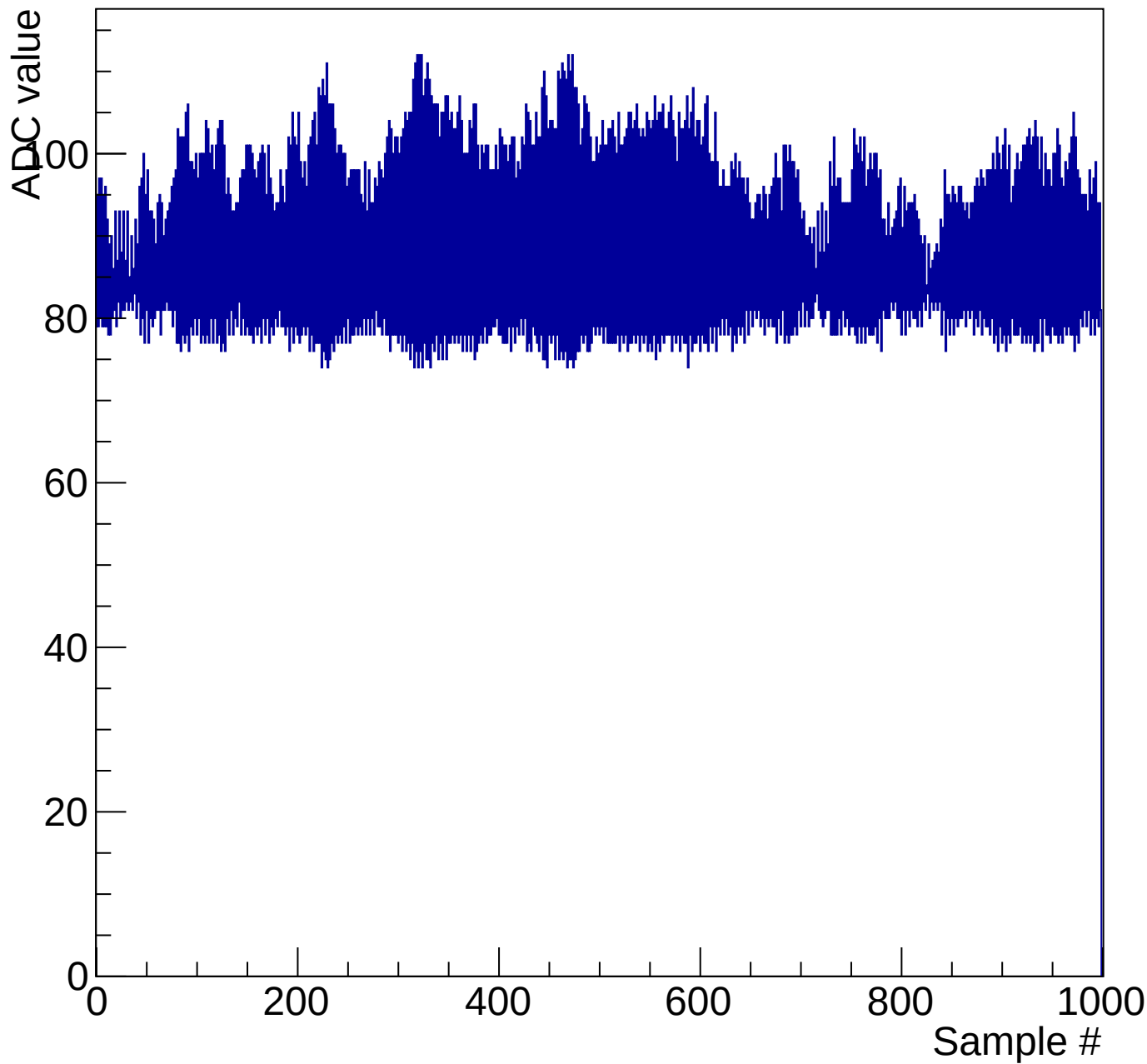
Pedestals ch 1 chip 62 run 34351 nom



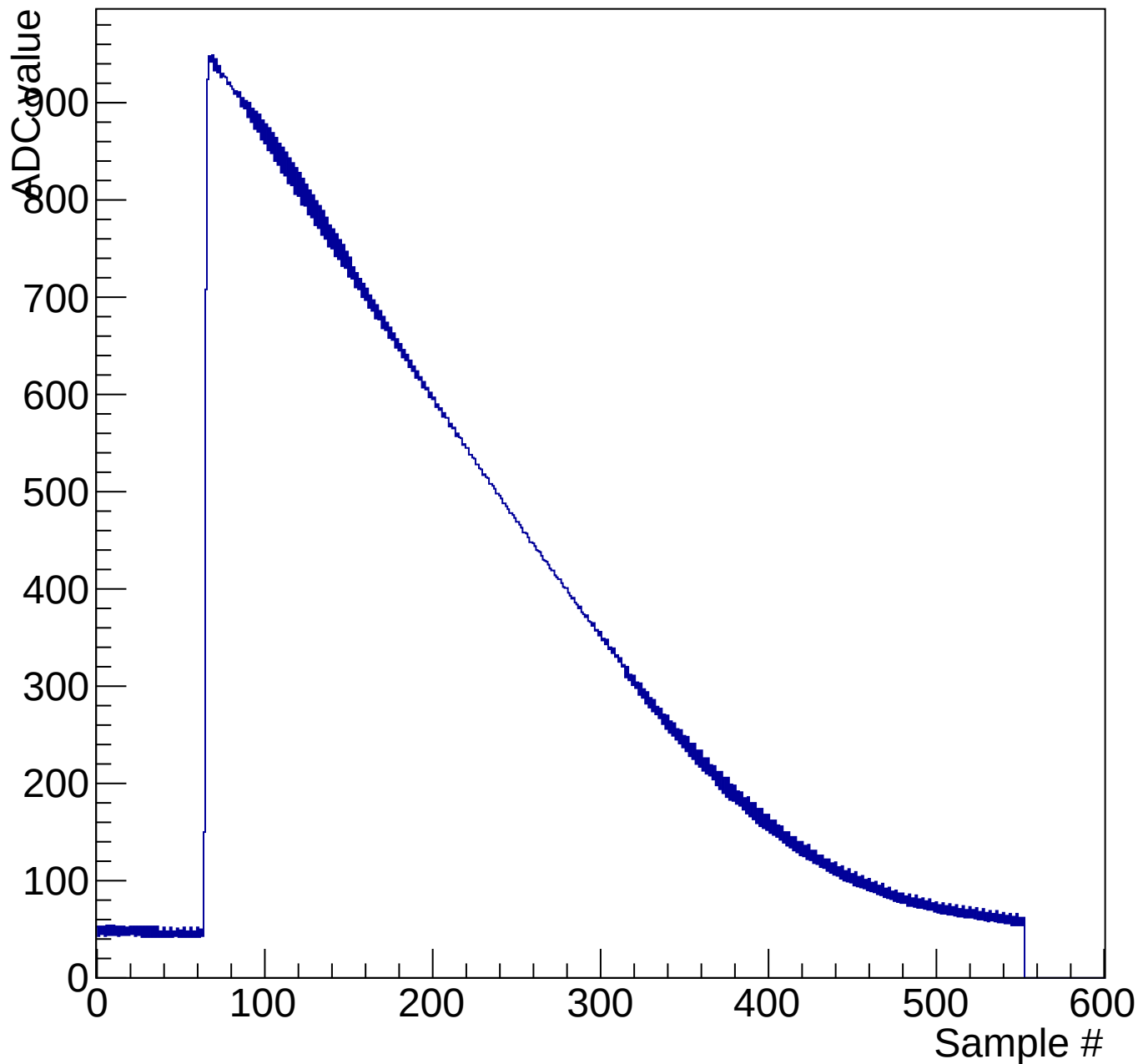
Run 34351 Event 1 Chip 62 Channel_1



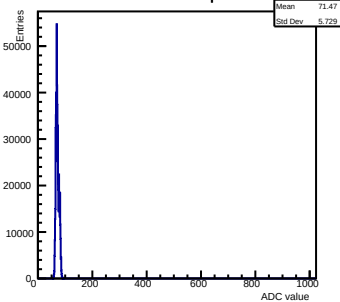
Run 34351 Event 2 Chip 62 Channel_1



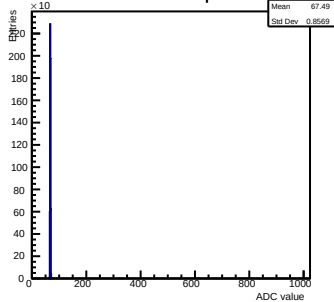
Run 34354 Event 126 Chip 62 Channel_1



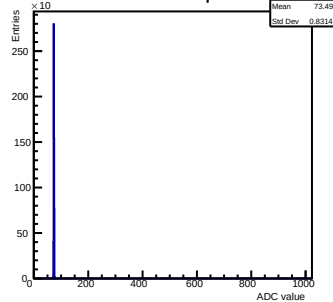
Pedestals ch 0 chip 60 nom



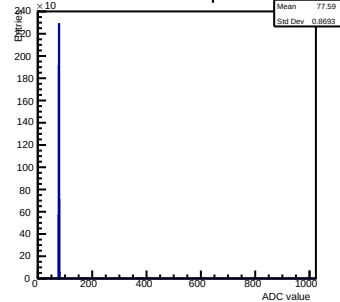
Pedestals ch 1 chip 60 nom



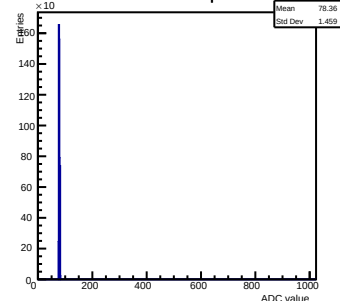
Pedestals ch 2 chip 60 nom



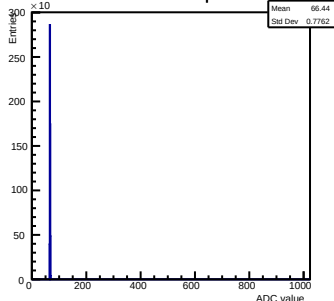
Pedestals ch 3 chip 60 nom



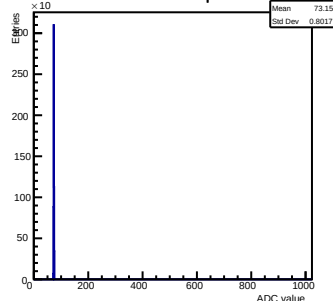
Pedestals ch 4 chip 60 nom



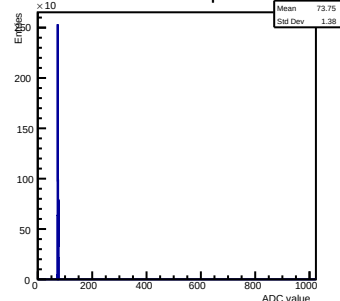
Pedestals ch 5 chip 60 nom



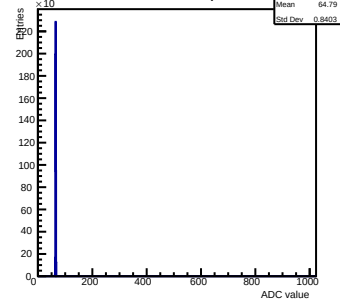
Pedestals ch 6 chip 60 nom



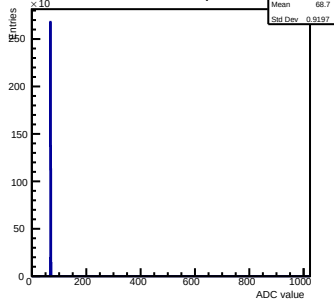
Pedestals ch 7 chip 60 nom



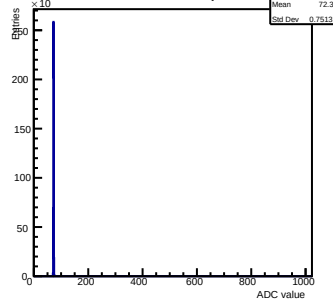
Pedestals ch 8 chip 60 nom



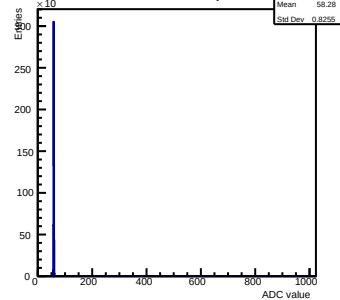
Pedestals ch 9 chip 60 nom



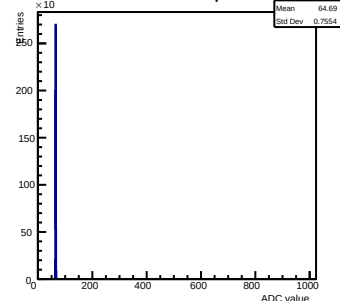
Pedestals ch 10 chip 60 nom



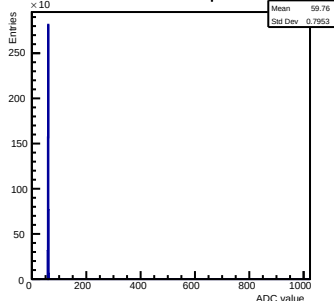
Pedestals ch 11 chip 60 nom



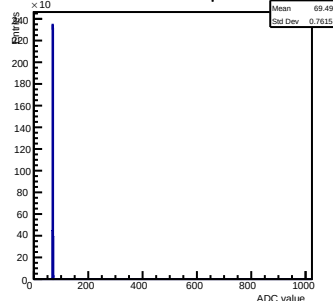
Pedestals ch 12 chip 60 nom



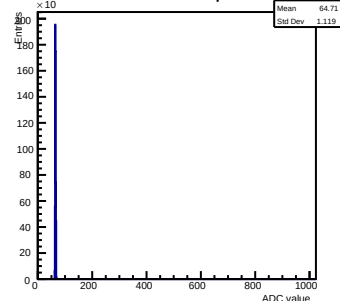
Pedestals ch 13 chip 60 nom



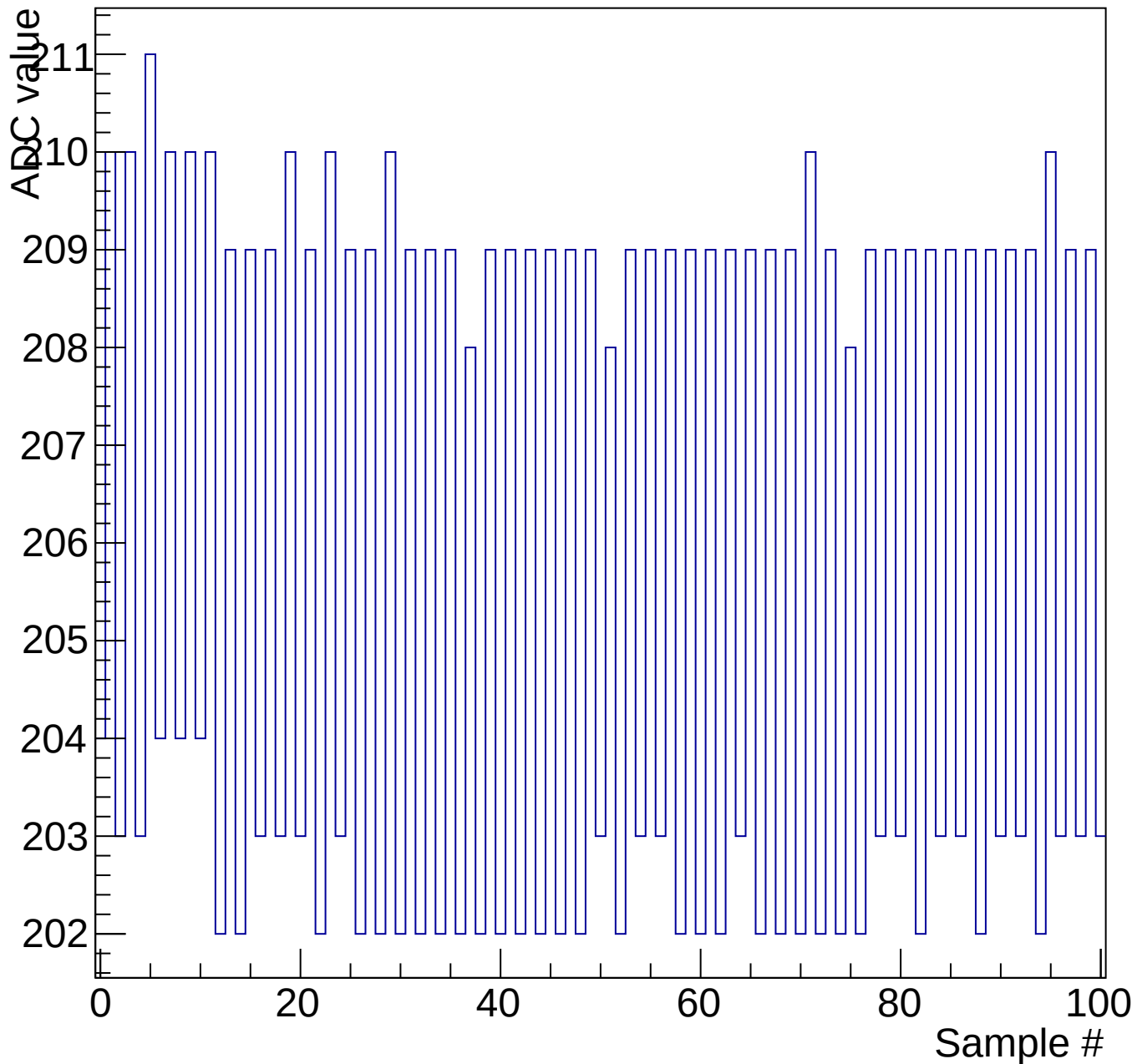
Pedestals ch 14 chip 60 nom



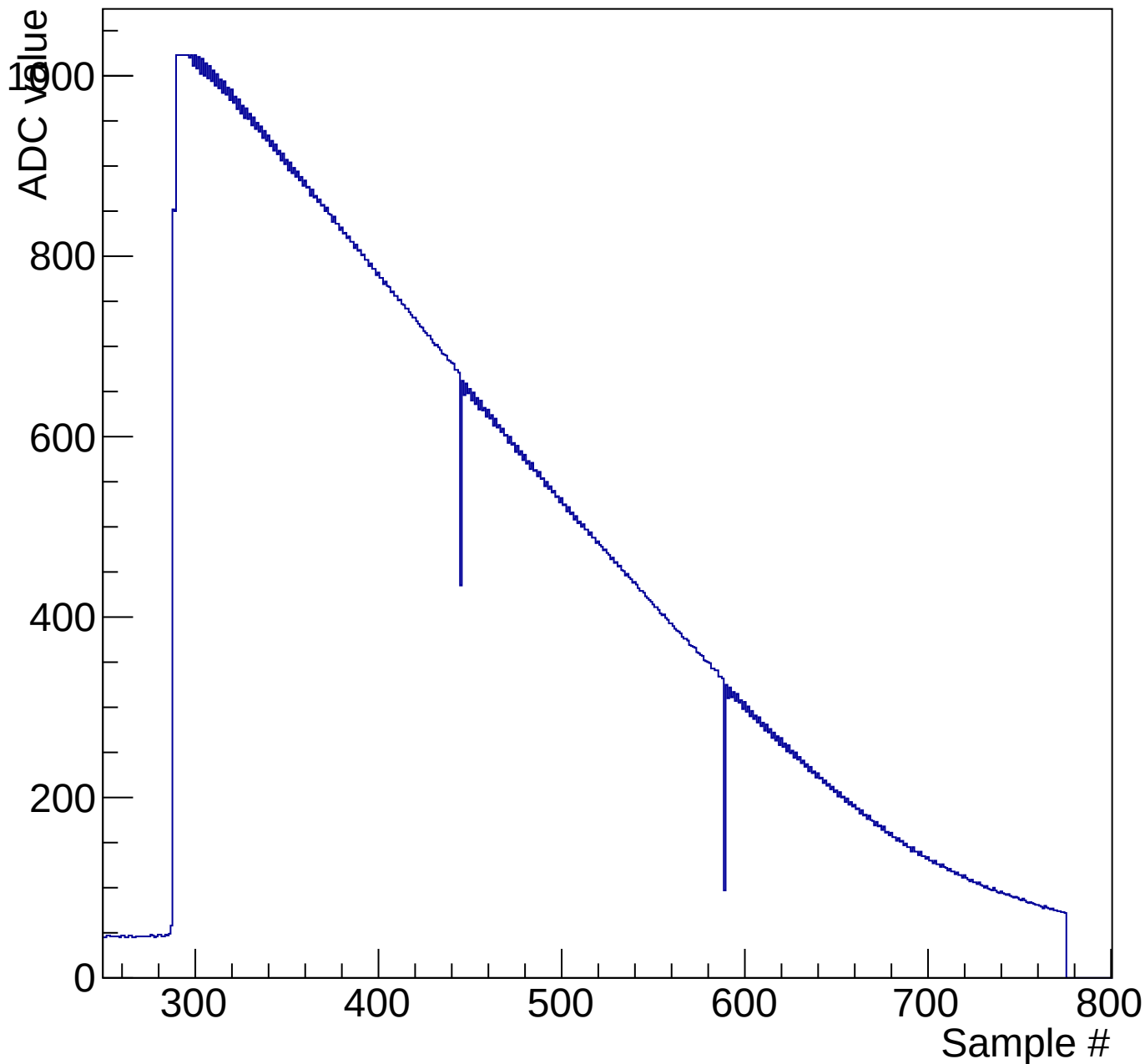
Pedestals ch 15 chip 60 nom



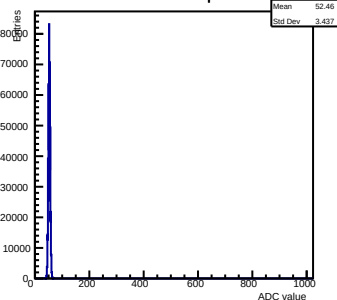
Run 34362 Event 1 Chip 60 Channel_11



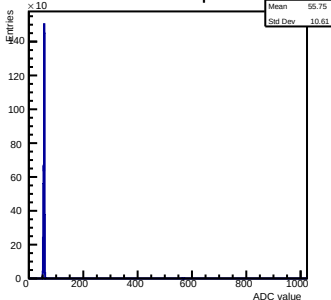
Run 34365 Event 95 Chip 60 Channel_11



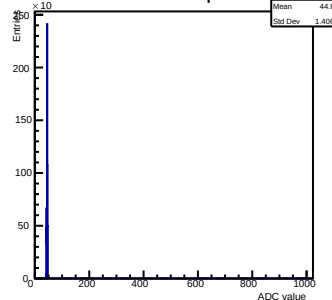
Pedestals ch 0 chip 57 nom



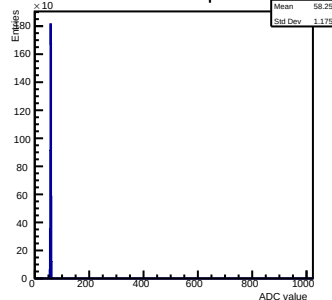
Pedestals ch 1 chip 57 nom



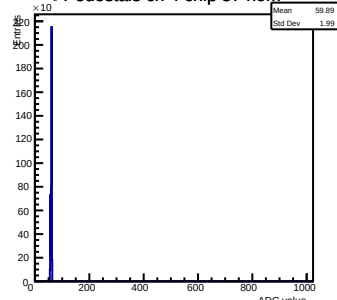
Pedestals ch 2 chip 57 nom



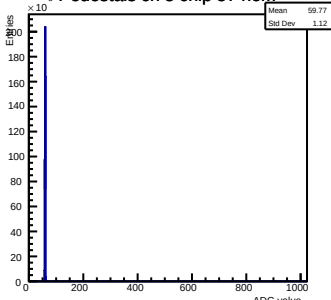
Pedestals ch 3 chip 57 nom



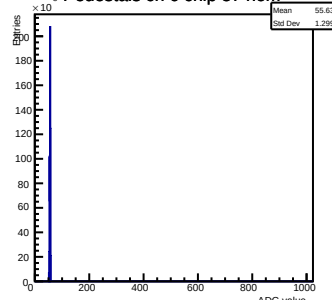
Pedestals ch 4 chip 57 nom



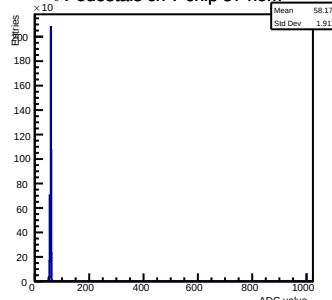
Pedestals ch 5 chip 57 nom



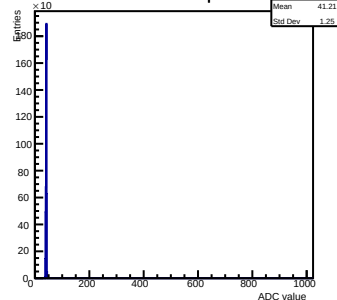
Pedestals ch 6 chip 57 nom



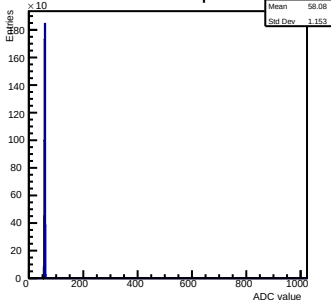
Pedestals ch 7 chip 57 nom



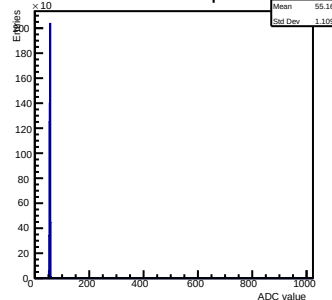
Pedestals ch 8 chip 57 nom



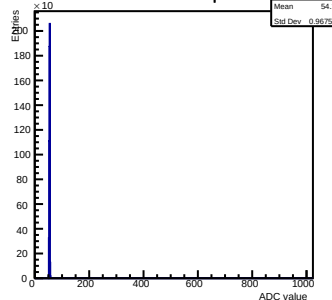
Pedestals ch 9 chip 57 nom



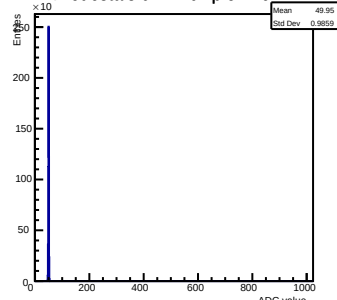
Pedestals ch 10 chip 57 nom



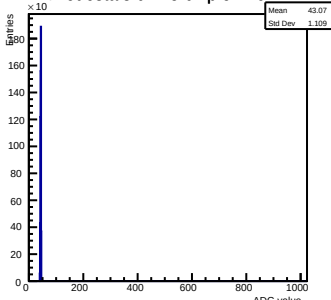
Pedestals ch 11 chip 57 nom



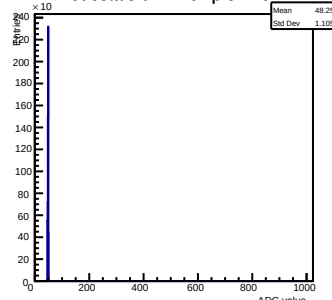
Pedestals ch 12 chip 57 nom



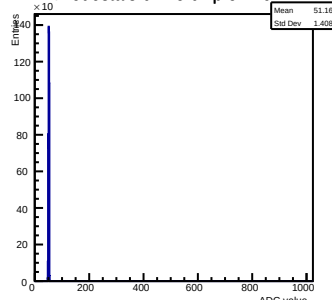
Pedestals ch 13 chip 57 nom



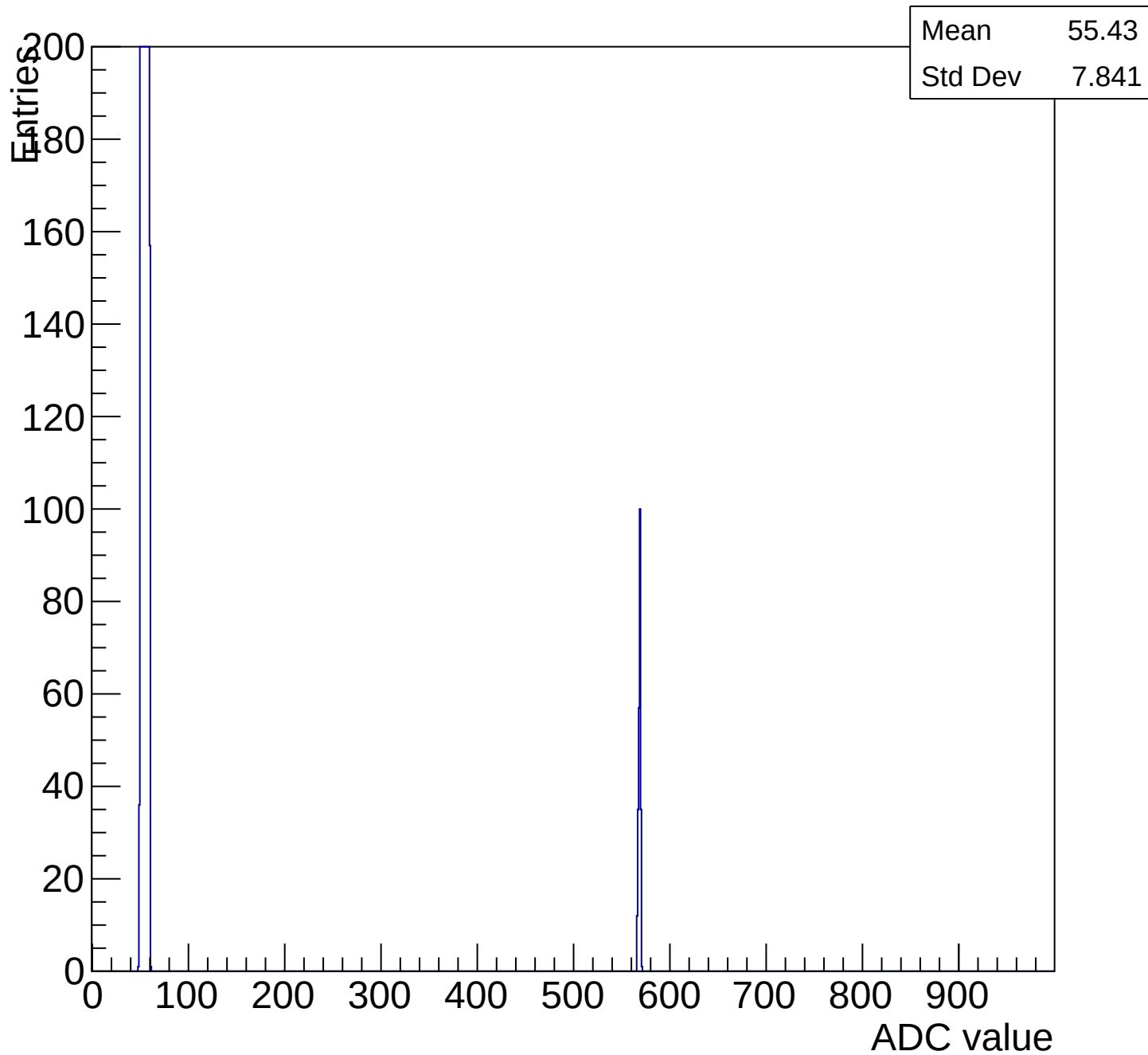
Pedestals ch 14 chip 57 nom



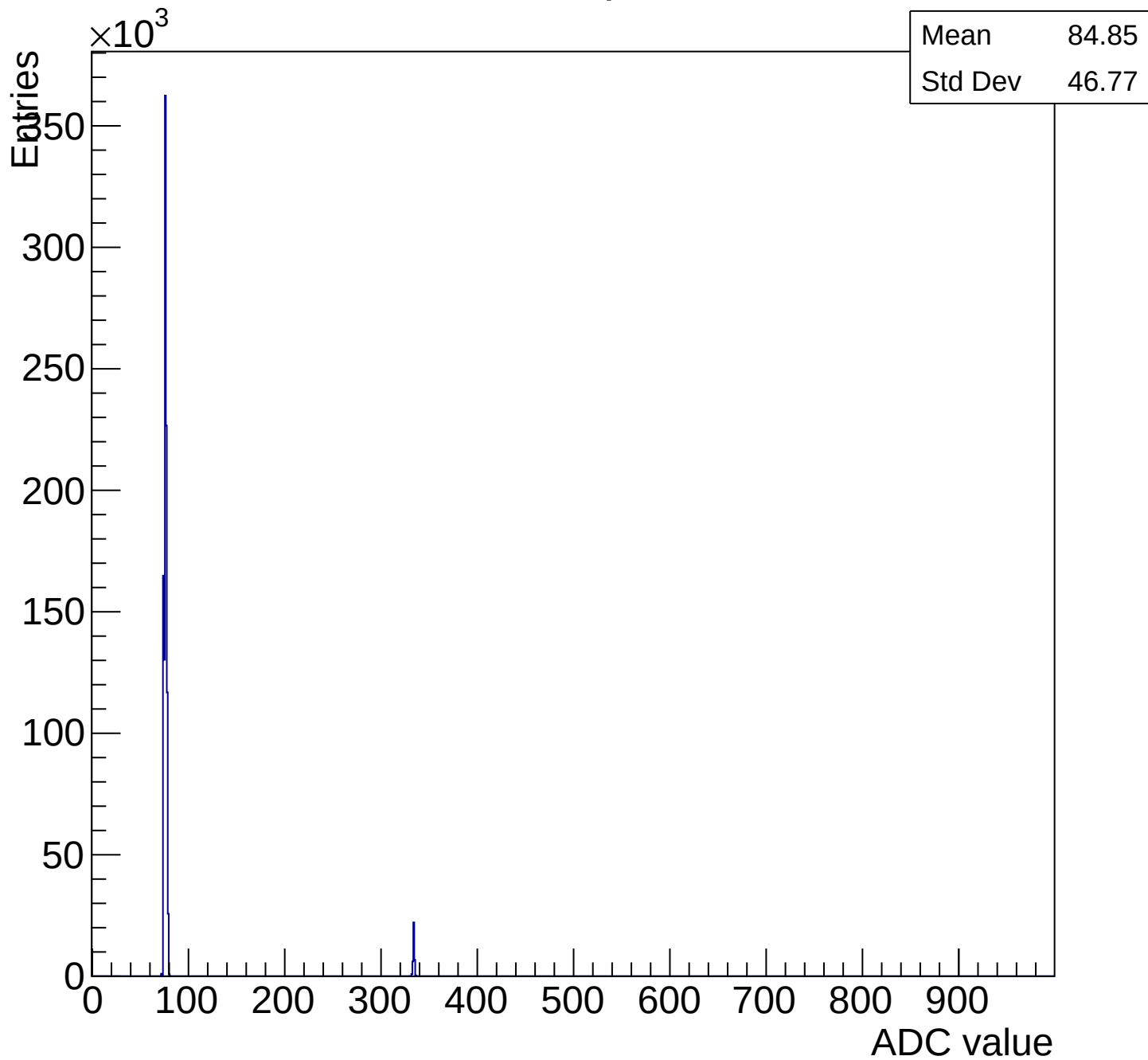
Pedestals ch 15 chip 57 nom



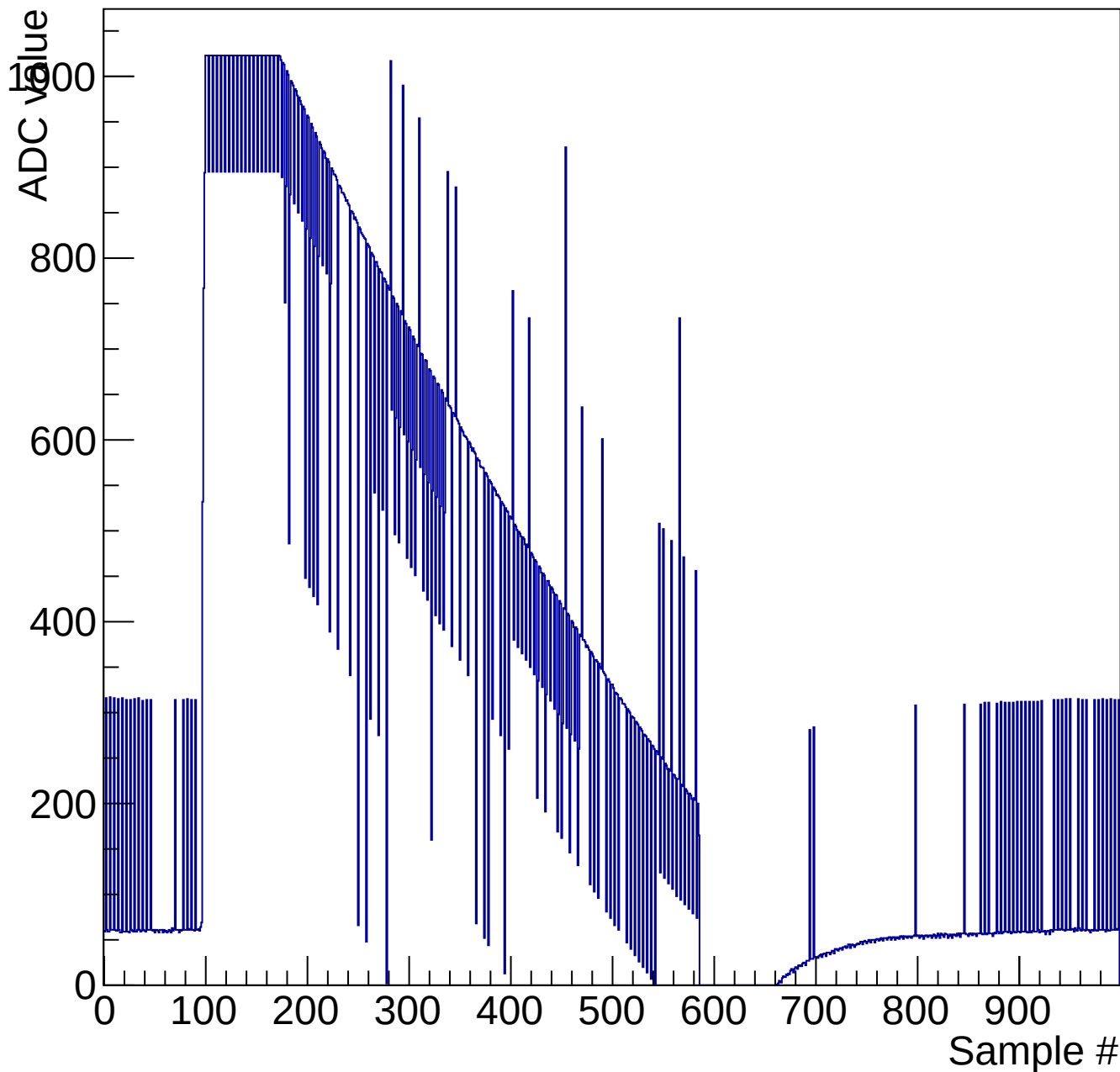
Pedestals ch 1 chip 57 run 34366 nom



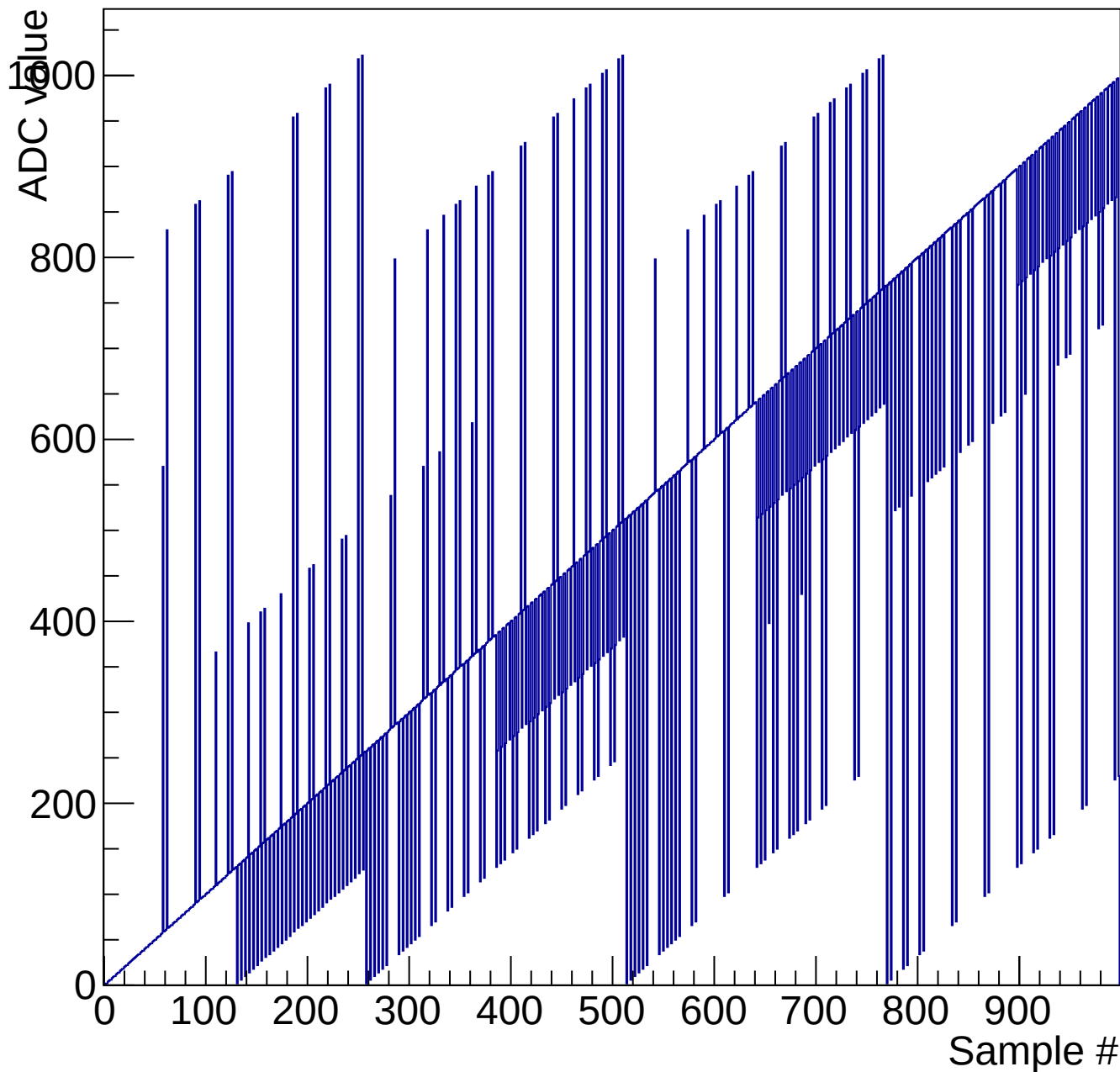
Pedestals ch 15 chip 55 run 34369 1



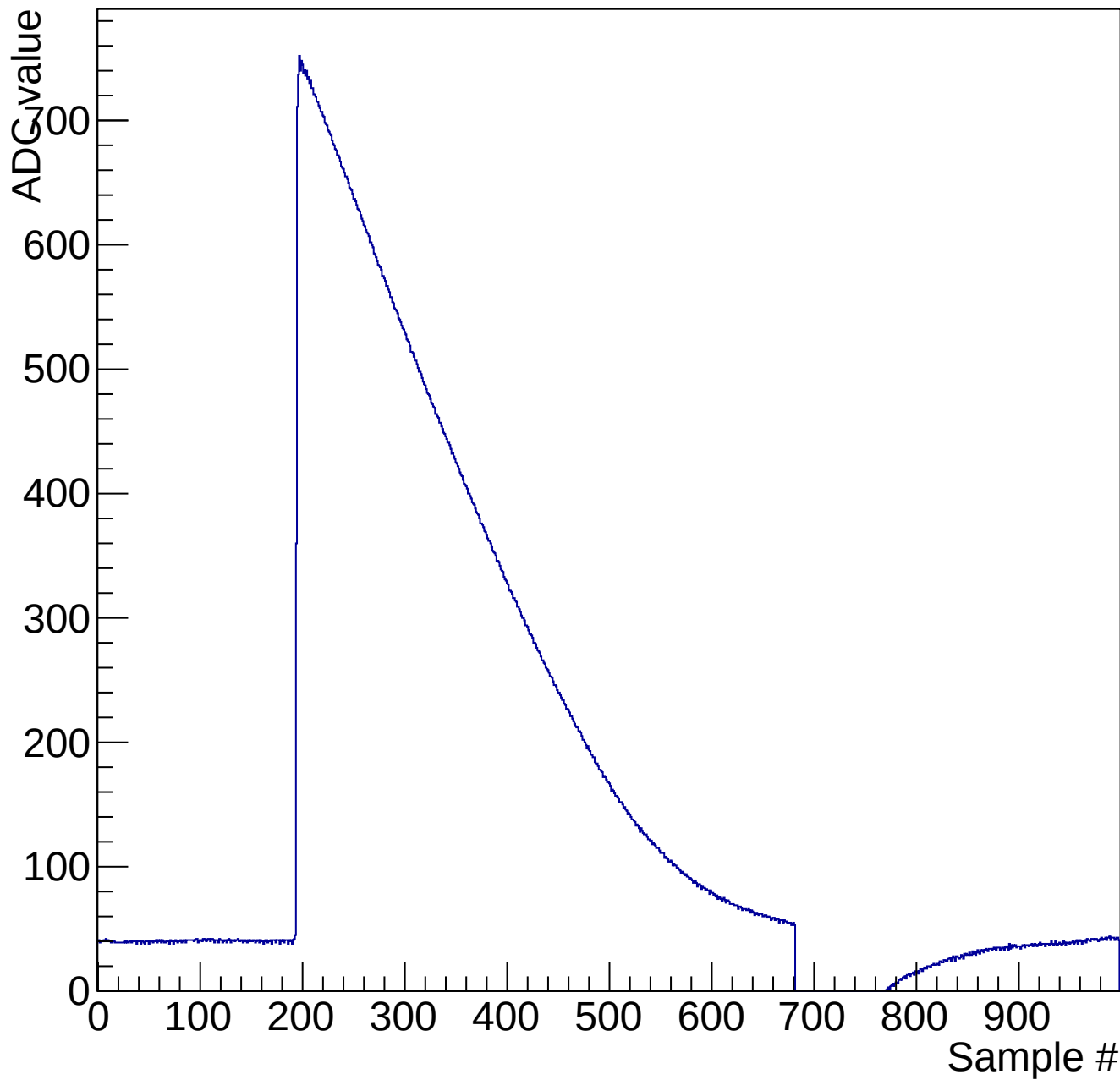
Run 34370 Event 1 Chip 55 Channel_15



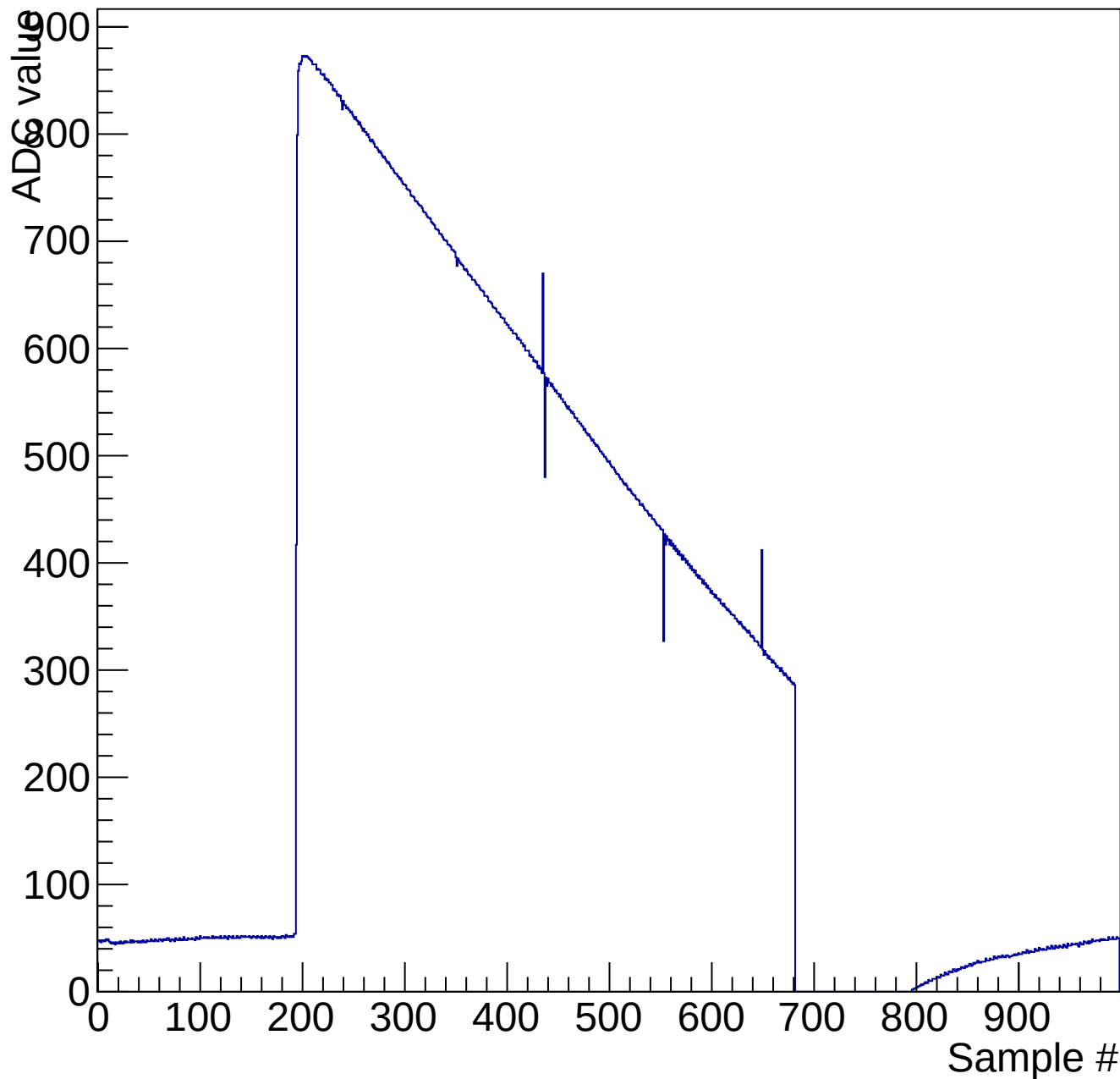
Run 34374 Event 1 Chip 55 Channel_15



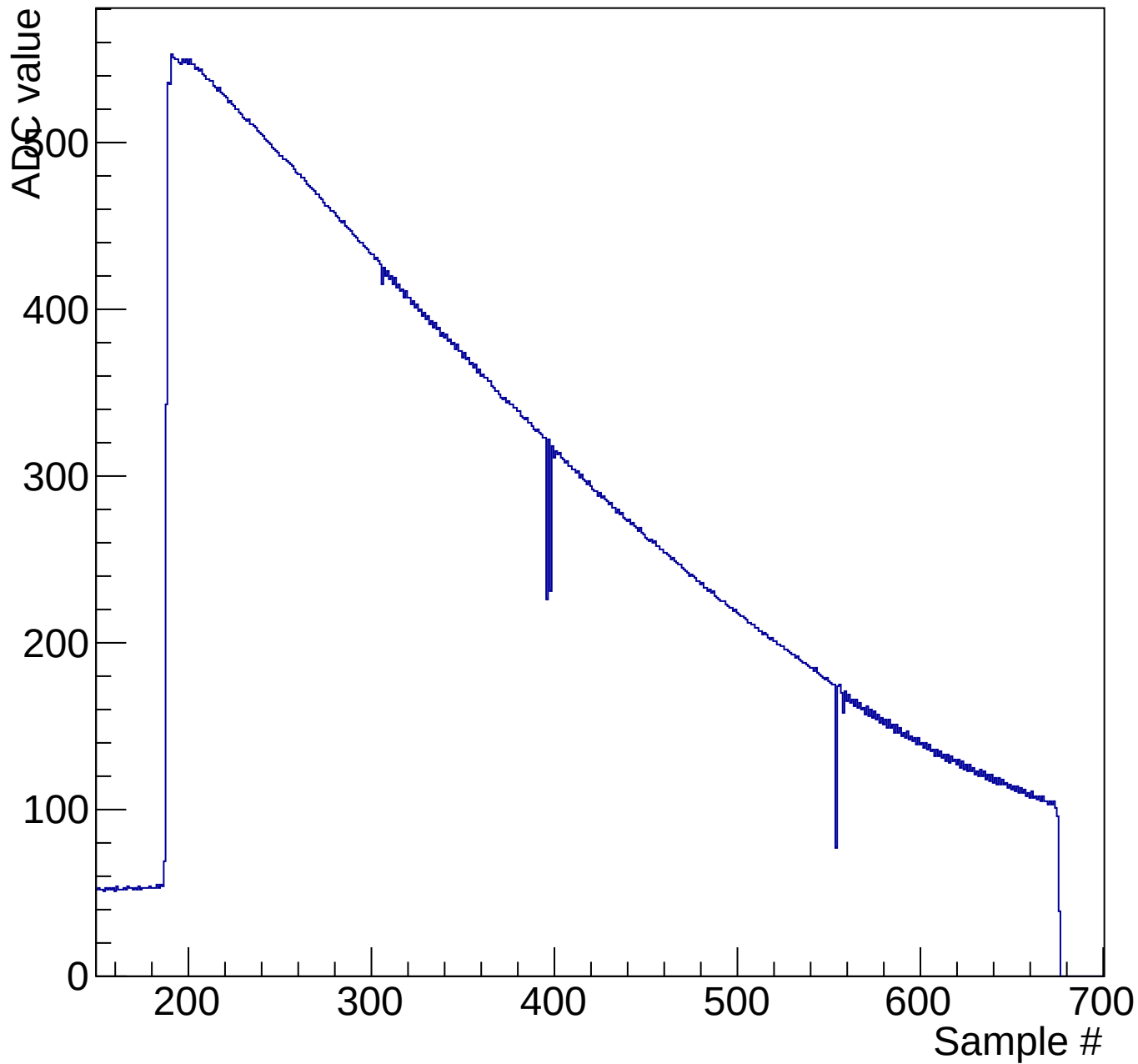
Run 34376 Event 134 Chip 52 Channel_8



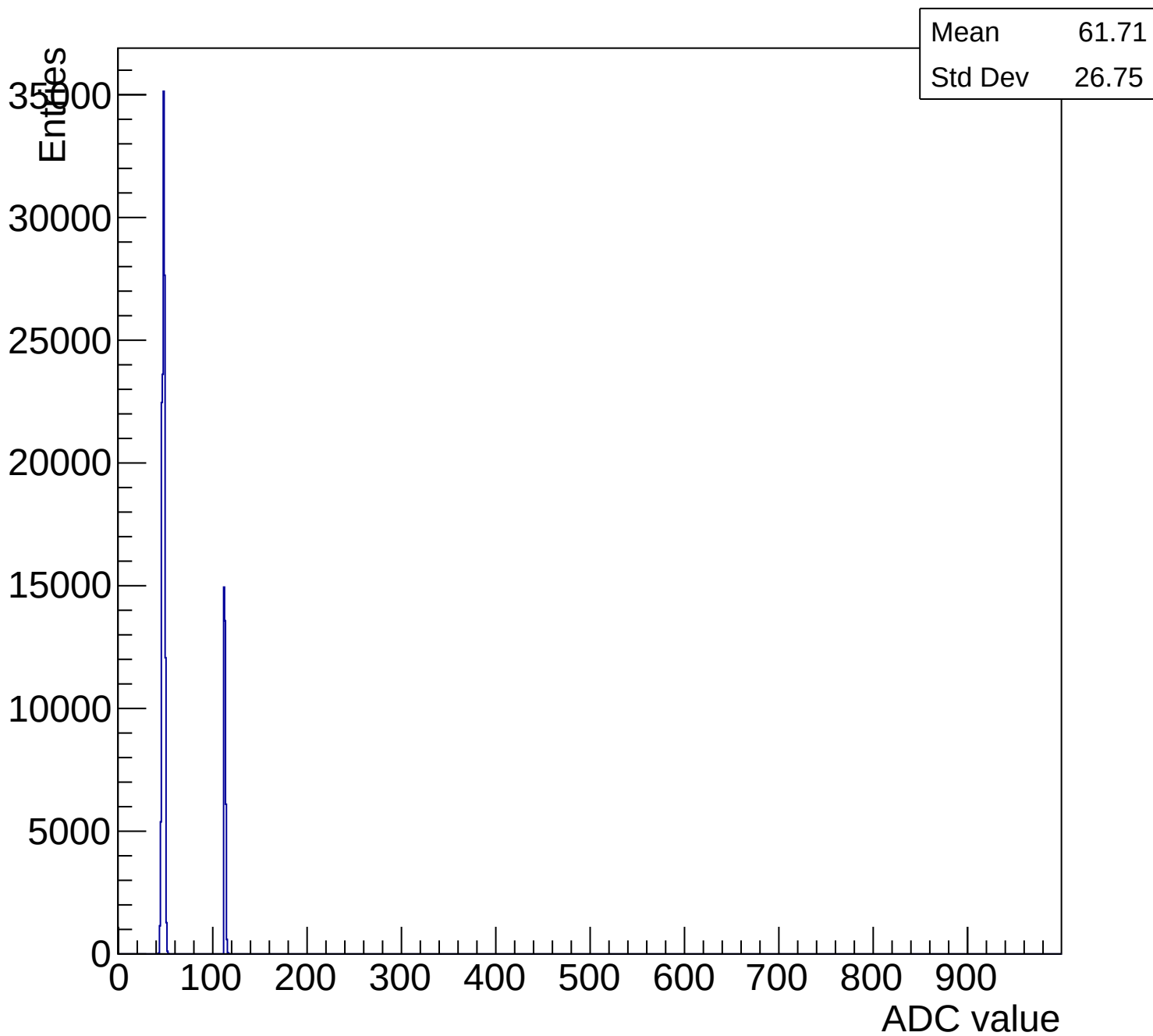
Run 34376 Event 134 Chip 52 Channel_9



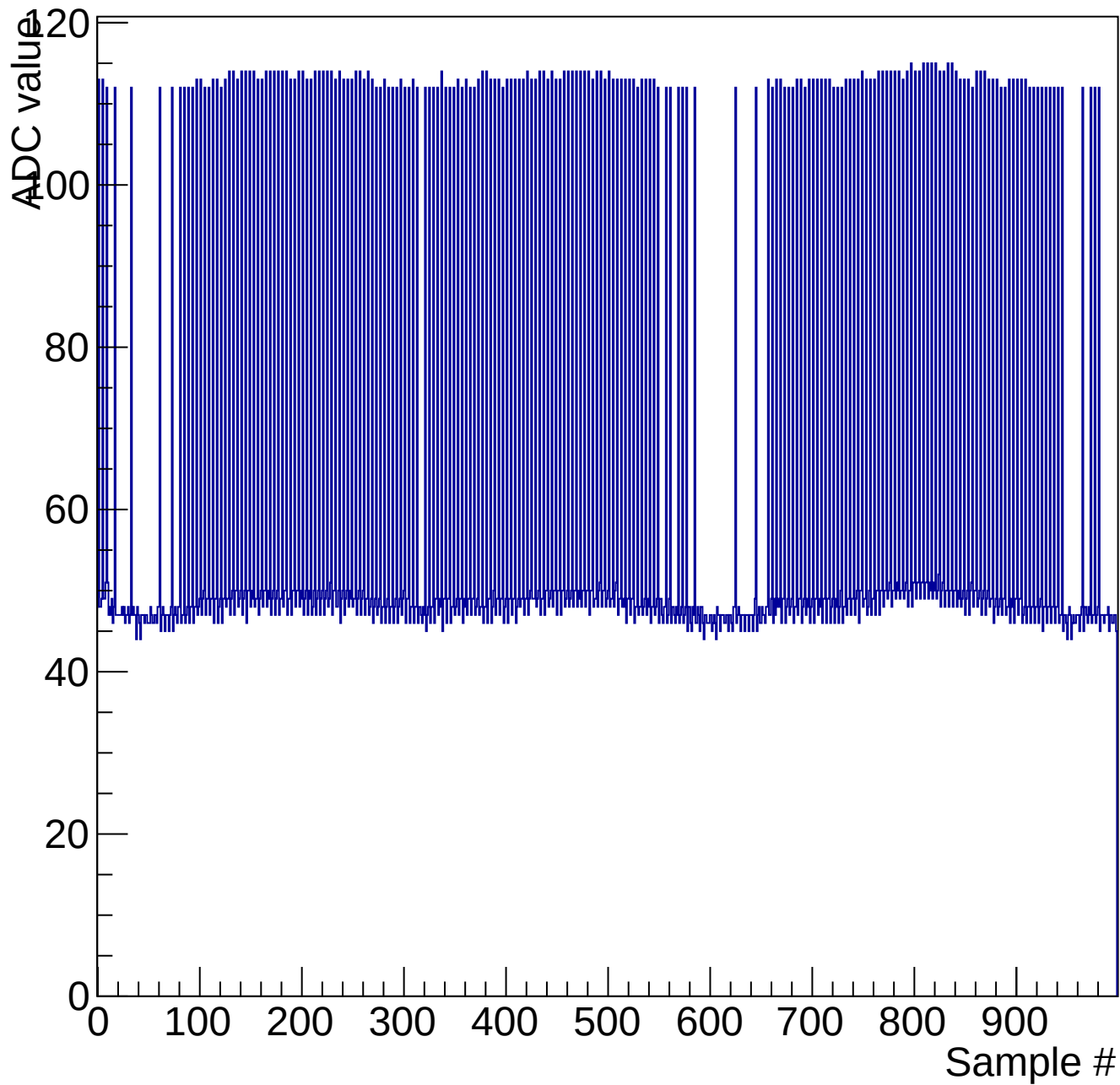
Run 34380 Event 1 Chip 52 Channel_9



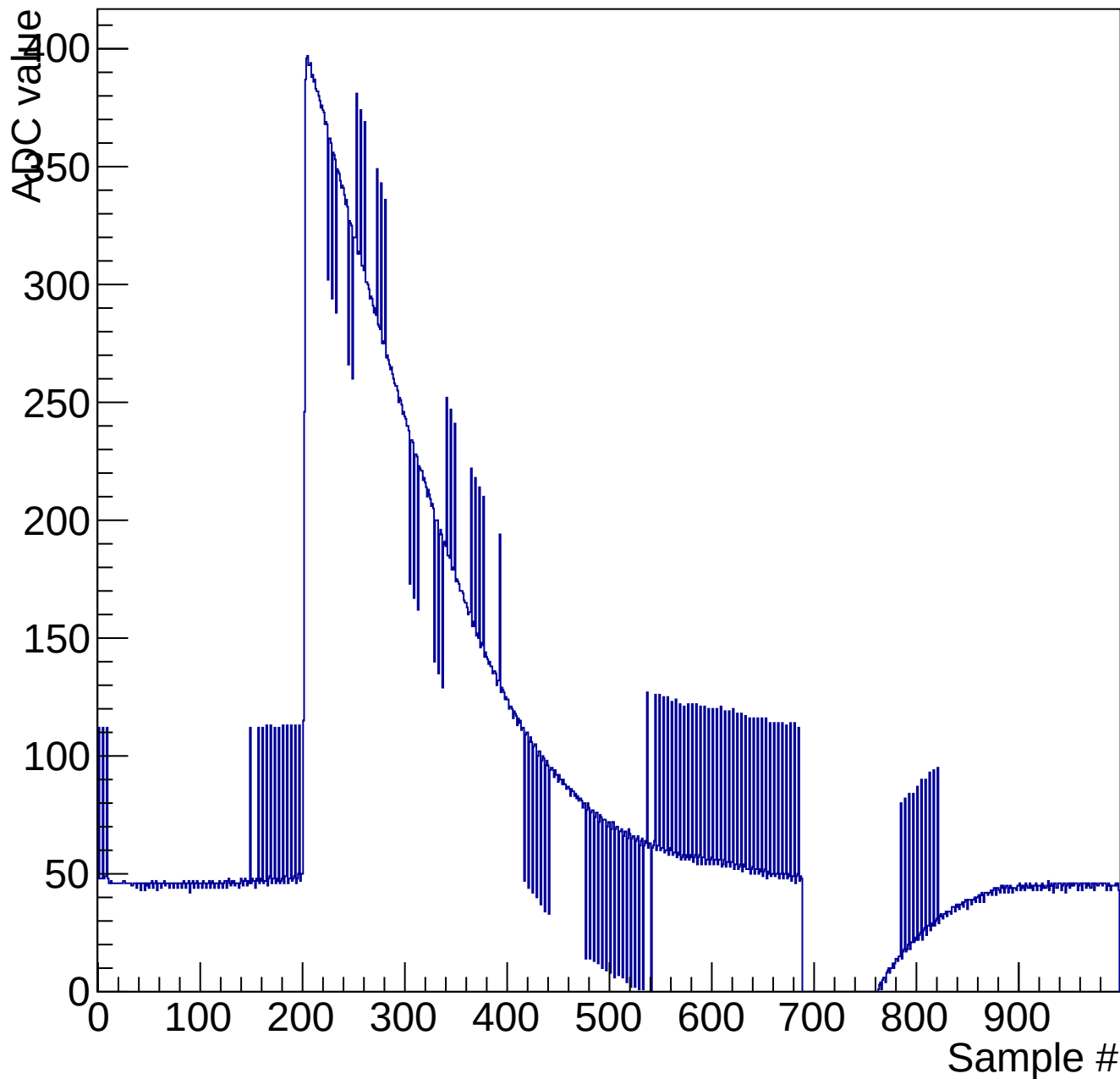
Pedestals ch 2 chip 38 run 34384 1



Run 34384 Event 211 Chip 38 Channel_2



Run 34385 Event 2 Chip 38 Channel_2



Run 34386 Event 150 Chip 38 Channel_2

