DTC link Protocol for ALICE EMCal/PHOS Detector

Description: This document is written for firmware designers of FEE/TRU and SRU on ALICE EMCal/PHOS detectors.

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1. Directions, bit rate and pin order of DTC signals on the RJ45 socket

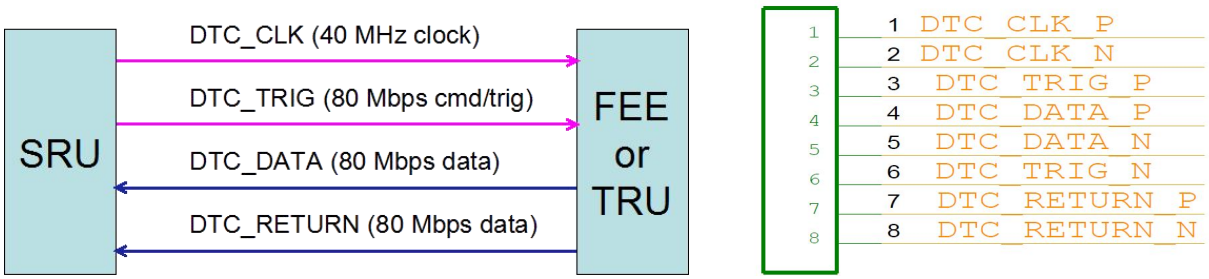
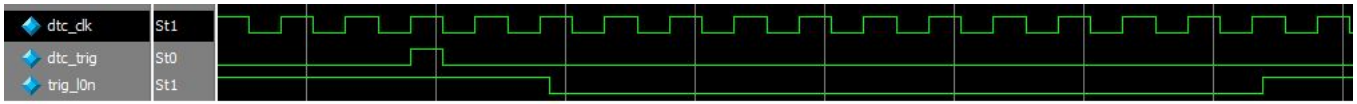


Fig. 1 Directions and bit rate of DTC signals and Pin order of DTC signals on the RJ45 socket (From DTC schematic)

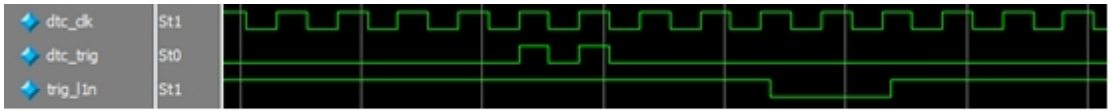
2. Format of Triggers and Commands transferred on DTC_TRIG

3 kinds of information are sent from SRU to FEE/TRU via DTC_TRIG line: Triggers, fast commands and slow commands.

- **Trigger info**: L0 (One 12.5 ns pulse); L1 (Two 12.5 ns pulses). Sent out during the positive period of DTC_CLK.



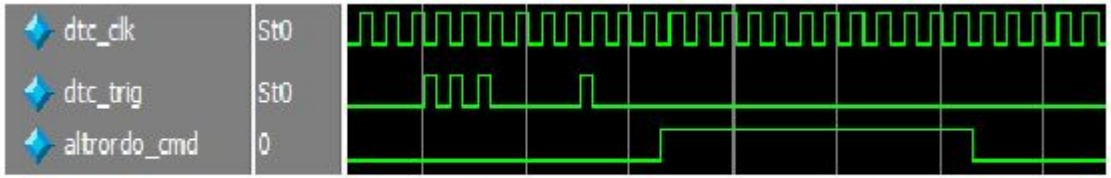
L0 trigger waveform: 1 pulse (12.5 ns) sent during the positive period of DTC_CLK



L1 trigger waveform: 2 consecutive high pulses, sent on the positive period of DTC_CLK

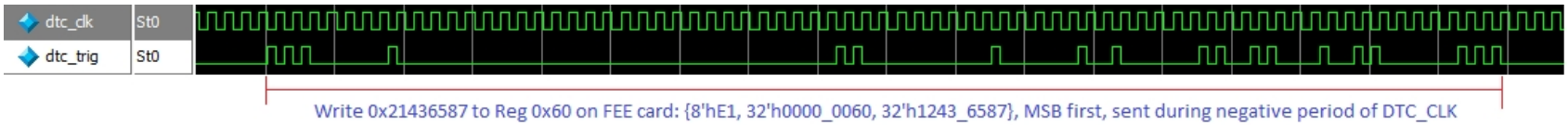
- **Fast command**: 8-bit wide, MSB first, sent out during the negative period of DTC_CLK.

Fast command	Coding	Description
RDOCMD	0xE2	Readout command, ask FEE/TRU readout ALTRO and transmit event data to SRU
SCLKSYNC	0xE4	Ask FEE to reset sampling clock divider
RJECTCMD	0xEA	Reject the event command (related to L2r trigger), ask FEE/TRU to discard the associated event data stored in the ALTRO buffer.
RSTCMD	0xE8	Reset TRU/FEE, asserts “reset” pin of ALTRO on FEE.
STREQ	0xE9	Ask FEE/TRU to send its status (The Status Frame) to SRU
ARDOEND	0xEF	Tell TRU that ALTRO readout in FEE is finished (ALTRO readout starts after FEE receives RDOCMD).



Readout command from SRU to FEE: 8-bit (8'hE2), MSB first, sent on negative period of DTC_CLK

- **Slow command**: To write or read registers. 0xE1(8-bit Header)+ Reg addr (32-bit) + Reg data (32-bit), MSB first, sent out during the negative period of DTC_CLK.
  - Address bit[31]: RW operation flag. '0': write; '1': read
  - Address bit[30]: FEE FPGA/ALTRO select bit. '0': FPGA registers; '1': ALTRO registers
  - In a read command, the Reg data field could be any value.
  - The definition of the other filed in Address field is up to the TRU/FEE firmware designer.



3. **Format of Reply and Event data transferred on DTC_DATA and DTC_RETURN**

Data are sent from FEE/TRU to SRU via DTC_DATA and DTC_RETURN lines, the bit rate on each line is 80M bps.

Bit order of **16 -bit** word, **LSB** first, **40 MHz DDR** mode								
DTC_DATA	Bit0	Bit2	Bit4	Bit6	Bit8	bit10	bit12	bit14
DTC_RETURN	bit1	Bit3	Bit5	Bit7	Bit9	bit11	bit13	bit15

Frame structure:

Status Frame: one header (**0xDCDC**) followed by one 16-bit **status** word.

- Bit[15] of status is the summary of the error flags. 0: TRU/FEE works fine. 1: Abnormal status detected.
- The definition of other bit fields is up to the TRU/FEE firmware designer

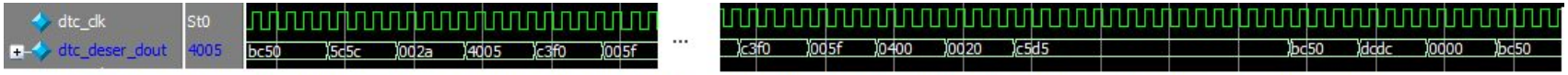
Reply Frame: one header (**0xF7F7**) followed by **address and data** (16-bit high addr, 16-bit low addr, 16-bit high data, 16-bit low data).

Event Frame: one header (**0x5C5C**) followed by **event data** and Event end flag (**0xC5D5 C5D5 C5D5 C5D5**).

- The length of the event data can be variable, depending on the event size.
- No event length word need be put in the Event Frame, the SRU will count it.



After SRU sent a read command (read Reg 0x20) to FEE, FEE sends a Reply packet and a Status packet to SRU.
Reply packet: 0xF7F7(Header), 0x8000_0020 (Read cmd with Reg addr), 0x0000_5040 (Content of Reg 0x20)
Status packet: 0xDCDC (Header), 0x0000 (Status)
At least 2 Sync words (0xbc50) should be inserted between Reply packet and Status packet.



Event Frame: 0x5C5C (Header), 0x002A (Low 16-bit), 0x4005 (High 16-bit) ... 0x0400 (Low 16-bit), 0x0020 (High 16-bit), 0xC5D5_C5D5_C5D5_C5D5(Trailer)
Status Frame: 0xDCDC(Header), 0x0000 (Status)
At least 2 consecutive Sync words (0xBC50) should be inserted between Event Frame and Status frame.

4. Frame Sequence Rule

1) The framing should guarantee that there is at least 2 Sync words (0xBC50) between each frame.
2) Every Reply or Event frame is followed by one Status frame.
3) Frame Sequence Order Example:

0xBC50,0XBC50,**Reply Frame**,0xBC50,0XBC50,**Status frame**,0xBC50,0XBC50 ... **Event frame**,0xBC50,0XBC50,**Status frame**,0xBC50,0XBC50 ...

5. Event Data Format Conversion

- **40-bit ALTRO** data format: The data packet structure readout from each ALTRO channel is described as below.

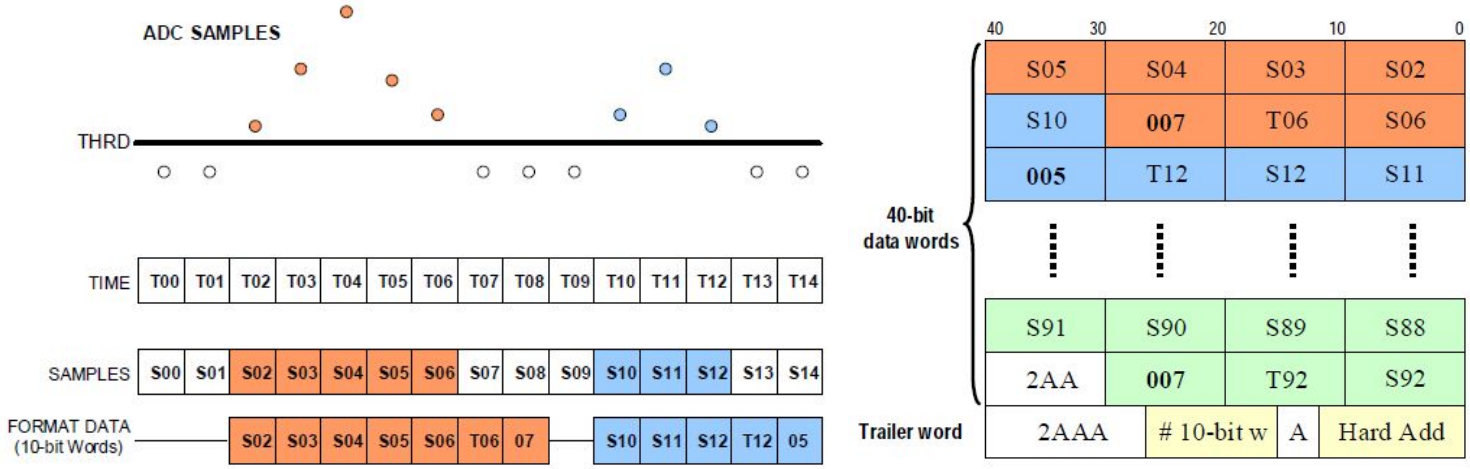


Fig. 2 **40-bit** ALTRO data format. **"A","2AA","2AAA"** hexadecimal pattern are packed in 40-bit words if data is not enough to complete a 40-bit word. "**#10-bit w**" is the total number of 10 bit words in the packet, this word provides the position of the last 10-bit word in the data packet; "**Hard Add**" is a sort of geographical address, includes 5-bit FEE addr + 3-bit ALTRO chip addr + 4-bit ALTRO channel addr. (**From ALTRO user manual**)

- **32-bit Event data** format: The event frame transferred from FEE/TRU to SRU is in 32-bit wide format. The data format of the event packet between the event header (0x5C5C) and Trailer word (0xC5D5_C5D5_C5D5_C5D5) is described below. It is **exactly as same as** the payload structure described in the **RCUV2 firmware manual**.



ALTRO Channel Header Format	
Bit location	**Meaning**
[11:0]	"**Hard Add**" from 40-bit ALTRO data
[15:12]	Reserved = "0000"
[25:16]	"**#10-bit w**" from 40-bit ALTRO data
[28:26]	Reserved = "000"
[29]	E: Channel Error Bit, set to '1' when a a mismatch for channel address or word count is detected. FEE will correct the corresponding info field.
[31:30]	Mark: "00" : Payload; "01" Header.

Fig. 3 32-**bit** FEE event data format. **"0x00"** hexadecimal pattern are packed in 32-bit words if data is not enough to complete a 32-bit word; "**DW0, DW1 ... DW9**" are 10-bit words from 40-bit ALTRO data; "**ALTRO channel header n**" is described as the table above.