ALICE EMCal/PHOS SRU FEE Firmware Register Table

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1 Firmware note

1) Last updated : 2015-07-19
2) PHOS SRU FM Ver = 0x2015071901; EMCal SRU FM Ver = 0x2015071911
3) FEE FM Ver = 0x5043
4) FPGA Part number: XCVLX130T-FFG1156C (Working range: 0 ~ 85 degree)
5) Compatible with CDH V2 and V3, configured by SRU Reg 0x20.
6) PAR (Pause-And-Reset (PAR) procedure) can be set by SRU Reg 0x20
7) DDL SN format: if SRU IP is XXX.XXX.XXX.156, then DDL0 SN is 1560, DDL1 SN is 1561.
8) EMCal has 5 more registers (Reg 0x6E, 0x6F, 0x71,0x73, 0x76) than PHOS to show info of DDL1.
9) Status register 0x4 of EMCal has 3 more bits (Bit 9,10,11) to show status of DDL1. Definition of other registers are totally same as PHOS.
10) In EMCal version, DDL link mask is decided by the content of DTCRDOMASK (Reg 0x23, 0x24). If Reg 0x23 = 0xfffff (all the DTC are masked), then DDL0 is masked/disabled. If Reg 0x24 = 0xfffff (all the DTC are masked), then DDL1 is masked/disabled.
11) Slow control is upgraded. The format of reply to DCS is fixed, including three 32-bit words: node ID, reg addr, reg data.

2 SRU Cable Connection

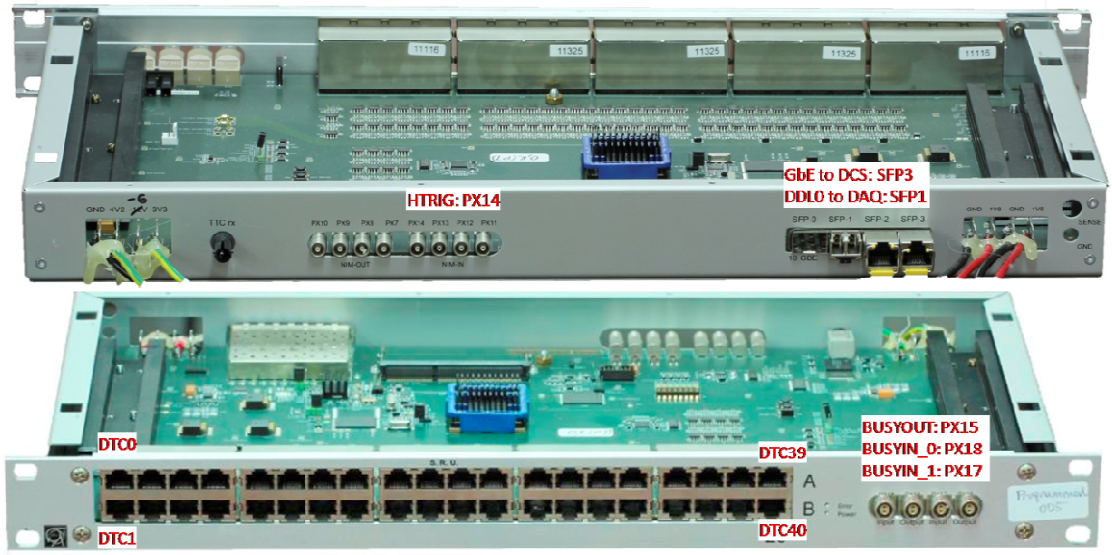


Fig. 1 SRU Cable Connection.

3 SRU Register Table

Group 1: Registers for Normal Readout Setup and Monitoring				
NAME	ADDR	TYPE	MEANING	DEFAULT VALUE(HEX)
Status				
S/N	01	R	Serial Number	-
IP	02	R	IP address	-
FMVER	03	R	Firmware version	-
SRUST	04	R	Status	-
DTCERRFLAG[19:0]	05	R	Error flag received from DTC0-19	-
DTCERRFLAG[39:20]	06	R	Error flag received from DTC20-39	-
FPGAMonReg	07	RW	SRU FPGA Monitor Flag, Addr and Temp	-
Command				
RESET	10	W	Reset SRU and FEE and ALTRO	-
PSSCAN	11	W	Phase scan command	0x11
WALIGN	12	W	DTC link word alignment command	-
BUSYCLR	13	W	Clear BUSY and Error flags, clear the data fragment in the buffer, reset all FEE.	-
DDLINIT	14	W	Init DDL link	
Configurations				
SRUCFG	20	R/W	Configuration Registers	0000 0009
DTCCLKEN[19:0]	21	R/W	Clock switch of DTC0-19 links	000 00000
DTCCLKEN[39:20]	22	R/W	Clock switch of DTC20-39 links	000 00000
DTCRDOMASK[19:0]	23	R/W	Readout mask of DTC0-19 links	000 FFFFF
DTCRDOMASK[39:20]	24	R/W	Readout mask of DTC20-39 links	000 FFFFF
ALTROCFG1	27	R/W	[9:0]: Zero suppression offset [13:10]: Zero suppression threshold [15]: Zero suppression enable/disable	000 00000
ALTROCFG2	28	R/W	[4:0]: L1 phase [8:5]: ALTRO sampling rate with respect to LHC clock [19:10]: Number of samples [23:20]: Number of pre-samples [24]: Number of ALTRO buffers	000 00000
TRIGL1TW	29	R/W	Time windows of level-1 trigger	012C 0078
TRIGL2TW	2A	R/W	Time windows of level-2 trigger	4E20 00C8

Group 2: Registers for Debugging Purpose				
NAME	ADDR	TYPE	MEANING	DEFAULT VALUE(HEX)
Commands				
FPGARELOAD	40	W	Reload firmware from Flash to FPGA	-
FEEFASTCMD	41	W	Fast command to FEE	-

STRIGCMD	42	W	Send one software trigger sequence	-
TRIGCNTCLR	43	W	Clear all trigger counters	-
TRIGERRCLR	44	W	Clear all trigger errors	-
DTCERRTEST	45	W	DTC link Error Tester command	-
Configuration				
PTRIGCFG	50	R/W	Periodical software triggers configuration (16'h4E20 = 500 us)	0000 4E20
TESTTRIGCFG0	51	R/W	Test trigger configuration 0 (12C0 = 120 us)	12C0 0064
TESTTRIGCFG1	52	R/W	Test trigger configuration 1 (1770 = 150 us)	000d 1770
Status				
RXL0CNT	60	R	Number of received L0 triggers by SRU	-
RXL1CNT	61	R	Number of received L1 triggers by SRU	-
RXL2ACNT	62	R	Number of received L2a triggers by SRU	-
RXL2RCNT	63	R	Number of received L2r triggers by SRU	-
TXL0L1CNT	64	R	Number of transmitted L0_L1 triggers to FEE	-
TXL2ACNT	65	R	Number of transmitted L2a triggers to FEE	-
TXL2RCNT	66	R	Number of transmitted L2r triggers to FEE	-
TRIGERRCNT	67	R	Number of invalid trigger sequences	-
DTCERRFLAG0	68	R	DTC test error flag of DTC0-19 links	-
DTCERRFLAG1	69	R	DTC test error flag of DTC20-39 links	-
L2ABUNCNT	6A	R	Bunch counter in last L2a message	-
L2AORBCNT	6B	R	Orbit counter in last L2a message	-
DDLDEBUGREG1	72	R	DDL0 interface debug register	-
DDLDEBUGREG2	73	R	EMCal DDL1 interface debug register	-
TRIGDEBUGREG	74	R	Trigger debug register	-
DDL0ECNT	75	R	Number of transmitted event over DDL0	-
DDL1ECNT	76	R	Number of transmitted event over EMCal DDL1	-
L2aMes8Cnt	7A	R	L2a Message counter	
DTCEventRdy [19:0]	7B	R	DTC Event Ready Status	
DTCEventRdy [39:20]	7C	R	DTC Event Ready Status	
				-
DRXDATA	1028-104F	R	Data over DTC link	-
DERRCNT	10A0-10CF	R	ERROR COUNTERS OF THE DTC LINK	-

Table 1 SRUST (0x04): SRU status

BIT	NAME	MEANING
[0]	BUSYFLAG	Busy flag.
[1]	ALTROFULL	ALTRO multi-event buffers are full.
[2]	TTCREADY	Status of TTCrx chip
[3]	ETHSYNCST	Synchronization status of GbE link.
[4]	BRDCLKLOCKST	Lock state of board clock
[5]	RDOCLKLOCKST	Lock state of readout clock
[7:6]	DDL0 mode	"00" : link is down, not ready. "01" : Link is ready, no data transmission. "10" : Data is transmission on the link. "11": back-pressure is raised, no more data can be transmitted.
[9:8]	DDL1 mode	
[11:10]	-	Reserved
[12]	TRIGERR0	L1 received without L0
[13]	TRIGERR1	L1 arrived earlier than expected
[14]	TRIGERR2	L2 timeout
[15]	TRIGERR3	L2 arrived earlier than expected
[16]	TRIGERR4	L2 received without L0 or L1
[19:17]	-	Reserved
[20]	PSSCAN_FLAG	1'b1: PSSCAN is on progress
[29:21]	-	Reserved
[30]	TrigBusy	SRU internal BUSY flag
[31]	-	Reserved

Table 2 FPGAMonReg (0x07): SRU Monitor Register

BIT	NAME	MEANING	DEFAULT
[15:0]	TEMP	Reg0x7[15:0]/64/1024*503 - 273	-
[21:16]	RegAddr		-
[30:22]	Reserved	-	
[31]	Alarm	Raised when FPGA temperature exceeds 85 C.	-

Table 3 PSSCAN (0x11): Phase scan command

BIT	NAME	MEANING	DEFAULT
[15:0]	PSRESO	Phase scan resolution (29.7 ps/count)	16'h0011 (~0.5 ns)
[16]	PSMODE	Auto mode (1'b0)/Manual mode (1'b1)	1'b0
[23:17]	-	Reserved	
[29:24]	DTC_MON_SEL	Select reference DTC port for monitor	6'h0 (DTC0)
[31:30]	-	Reserved	

Table 3 SRUCFG (0x20): Configuration

BIT	NAME	MEANING	DEFAULT
[0]	CLKSRCSEL	1'b0: Always use board clock.	1'b1

		1’b1: Use TTC clock if it is ready, otherwise use board clock.	
[3:1]	BUFTH	Number of multi-buffers	3’h4
[5:4]	TRIGMODE	2’b00: Software trigger; 2’b01: Hardware trigger 2’b10: TTC trigger	2’b0
[6]	BUSYINEN[0]	Enable (1’b1)/Disable (1’b0) BUSY input of PX18	1’b0
[7]	BUSYINEN[1]	Enable (1’b1)/Disable (1’b0) BUSY input of PX17	1’b0
[15:8]	-	Reserved	8’h0
[23:16]	ParReq	Pause-And-Reset (PAR) procedure	8'h0
[29:24]	-	Reserved	6'h0
[30]	RdoStartOpt	1'b0: Start ALTRO readout after L1 trigger. 1'b1: Start ALTRO readout after L2a trigger.	1'b0
[31]	CDHVer	1'b0: CDHV2.0; 1'b1: CDHV3.0	1'b0

Table 4 TRIGL1TW (0x29): Time windows of level-1 trigger

BIT	NAME	MEANING	DEFAULT
[15:0]	L1TWL	Low threshold of L1 trigger time window (25 ns/count)	16’h0078
[31:16]	L1TWH	High threshold of L1 trigger time window (25 ns/count)	16’h012C

Table 5 TRIGL1TW (0x2A): Time windows of level-2 trigger

BIT	NAME	MEANING	DEFAULT
[15:0]	L2TWL	Low threshold of L2 trigger time window (25 ns/count)	16’h00C8
[31:16]	L2TWH	High threshold of L2 trigger time window (25 ns/count)	16’h4E20

Table 6 FEEFASTCMD (0x41): Fast command to FEE

Value	Meaning
32’h0000 00E8	Reset FEE
32’h0000 00E9	Request FEE status
32'h0000 00E4	SCLKSYNC, ALTRO sampling clock synchronization command

Table 7 PTRIGCFG (0x50): Periodical software triggers configuration

BIT	NAME	MEANING	DEFAULT
[15:0]	Period	Period of periodical test trigger sequences (25 ns/count)	16’ h4E20 (500 us)
[16]	Switch	Switch On (1’b1); Switch Off (1’b0).	1’h0
[31:17]	-	Reserved	15’h0

Table 8 TESTTRIGCFG0 (0x51): Test trigger configuration 0

BIT	NAME	MEANING	DEFAULT
[15:0]	Fake L0 Latency	Latency of fake L0 trigger (25 ns/count)	16’h0064
[31:16]	L1 latency	Latency of L1 trigger (25 ns/count)	16’h12C0

Table 9 TESTTRIGCFG1 (0x52): Test trigger configuration 1

BIT	NAME	MEANING	DEFAULT
[15:0]	L2 Latency	Latency of L2 trigger (25 ns/count)	16'h1770
[19:16]	TrigSeqSet	Trigger sequence setting. L2-L1-L0(fake)-L0	16'h000d
[31:20]	Reserved	-	-

Table 10 DDLDEBUGREG0/1 (0x72/0x73): DDL interface debug registers

BIT	MEANING	DEFAULT
[14:0]	DDL FSM ST	
[23:15]	9'h0	
[24]	filf_n: (I) DDL flow control. '0': back-pressure is raised	
[25]	siu_fidir: (I)Direction. '1': SRU-->LDC	
[26]	fiben_n: (I) DDL bus enable. '0': bus is enabled	
[27]	fbctrl_n: (IO) DDL bus control signal. '0': ddl command is on transmission.	
[28]	fbten_n: (IO) '1': No data and command is on transmission over DDL	
[31:29]	3'b0	

4 FEE Register Table

For information regarding how to read and write different registers (FEE FPGA and ALTRO), please see SRU documentation/manual.

FEE FPGA Register Definition (FMVER: 0x5043)			
Reg. Name	Reg. Addr(Hex)	Access Type	Meaning
REGEN	01	R/W	Enable power regulator
LGSEN	02	R/W	LG suppression Enable
PHYADDR	03	R/W	FEE physical address
TEMPTH	05	R/W	High temperature threshold, 1 C/ADC
CSPMK0	06	R/W	CSP0—15 mask
CSPMK1	07	R/W	CSP16—31 mask
HGST0	08	R	Saturation status of HG0—15
HGST1	09	R	Saturation status of HG16—31
EREG0	0A	R	General error flags
ErrFpgaCmd	0B	R	Error info of last invalid FPGA command
ErrALTCmd	0C	R	Error info of last invalid ALTRO command
ErrALTRdo	0D	R	Error info of last failed Readout operation
CNTRST	1B	W	Clear counters
HVLOAD	1E	W	Load HV values to DAC
ERRCLR	1F	W	Clear error flags
FMVER	20	R	Firmware version
L0CNT	21	R	L0 trigger counter
L1CNT	22	R	L1 trigger counter
L2ACNT	23	R	L2a (Readout Command) trigger counter
L2RCNT	24	R	L2r (Reject Command) trigger counter
EOCNT	25	R	Number of events sent out
CMDCNT	26	R	Number of received FPGA+ALTRO commands
ADCST	50 - 5E	R	15 ADC values
HVBIAS	60 - 7F	R/W	32 channels HV bias setting 0x60-0x67: CSP 23 down to CSP 16 0x68-0x6F: CSP 0 to CSP 7 0x70-0x77: CSP 8 to CSP 15 0x78-0x7F: CSP 31 down to CSP 24
S/N	80	R	FEE card Serial Number

REGEN(0x1): Power regulator Enable (“1”)/Disable(“0”)

Bit	Meaning	Default
0	ALTRO power (OFF=0, ON=1)	ON
1	HV Bias power (OFF=0, ON=1)	ON
2	Shaper power (OFF=0, ON=1)	ON
[15:3]	Unused	0

LGSEN(0x2): LG suppression Enable (“1”)/Disable (“0”)

Bit	Meaning	Default
0	LG suppression (OFF=0, ON=1)	ON
[15:1]	Unused	0

PHYADDR(0x3): LG suppression Enable (“1”)/Disable (“0”)

Bit	Meaning	Default
[3:0]	GTL position (0-9 for EMCal)	0
[4]	Branch (A=0, B=1)	A
[15:5]	Unused	0

TEMPTH(0x4): Temperature threshold. The TOI (Temperature Over Indicator: ***EREG0 [2:0]***) become high respectively if the related temperature sensor exceeds this threshold. Three sensors work independently.

Bit	Meaning	Default
[7:0]	Temperature threshold (1 C/ADC)	75 C
[15:8]	Unused	0

CSPMK0 (0x6), ***CSPMK1***(0x7): Readout mask. “1”: Do NOT readout the associated CSP channel.

Bit	Associated CSP numbering	Meaning	Default
0x6[0]	CSP0	Unmask=0; Mask=1	Unmasked
0x6[1]	CSP1	Unmask=0; Mask=1	Unmasked
…	…	Unmask=0; Mask=1	Unmasked
0x6[15]	CSP15	Unmask=0; Mask=1	Unmasked
0x7[0]	CSP16	Unmask=0; Mask=1	Unmasked
…	…	Unmask=0; Mask=1	Unmasked
0x7[14]	CSP30	Unmask=0; Mask=1	Unmasked
0x7[15]	CSP31	Unmask=0; Mask=1	Unmasked

HGST0 (0x8), ***HGST1***(0x9): HG saturation state. “1”: HG of related CSP channel is saturated.

0x7[15]	…	0x7[1]	0x7[0]	0x6[15]	…	0x6[1]	0x6[0]
CSP31	…	CSP17	CSP16	CSP15	…	CSP1	CSP0

EREG0(0x0A): General error flags

bit	Meaning
0	Temperature1 overflow indicator (TOI1)
1	Temperature2 overflow indicator (TOI2)
2	Temperature3 overflow indicator (TOI3)
3	Shaper power error
4	HV bias power error
5	ALTRO power error
6	Main power error
7	ErrFpgaCmd[14]: Invalid Command error flag
8	ErrALTCmd[12]: ACK is not released on the ALTRO bus
9	ErrALTCmd[13]: ACK is not asserted on the ALTRO bus
10	ErrALTCmd[14]: Invalid ALTRO command flag
11	ErrALTRdo[15]: ACK is not asserted
12	ErrALTRdo[14]: TRSFN is not asserted
13	ErrALTRdo[13]:TRSFN is not released
14	Unused
15	The "OR" of all typesof errors

ErrFpgaCmd(0x0B): Error info of last invalid FPGA command

bit	Meaning
13~0	The last invalid command address
14	Invalid Command error flag
15	R/W flag

ErrALTCmd(0x0C): Error info of last invalid ALTRO command

bit	Meaning
4--0	ALTRO command
8--5	ALTRO channel address
11--9	ALTRO chip address
12	ACK is not released on the ALTRO bus
13	ACK is not asserted on the ALTRO bus
14	Invalid ALTRO command flag
15	R/W flag

ErrALTRdo(0x0D): Error info of last invalid ALTRO command

bit	Meaning
3--0	ALTRO channel address
6--4	ALTRO chip address
12--7	Unused
13	TRSFN is not released
14	TRSFN is not asserted
15	ACK is not asserted

All ADC registers are 10-bit wide.

ADC ID	Memory location name	Addr.	Description	Conv. factor
ADC 0	TEMP1	0x50	Temperature for ADC IC13	0.25°C * ADC counts
	D4V0	0x51	4.0V Digital Voltage	8.04mV * ADC counts
	D4V0C	0x52	4.0V Digital Current Alternatively Voltage level used for current calc.	29.8mA * ADC counts
	D3V3	0x53	3.3V Digital Voltage	6.44 mV * ADC counts
	D3V3C	0x54	3.3V Digital Current Alternatively Voltage level used for current calc.	42.9 mA * ADC counts
ADC 1	TEMP2	0x55	Temperature for ADC IC15	0.25°C * ADC counts
	A6nV0	0x56	-6.0V Analog Voltage	4.88mV * ADC counts / 1000 - 8.2V
	A6nV0C	0x57	-6.0V Analog Current Alternatively Voltage level used for current calc.	29.3mA * ADC counts
	A6pV0	0x58	6.0V Analog Voltage *Default Data Value: 0x1E8 (= 5.6 V)*	11.4 mV * ADC counts
	A6pV0C	0x59	6.0V Analog Current Alternatively Voltage level used for current calc.	34.73 mA * ADC counts
ADC 2	TEMP3	0x5A	Temperature for ADC IC14	0.25°C * ADC counts
	A3V3	0x5B	3.3V Analog Voltage	6.44 mV * ADC counts
	A3V3C	0x5C	3.3V Analog Current Alternatively Voltage level used for current calc	42.9 mA * ADC counts
	A13V0	0x5D	13.0V Analog Voltage	26.8 mV * ADC counts
	A13V0C	0x5E	13.0V Analog Current Alternatively Voltage level used for current calc	22.3 mA * ADC counts

5 CSP <----> HG/LG channel mapping

CSP No.	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
HG No.	7'h2a	7'h2e	7'h25	7'h21	7'h31	7'h35	7'h3e	7'h3a
LG No.	7'h2b	7'h2f	7'h24	7'h20	7'h30	7'h34	7'h3f	7'h3b
CSP No.	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
HG No.	7'h0a	7'h0e	7'h05	7'h01	7'h41	7'h45	7'h4e	7'h4a
LG No.	7'h0b	7'h0f	7'h04	7'h00	7'h40	7'h44	7'h4f	7'h4b
CSP No.	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**
HG No.	7'h28	7'h2c	7'h27	7'h23	7'h33	7'h37	7'h3c	7'h38
LG No.	7'h29	7'h2d	7'h26	7'h22	7'h32	7'h36	7'h3d	7'h39
CSP No.	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
HG No.	7'h08	7'h0c	7'h07	7'h03	7'h43	7'h47	7'h4c	7'h48
LG No.	7'h09	7'h0d	7'h06	7'h02	7'h42	7'h46	7'h4d	7'h49

6 ALTRO SCLK (sampling clock) synchronization and detection

a) Synchronize 10 MHz SCLK in all SRUs before data taking

Send a SCLKSYNC command (page 6 of SRU manual) to SRU, SRU will broadcast this command to all FEE cards, then all the SCLK generators in FEE will be reset and synchronized to same phase.

b) Detect the time stamp of the SCLKSYNC command

Since the SCLKSYNC commands are sent in different SRU at different time. So, it is necessary to detect the time when SRUs send SCLKSYNC to FEEs.

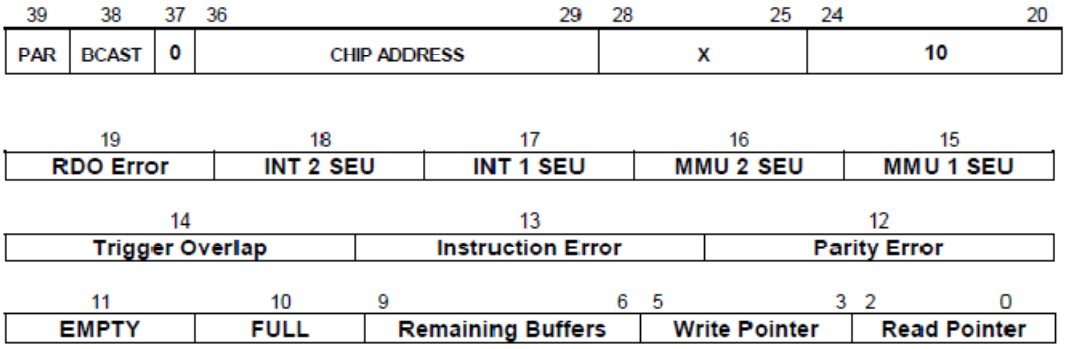
There is a counter in SRU, it will be reset when SRU receives TTC bunch clock reset command. Therefore, these counters in all the SRU are synchronized. SRU will record the counter value when it broadcast SCLKSYNC command to FEEs.

7 Frequently used ALTRO Registers

From ALTRO user manual; available athttp://cern.ch/ep-ed-alice-tpc/altro_chip.htm
For information regarding how to read and write different ALTRO registers, please see SRU documentation/manual.

Reg. Name	Reg. Addr	Access Type	Per Channel/ Global	Meaning
VFPED[1]	06	R+R/W	Per Channel	Variable/Fixed pedestal data
ADEVL	11	R	Per Channel	Chip address + Event length
ZSTHR[1]	08	R/W	Global	Offset + Threshold ZS
TRCFG[1]	0A	R/W	Global	Trigger Delay + N.Samples/Event
DPCFG[1]	0B	R/W	Global	ZSU +MAU + BSU configuration
BFNPT[1]	0C	R/W	Global	Filter Enable + Buffer.N. + Pre-trigger
ERSTR	10	R	Global	Error + Status register
TRCNT	12	R	Global	L0 Trigger Counter
TRCLR	1C	W	Global	Clear Trigger Counter
ERCLR	1D	W	Global	Clear Error Flags

ERSTR Register bit encoding



Parameter	Description
Read Pointer	Pointer to the buffer that is to be read out
Write Pointer	Pointer to the buffer that is to be written on next trigger
Remaining Buffers	Number of empty buffers remaining in the Data Memory
FULL	Flag signalling that all the buffers of the memory are filled with valid event
EMPTY	Flag signalling that all the buffers of the memory are available for writing
Parity Error	A parity error has been detected while decoding an instruction (sticky bit)
Instruction Error	An illegal instruction has been received (sticky bit)

Trigger Overlap	A trigger pulse has been received during the processing window of a previous trigger (sticky bit)
MMU 1 SEU	One Single Event Upset has been detected in the state machine that controls the buffers of the Data Memory (sticky bit)
MMU 2 SEU	Two Single Event Upsets have been detected in the state machine that controls the buffers of the Data Memory
INT 1 SEU	One Single Event Upset has been detected in the state machine that controls the interface to the external bus (sticky bit)
INT 2 SEU	Two Single Event Upsets have been detected in the state machine that controls the interface to the external bus (sticky bit)
RDO Error	A readout command has been received when there was nothing to read out. (sticky bit)

Notes

- Single Event Upsets (SEU) will only occur in the presence of radiation. If a SEU happens, the affected state machine will recover automatically. If a double SEU is detected, the corresponding state machine has interrupted its logical sequence and gone to idle state. The chip must therefore be reset when possible.
- All of the error bits are sticky, that is, they remain in the "1" state after they are set. The error bits are reset when the chip is reset or powered off or the ERCLR command is issued.
- When running in 4-buffer mode, the Write Pointer and Read Pointer can only take the values 0, 2, 4 or 6. In the 8-buffer mode, they take all values between 0 and 7.