SRU Gbe Detector Control Specification Draft for AIDA/LCTPC

Description: This document is written for DCS software designer and SRU firmware designers for AIDA LCTPC.

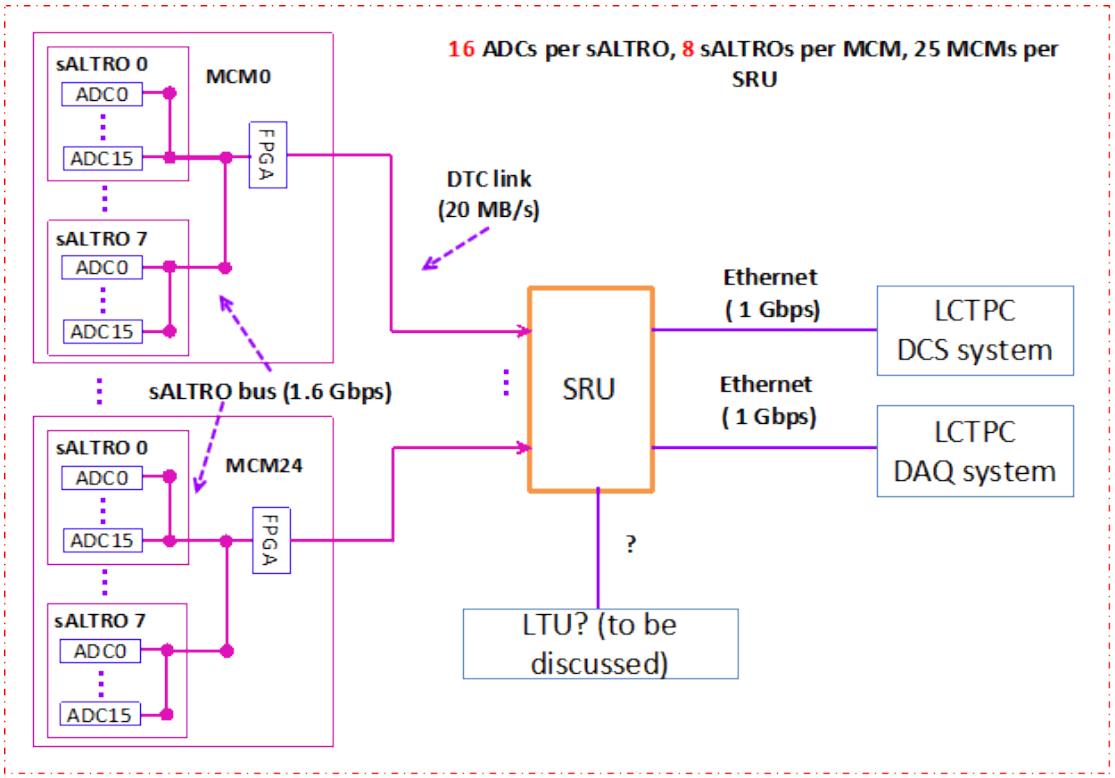
Last modified: 2014-3-26

Contact info: Fan.Zhang (fanzhang.ccnu@gmail.com)

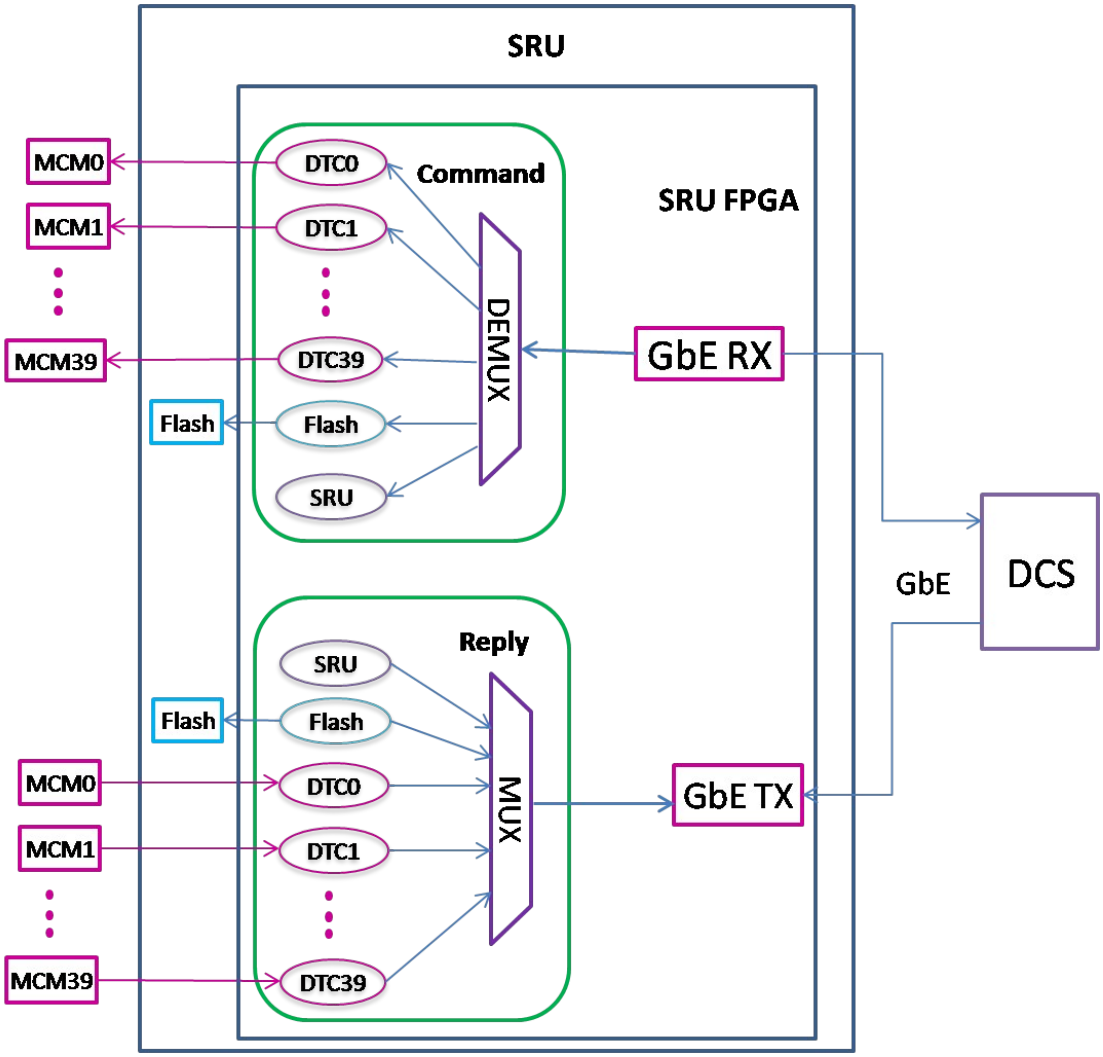
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1. SRU readout configuration for AIDA LCTPC



2. DCS Control concept in the SRU



The SRU is able to receive and transmit UDP packets to the DCS server at the same time. Each SRU manages 42 slave DCS nodes, including the SRU itself, a Flash controller and 40 DTC controllers. UDP port numbers and message headers are used to address different nodes. Each UDP slave node has its own receiving and transmitting multi-frame buffers.Polling mechanism is used in the multiplexer (MUX) of the UDP transmitter, the UDP MUX checks all the UDP transmitting buffers in successive cycles, and transmits one UDP frame once the selected buffer is not empty.

3. DCS-->SRU Frame Structure

The UDP source port of the SRU/DTC command frame is not checked currently, it could be any value. The UDP destination port should be 0x1001 (4097 in decimal digits).

The frame structure of commands for the SRU and DTC nodes are shown in the Table 1.

Table SRU/DTC command frame structure

32 bits				
NodeSel	11’b0			NodeSelH[20:0]
NodeSel	12’b0			NodeSelL[19:0]
CmdAddr	WR(1-bit)	Ctype (1-bit)		CmdAddr[29:0]
CmdData			CmdData[31:0]	
			…	
CmdAddr	WR(1-bit)	Ctype (1-bit)		CmdAddr[29:0]
CmdData			CmdData[31:0]	

The fragmentation is disabled during the UDP packet transmission over the network. And the jumbo frame[1] is enabled in the SRU Ethernet MAC. The payload of the standard Ethernet frame cannot be longer than 1500 bytes; the jumbo frame can carry up to 9000 bytes of payload. Currently, the depth the buffer in the SRU is less 4096 bytes (Could be extended when it is necessary). Therefore, the maximum commands number in a single command frame is 500 (Leave some bytes of space for the frame overhead).

NodeSel

This field has 41 active bits, corresponding to 41 slave DCS nodes, including one SRU node and 40 DTC nodes (see Figure 1).The 21st bit (NodeSelH[20]) maps to the SRU; NodeSelH[19:0] maps to DTC39 ~DTC20; NodeSelL[19:0] maps to DTC19 ~ DTC0. If the corresponding bit is set, this command frame will be forwarded to the command buffers in the mapped slave DCS nodes.

WR

This field specifies the operation type of the command:
“1” : Read command;
“0” : Write command.

Ctype

This field specifies the type of child node on the FEE board.
“1”: ALTROs
“0”: FEE FPGA

CmdAddr[29:0]

The structure of this field depends on the type of the nodes.
SRU: this field is a 30 bit register address (See Table).
FEE FPGA:

14’b0	Addr[15:0] (16 bit register address)

ALTRO:

1http://en.wikipedia.org/wiki/Jumbo_frame

10’b0	ALTRO command addr[19:0]

ALTRO command address (Compatible with the format defined in the ALTRO manual)

19	18	17	[16:12]	[11:9]	[8:5]	[4:0]
1’b0	BCAST	1’b0	FEE addr	ALTRO addr	Channel addr	Register Addr

BCAST

“1”: Commands are broadcast to all of 64 ALTRO channels in this FEE card.

“0”: BCAST is disabled.

FEE addr: The value in this field should be SAME as the value in the FEE address register (0x3, see details in the table)

ALTRO addr: There are 4 ALTROs on the FEE board. Their addresses are 0x0, 0x2, 0x3, 0x4.

Channel addr: This field is used to address 16 channels in the ALTRO.

Register addr: The ALTRO register has 5 bits, the detailed information is listed in the table.

CmdData

This field is a 32-bit data field. For the read command, it could be any value.

4. SRU-->DAQ Frame Structure

The UDP source port is 0x1001 (4097 in decimal digits). The SRU/DTC reply frame has a fixed length (8 bytes); it only contains one register address and its value. The node address will be added into the reply message when the UDP tool of the FEE server is updated.

Table SRU/DTC reply frame structure

32 bits
Read command(register address)
Register value

5. Frame examples with explanation

- **Read SRU version registers**

```
10.160.36.156  #   IP
4097           #UDP  port
00100000       #  Node  Sel:  Select  SRU  node(Bit  40  is  '1').
00000000       #                Node                 Sel
80000003       #  Address  word:  Read  SRU  register  0x3
00000000       # Data word
```

  - **SRU replies value of SRU version register 0x3, only 8 bytes in the UDP payload**

```
80000003       #  Address  word:  Read  SRU  register  0x3
```

14032601 # Data word: SRU version = 0x14032601 (means 2014-03-26 version 01)

- **Write SRU version registers 0x23 (**Readout mask of DTC0-19 links**)**

  10.160.36.156 # IP
  4097 #UDP port
  00**1**00000 # Node Sel: Select SRU node(Bit 40 is '1').
  00000000 # Node Sel
  00000023 # Address word: Write SRU register 0x23
  0000000F # Data word: 0x0000_000F, mask DTC0~3 in the readout list

- **Read and Write multiple registers in the MCM connected to DTC0**

```
10.160.36.156  #   IP
4097           #UDPport
00000000       #                Node                Sel:
00000001       #      Node      Sel:      Select      DTC0      node
80000020       # Address word: Read CPLD on MCM register 0x20
00000000       # Data word:
C0000010       #   Address   word:   Read   sALTRO   register   0x10
00000000       # Data word:
00000060       # Address word: Write CPLD on MCM register 0x60
00000210       # Data word: 0x0210
4000000A       #   Address   word:   Write   sALTRO   register   0x0A
00000210       # Data word: 0x00210
......
(Maximum number of commands in a single frame: 500)
```

6. Flash command frame

SRU has two codes: a common boot code which stored in the small PROM chip on the SRU, and the application-specific user code that stored in the large Flash. Boot code only has Ethernet connection and Flash write/read function. It is used to program the load application-specific user code into big Flash on SRU via Ethernet connection.

The SRU boot code are wrote by Sorin. He uses different frame format from us. Here are two examples and its comments. These scripts are only used for program IP address into Flash. They are only used when one prepare a new SRU.

- **WIPHtoFlash.txt, Remember to modify the IP address you want to set into Flash**

```
10.160.132.121    #IP
10103             #UDPport
ec307132          #RequestID
800000e8          #SubAddress
aabbffff          #CmdType
00ffc001          #Flashaddress
0000aa0           # IP addr high 16-bit ("0aa0" stands for 10.160)
```

- **WIPLtoFlash.txt, Remember to modify the IP address you want to set into Flash**

```
10.160.132.121    #IP
10103             #UDPport
ec307132          #RequestID
```

```
800000e8        #SubAddress
aabbffff        #CmdType
00ffc000        #Flashaddress
0000249C        # IP address low 16-bit ("249C" stands for 36.156)
```

7. Latest SRU register tables

Group 1: Registers for Normal Readout Setup and Monitoring				
NAME	ADDR	TYPE	MEANING	DEFAULT VALUE(HEX)
Status				
S/N	01	R	Serial Number	-
IP	02	R	IP address	-
FMVER	03	R	Firmware version	-
SRUST	04	R	Status	-
DTCERRFLAG[19:0]	05	R	Error flag received from DTC0-19	-
DTCERRFLAG[39:20]	06	R	Error flag received from DTC20-39	-
Command				
RESET	10	W	Reset SRU and FEE and ALTRO	-
PSSCAN	11	W	Phase scan command	0x64
WALIGN	12	W	DTC link word alignment command	
SCLKSYNC	13	W	DTC clock synchronization command	-
Configurations				
SRUCFG	20	R/W	Configuration Registers	0000 0008
DTCCLKEN[19:0]	21	R/	Clock switch of DTC0-19 links	000 FFFFF

		W		
DTCCLKEN[39:20]	22	R/W	Clock switch of DTC20-39 links	000 00000
DTCRDOMASK[19:0]	23	R/W	Readout mask of DTC0-19 links	000 FFFFE
DTCRDOMASK[39:20]	24	R/W	Readout mask of DTC20-39 links	000 FFFFF
ALTROCFG[19:0]	27	R/W	Copy of ALTRO CFG1	000 00000
ALTROCFG[39:20]	28	R/W	Copy of ALTRO CFG2	000 00000
TRIGL1TW	29	R/W	Time windows of level-1 trigger	012C 0078
TRIGL2TW	2A	R/W	Time windows of level-2 trigger	4E20 00C8

Group 2: Registers for Debugging Purpose

NAME	ADDR	TYPE	MEANING	DEFAULT VALUE(HEX)
Commands				
FPGARELOAD	40	W	Reload firmware from Flash to FPGA	-
FEEFASTCMD	41	W	Fast command to FEE	-

STRIGCMD	42	W	Send one software trigger sequence	-
TRIGCNTCLR	43	W	Clear all trigger counters	-
TRIGERRCLR	44	W	Clear all trigger errors	-
Configuration				
PTRIGCFG	50	R/W	Periodical software triggers configuration	0000 0320
TESTTRIGCFG0	51	R/W	Test trigger configuration 0	00d4 0064
TESTTRIGCFG1	52	R/W	Test trigger configuration 1	000d 0190
Status				
RXL0CNT	60	R	Number of received L0 triggers by SRU	-
RXL1CNT	61	R	Number of received L1 triggers by SRU	-
RXL2ACNT	62	R	Number of received L2a triggers by SRU	-
RXL2RCNT	63	R	Number of received L2r triggers by SRU	-
TXL0L1CNT	64	R	Number of transmitted L0_L1 triggers to FEE	-
TXL2ACNT	65	R	Number of transmitted L2a triggers to FEE	-
TXL2RCNT	66	R	Number of transmitted L2r triggers to FEE	-

TRIGERRCNT	67	R	Number of invalid trigger sequences	-
DTCERRFLAG0	68	R	DTC test error flag of DTC0-19 links	-
DTCERRFLAG1	69	R	DTC test error flag of DTC20-39 links	-
L2ABUNCNT	6A	R	Bunch counter in last L2a message	-
L2AORBCNT	6B	R	Orbit counter in last L2a message	-
DDL0BUNCNT	6C	R	Bunch counter in last DDL0 CDH	-
DDL0ORBCNT	6D	R	Orbit counter in last DDL0 CDH	-
DDL1BUNCNT	6E	R	Bunch counter in last DDL1 CDH	-
DDL1ORBCNT	6F	R	Orbit counter in last DDL1 CDH	-
DDLBPCNT0	70	R	DDL0 back pressure counter	-
DDLBPCNT1	71	R	DDL1 back pressure counter	-
ECDEBUGREG0	72	R	DDL0 Event concentrator debug register	-
ECDEBUGREG1	73	R	DDL1 Event concentrator debug register	-
TRIGDEBUGREG	74	R	L2 trigger FSM debug register	-
DDL0ECNT	75	R	Number of transmitted event over DDL0	-
DDL1ECNT	76	R	Number of transmitted event over DDL1	-

ALTRODEBUG	77	R	ALTRO debug register	-
ABUSYCNT	78	R	ALTRO busy counter	-
BUSYCNT	79	R	BUSY counter	-
				-
DRXDATA	1028-104F	R	Data over DTC link	-
DERRCNT	10A0-10CF	R	ERROR COUNTERS OF THE DTC LINK	-
DRXDEBUGREG	10C8-10EF	R	DTC RX DEBUG REGISTERS	-

2 Register coding

Table SRUST (0x04): SRU status

BIT	NAME	MEANING
[0]	BUSYFLAG	Busy flag.
[1]	ALTROFULL	ALTRO multi-event buffers are full.
[2]	TTCREADY	Status of TTCrx chip
[3]	ETHSYNCST	Synchronization status of GbE link.
[4]	BRDCLKLOCKST	Lock state of board clock
[5]	RDOCLKLOCKST	Lock state of readout clock
[6]	DDL0ST0	DDL0 link on/off
[7]	DDL0ST1	DDL0 is ready for receive event data

[8]	DDL0ST2	DDL0 synchronized
[9]	DDL1ST0	DDL1 link on/off
[10]	DDL2ST1	DDL1 is ready for receive event data
[11]	DDL3ST2	DDL1 synchronized
[12]	TRIGERR0	L1 received without L0
[13]	TRIGERR1	L1 arrived earlier than expected
[14]	TRIGERR2	L2 timeout
[15]	TRIGERR3	L2 arrived earlier than expected
[16]	TRIGERR4	L2 received without L0 or L1
[31:17]	-	Reserved

Table 2 PSSCAN (0x11): Phase scan command

BIT	NAME	MEANING	DEFAULT
[15:0]	PSRESO	Phase scan resolution (78 ps/count)	16’h0064
[16]	PSMODE	Auto mode (1'b0)/Manual mode (1'b1)	1'b0
[31:17]	Reserved	-	

Table 3 SRUCFG (0x20): Configuration

BIT	NAME	MEANING	DEFAULT
[0]	CLKSRCSE	1’b0: Use TTC clock when it is ready;	1’b0

	L	1’b1: Always use board clock.	
[4:1]	BUFTH	Number of multi-buffers	3’h4
[6:5]	TRIGMODE	2’b00: Software trigger; 2’b01: Hardware trigger 2’b10: TTC trigger	2’b0
[7]	BUSYINEN[0]	Enable (1’b1)/Disable (1’b0) BUSY input of PX18	1’b0
[8]	BUSYINEN[1]	Enable (1’b1)/Disable (1’b0) BUSY input of PX17	1’b0
[9]	DDLMASK[0]	Mask (1'b1) DDL0	1'b0
[10]	DDLMASK[1]	Mask (1'b1) DDL1	1'b1
[31:1]	-	Reserved	22’h0

Table 4 TRIGL1TW (0x29): Time windows of level-1 trigger

BIT	NAME	MEANING	DEFAULT
[15:0]	L1TWL	Low threshold of L1 trigger time window (25 ns/count)	16’h0078
[31:16]	L1TWH	High threshold of L1 trigger time window (25 ns/count)	16’h012C

Table 5 TRIGL1TW (0x2A): Time windows of level-2 trigger

BIT	NAME	MEANING	DEFAULT
[15:0]	L2TWL	Low threshold of L2 trigger time window (25 ns/count)	16’h00C8

[31:16]	L2TWH	High threshold of L2 trigger time window (25 ns/count)	16'h4E20

Table 6 FEEFASTCMD (0x41): Fast command to FEE

Value	Meaning
32'h000000E6	Switch on PRBS test mode
32'h000000E7	Switch off PRBS test mode
32'h000000E8	Reset FEE
32'h000000E9	Request FEE status

Table 7 PTRIGCFG (0x50): Periodical software triggers configuration

BIT	NAME	MEANING	DEFAULT
[15:0]	Period	Period of periodical test trigger sequences (25 ns/count)	16'h0320
[16]	Switch	Switch On (1'b1); Switch Off (1'b0).	1'h0
[31:17]	-	Reserved	15'h0

Table 8 TESTTRIGCFG0 (0x51): Test trigger configuration 0

BIT	NAME	MEANING	DEFAULT
[15:0]	Fake L0 Latency	Latency of fake L0 trigger (25 ns/count)	16'h0064

[31:16]	L1 latency	Latency of L1 trigger (25 ns/count)	16’h00d4

Table 9 TESTTRIGCFG1 (0x52): Test trigger configuration 1

BIT	NAME	MEANING	DEFAULT
[15:0]	L2 Latency	Latency of L2 trigger (25 ns/count)	16’h0064
[19:16]	TrigSeqSet	Trigger sequence setting. L2-L1-L0(fake)-L0	16’h000d
[31:20]	Reserved	-	-