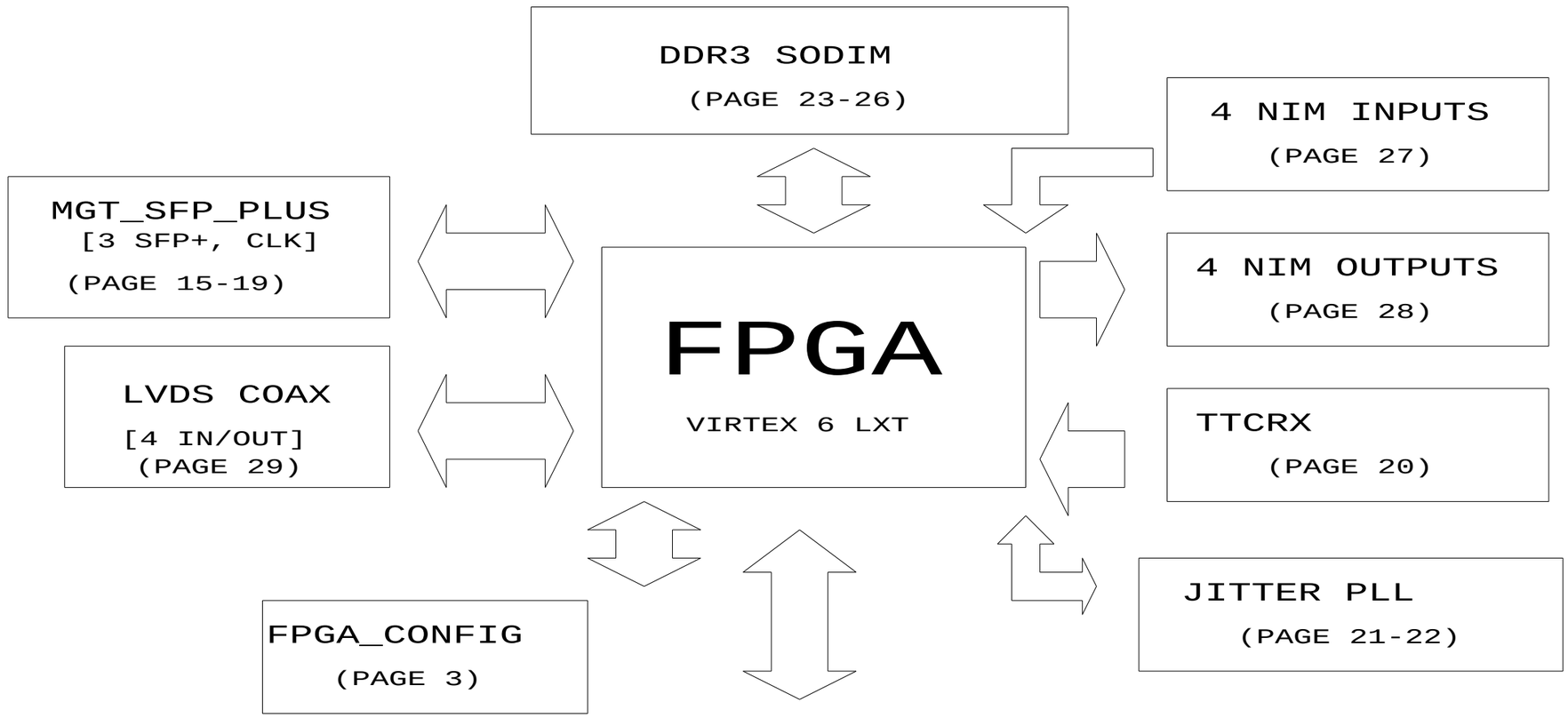


TO DO	STATUS
FIX VARIOUS BUGS	VERIFICATION
CONFIGURATION	
ADD XILINX XL FLASH	DROPPED
REPLACE BPI FLASH	DROPPED
ADD SPI FLASH	DROPPED
FRONTPANEL LEDS	DONE
10GB ETHERNET	DONE
JITTER CLEANER PLL	DONE
POWER BUDGET	

Project file:sru_rev2.cpm SYSTEM:

CERN TE/MPE
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND

PROJECT:SRU v2.0

MODULE:sru_top | Sheet: Module: 1/2 / Project: 1/81

LAST_MODIFIED=Wed Oct 12 12:58:56 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

HISTORY		
REVISION	NOTE	DESCRIPTION
REV2	1	FIX: CE AND OE EXCHANGED ADDED BCNTRES AND EVCNTRES

GND\G — GROUND\G

GND_POWER\G

FPGA

LVDS_40X_RJ45
QUAD_RJ45_IO_P<159..0> — QUAD_RJ45_IO_P<0..159> (DTC LINKS)
QUAD_RJ45_IO_N<159..0> — QUAD_RJ45_IO_N<0..159>

LVDS_COAX
LVDS_VXX_E\G
VCC3V3_LVDS_E\G
LVDS_VXX, VCC3V3_LVDS
COAX_LVDS_IO_P<3..0> — COAX_LVDS_IO_P<3..0> (LVDS I/O)
COAX_LVDS_IO_N<3..0> — COAX_LVDS_IO_N<3..0>

NIM_INPUT
NIM_TO_TTL<3..0> — NIM_TO_TTL<3..0> (GP I/O)

NIM_OUTPUT
VCC6V0N_NIM
TTL_TO_NIM<3..0> — TTL_TO_NIM<3..0>

MGT_SFP_PLUS
SFP_RX_P<3..0> — SFP_RX_P<3..0> (HIGH SPEED INTERFACE)
SFP_RX_N<3..0> — SFP_RX_N<3..0>
GTX_125M_REFCLK_P — GTX_125M_REFCLK_P
GTX_125M_REFCLK_N — GTX_125M_REFCLK_N
SFP_REFCLK_P<1..0> — SFP_REFCLK_P<1..0>
SFP_REFCLK_N<1..0> — SFP_REFCLK_N<1..0>
SFP_TX_P<3..0> — SFP_TX_P<3..0>
SFP_TX_N<3..0> — SFP_TX_N<3..0>
SFP_SCL — SFP_SCL
SFP_SDA — SFP_SDA
SFP_RXLOS — SFP_RXLOS

JITTER_CLEANER
PLLOUT0_P, PLLOUT0_N — CLKOUT0_P, CLKOUT0_N
PLLOUT1_P, PLLOUT1_N — CLKOUT1_P, CLKOUT1_N
CLKIN0_P, CLKIN0_N — TTC_CLK40B_P, TTC_CLK40B_N
CLKIN1_P, CLKIN1_N — PLLIN1_P, PLLIN1_N
CLKIN_SEL — PLLCLK_SEL
CLKUWIRE, DATAUWIRE, LEUWIRE — PLL_CLKU, PLL_DATAU, PLL_LEU
SYNC_N — PLL_SYNC_N
PLL_LOCK — PLL_LOCK
VCC3V3_PLL — VCC3V3_DIG\G

PLLOUT0_P — PLLCLK0_P
PLLOUT0_N — PLLCLK0_N
PLLOUT1_P — PLLCLK1_P
PLLOUT1_N — PLLCLK1_N
CLKPLL_P
CLKPLL_N
PLLCLK_SEL
CLKUWIRE
DATAUWIRE
LEUWIRE
PLL_SYNC_N
PLL_LOCK
VCC1V0_MGTAVCC
VCC1V2_MGTAVTT

SPARE<11..0>

FPGA_CONFIG

CONFIG INTERFACE:
FPGA_DONE — FPGA_DONE
CONFIG_MODE_CHG_B — CONFIG_MODE_CHG_B
FPGA_INIT_B — FPGA_INIT_B
FPGA_DIN — FPGA_DIN
FPGA_CCLK — FPGA_CCLK
FPGA_PROGRAM_B — FPGA_PROGRAM_B
JTAG_RST_N — JTAG_RST_N
JTAG_TCK — JTAG_TCK
JTAG_TMS — JTAG_TMS
JTAG_TDO — JTAG_TDO
FPGA_TDI — FPAG_TDI
FLASH_D<15..0> — FLASH_D<15..0>
RS1 — RS1
RS0 — RS0
FLASHOE_B — FLASHOE_B
FLASHCS_B — FLASHCS_B
FLASHWE_B — FLASHWE_B
FLASH_A<22..0> — FLASH_A<22..0>

** CE AND OE EXCHANGED

TTCRX

TTC INTERFACE:
TTC_CLK40_P — TTC_CLK40_P
TTC_CLK40_N — TTC_CLK40_N
L1ACCEPT_P — L1ACCEPT_P
L1ACCEPT_N — L1ACCEPT_N
DBERRSTR_2V5 — DBERRSTR_2V5
SERIAL_B_2V5 — SERIAL_B_2V5
TTC_SCL — TTC_SCL
TTC_SDA — TTC_SDA
TTC_RESET_B_2V5 — TTC_RESET_B_2V5
DQ_NOR_2V5 — DQ_NOR_2V5
TTC_READY_2V5 — TTC_READY_2V5
DOUTSTR_2V5 — DOUTSTR_2V5
DOUT_2V5<7..0> — DOUT_2V5<7..0>
SADDR_2V5<7..0> — SADDR_2V5<7..0>
BCNTRES_2V5 — BCNTRES_2V5
EVCNTRES_2V5 — EVCNTRES_2V5

TTC_CLK40B_P — TTC_CLK40B_P
TTC_CLK40B_N — TTC_CLK40B_N
VCC5V0_HFBR — VCC5V0_HFBR

POWER_SUPPLIES

CONFIG_MODE_CHG_B
FPGA_PROGRAM_B
MON_OTI<2..0> — MON_OTI<2..0>
MON_I2C_SCL — MON_I2C_SCL
MON_I2C_SDA — MON_I2C_SDA
MON_CONVST — MON_CONVST
DDR_PS_EN — DDR_PS_EN
LVDS_E_PS_EN — LVDS_E_PS_EN
LVDS_W_PS_EN — LVDS_W_PS_EN

VCC_MGTAVTT — VCC_MGTAVTT_1V2
VCC_MGTAVCC — VCC_MGTAVCC_1V0
VCC5V0_HFBR
VCC6V0N_NIM

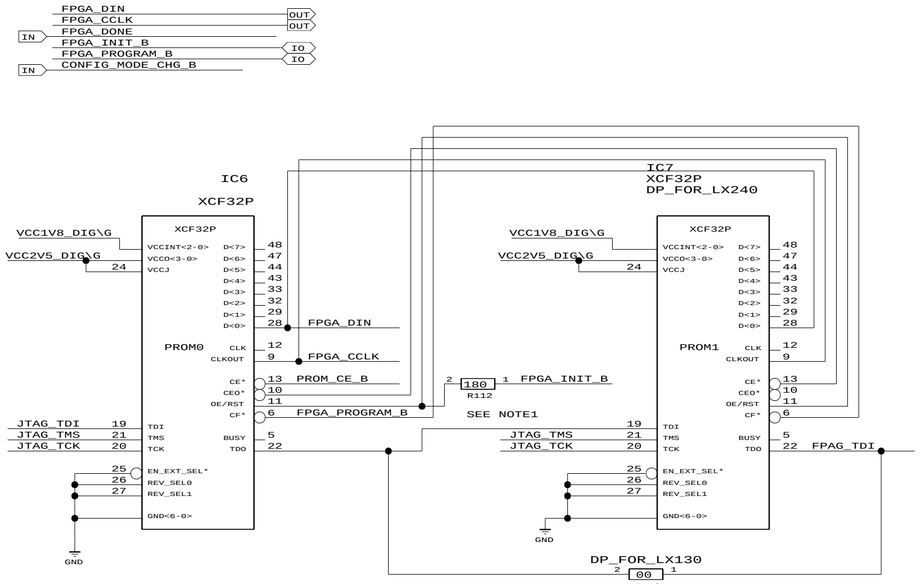
DDR3_INTERFACE

VCC1V5_DDR\G — VCC1V5
VCC3V3_DIG\G — VCC3V3
VCC_LEDS
VTTVDR_EN
VCC3V3_G0\G — VCC_LDO
VTTDDR_PG
SPARE<11..0>

R129 160K
R130 100
LD8 HSMY-C170
T13 SOT23 NDS331N

NOTE:
LD8 indicates the output of
DDR teminal regulator is GOOD

Project file:sru_rev2.cpm			SYSTEM:
European Organization for Nuclear Research, 1211 GENEVA 23, SWITZERLAND (TE/MPE)	PROJECT:SRU v2.0		
	MODULE:sru_top	Sheet: 2/2 (Module: / Project: 2/81)	
	LAST_MODIFIED=Fri Dec 09 11:01:29 2011		
	Design by: FZhang/SMartoiu	PCB by: EXT	DATE: 29/07/2010



XCF32P DECOMPRESSION SETUP--FPGA SLAVE MODE

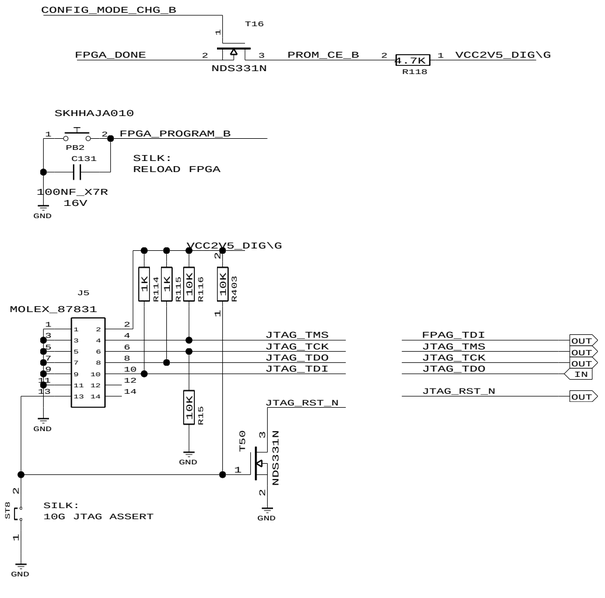
NOTE1

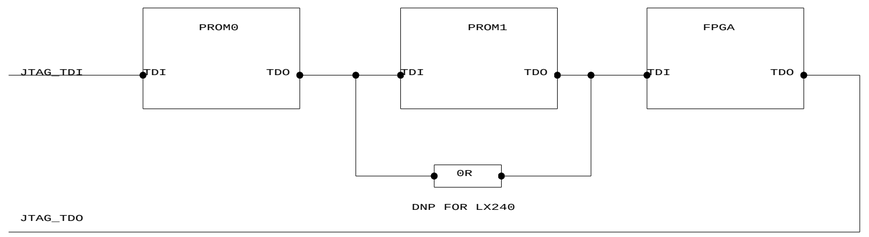
IN MASTER BPI-UP MODE,

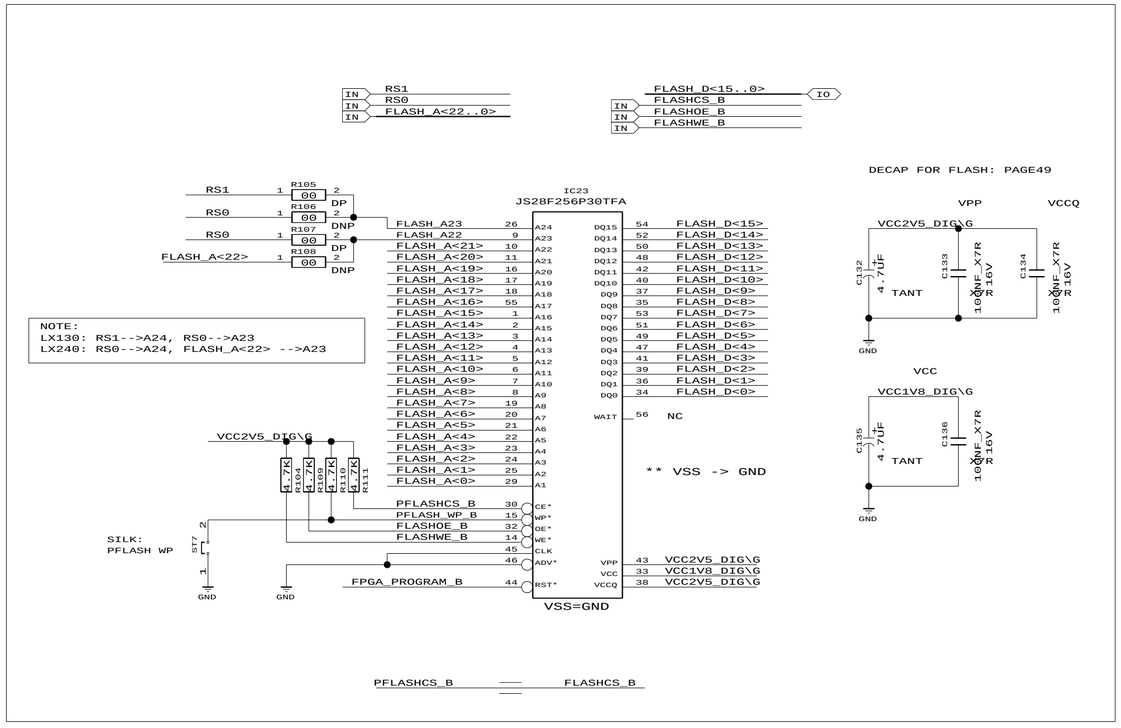
FPGA CCLK PIN MUST NOT BE DRIVEN OR TIED '1' OR '0'

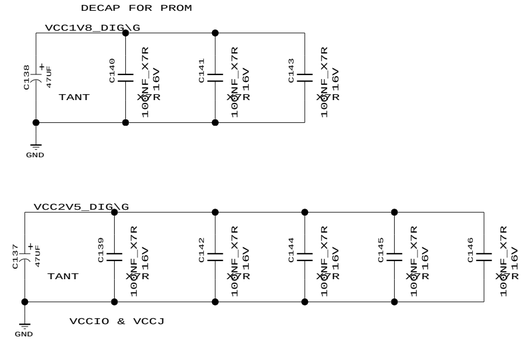
SO, I DRIVE BOTH PROMS IN RESET STATE AFTER POWER-ON CONFIGURATION OK.

GIVE 15 SECONDS FOR DEFAULT POWER ON CONFIGURATION BY LM3881









Project file:sru_rev2.cpm	SYSTEM:
European Organization for Nuclear Research, 1211 GENEVA 23, SWITZERLAND (TE/MPE)	PROJECT:SRU v2.0
MODULE:fpga_config	Sheet: 1/1 — Module: / Project: 3/81
LAST_MODIFIED=Fri Dec 09 11:02:04 2011	
Design by: FZhang/SMartoiu	PCB by: EXT — DATE: 29/07/2010

J17

OPTIONAL WIS OVERHEAD INTERFACE

SIL254D

3	3	GND\G
2	2	VCC2V5_WISDBG
1	1	VCC2V5_DIG\G

IO SPARE<11..0>

IC2

SN74AVC2T45DCU

VCC1V5_DDR\G, VCC2V5_WISDBG

74AVC2T45 (VCCA, VCCB, A1, A2, DIR, GND, B1, B2)

SPARE<11>	2	7	WIS_RCLKO
SPARE<10>	3	6	WIS_RFPO
GND\G	5		

GND

IC3

SN74AVC2T45DCU

VCC1V5_DDR\G, VCC2V5_WISDBG

74AVC2T45 (VCCA, VCCB, A1, A2, DIR, GND, B1, B2)

SPARE<9>	2	7	WIS_TCLKO
SPARE<8>	3	6	WIS_TFPO
GND\G	5		

GND

IC4

SN74AVC2T45DCU

VCC1V5_DDR\G, VCC2V5_WISDBG

74AVC2T45 (VCCA, VCCB, A1, A2, DIR, GND, B1, B2)

SPARE<7>	2	7	WIS_RDO
SPARE<5>	3	6	UART_RX
GND\G	5		

GND

IC34

SN74AVC2T45DCU

VCC1V5_DDR\G, VCC2V5_WISDBG

74AVC2T45 (VCCA, VCCB, A1, A2, DIR, GND, B1, B2)

SPARE<6>	2	7	WIS_TDAIN
SPARE<4>	3	6	UART_TX
VCC1V5_DDR\G	5		

GND

VCC1V5_DDR\G

C457 100NF_X7R 16V — GND
C458 100NF_X7R 16V — GND
C459 100NF_X7R 16V — GND
C460 100NF_X7R 16V — GND

VCC2V5_WISDBG

C464 100NF_X7R 16V — GND
C463 100NF_X7R 16V — GND
C462 100NF_X7R 16V — GND
C461 100NF_X7R 16V — GND

XAUI2SFP10GBE

FXTX_P<3..0>	XAUIRX_P<3..0>	FPGA_RCK_P	PHY10G_RCK_P
FXTX_N<3..0>	XAUIRX_N<3..0>	FPGA_RCK_N	PHY10G_RCK_N
FXRX_P<3..0>	XAUITX_P<3..0>	FPGA_VCK_P	PHY10G_VCK_P
FXRX_N<3..0>	XAUITX_N<3..0>	FPGA_VCK_N	PHY10G_VCK_N
		CLK64A_P	PHY10G_XCK_P
PHY10G_MDC	MDC	CLK64A_N	PHY10G_XCK_N
PHY10G_MDIO	MDIO		
PHY10G_RST_N	RESET_N	LASI	PHY10G_LASI
SFP_SCL	SCL_EPLL	WIS_INTA	PHY10G_INTA
SFP_SDA	SDA_EPLL		
		WIS_RCLKO	WIS_RCLKO
JTAG_TCK	JTAG_TCK	WIS_RDO	WIS_RDO
JTAG_TMS	JTAG_TMS	WIS_RFPO	WIS_RFPO
FPGA_TDO	JTAG_TDI	WIS_TCLKO	WIS_TCLKO
PHY10G_TDO	JTAG_TDO	WIS_TFPO	WIS_TFPO
JTAG_RST_N	JTAG_TRST_B	WIS_TDAIN	WIS_TDAIN

J6

SIL254D

3	3	FPGA_TDO	
2	2	JTAG_TDO	*!*
1	1	PHY10G_TDO	

Project file:sru_rev2.cpm SYSTEM:

European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

PROJECT:SRU v2.0

MODULE:fpga | Sheet: 1/7 | Module: | Project: 4/81

LAST_MODIFIED=Fri Dec 09 11:01:35 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

LX130 OR LX240

IC11
XC6VLX240T-1FFG1156CES

BANK 33

IO_L0P_33	AE13	QUAD_RJ45_IO_P<0>
IO_L0N_33	AE12	QUAD_RJ45_IO_N<0>
IO_L1P_33	AJ11	QUAD_RJ45_IO_P<1>
IO_L1N_33	AK11	QUAD_RJ45_IO_N<1>
IO_L2P_33	AD14	QUAD_RJ45_IO_P<2>
IO_L2N_33	AC14	QUAD_RJ45_IO_N<2>
IO_L3P_33	AK12	QUAD_RJ45_IO_P<3>
IO_L3N_33	AJ12	QUAD_RJ45_IO_N<3>
IO_L4P_33	AF11	QUAD_RJ45_IO_P<4>
IO_L4N_VREF_33	AE11	QUAD_RJ45_IO_N<4>
IO_L5P_33	AM10	QUAD_RJ45_IO_P<5>
IO_L5N_33	AL10	QUAD_RJ45_IO_N<5>
IO_L6P_33	AG11	QUAD_RJ45_IO_P<6>
IO_L6N_33	AG10	QUAD_RJ45_IO_N<6>
IO_L7P_33	AL11	QUAD_RJ45_IO_P<7>
IO_L7N_33	AM11	QUAD_RJ45_IO_N<7>
IO_L8P_SRCC_33	AJ10	QUAD_RJ45_IO_P<8>
IO_L8N_SRCC_33	AH10	QUAD_RJ45_IO_N<8>
IO_L9P_MRCC_33	AC13	QUAD_RJ45_IO_P<9>
IO_L9N_MRCC_33	AC12	QUAD_RJ45_IO_N<9>
IO_L10P_MRCC_33	AD12	QUAD_RJ45_IO_P<10>
IO_L10N_MRCC_33	AD11	QUAD_RJ45_IO_N<10>
IO_L11P_SRCC_33	AP11	QUAD_RJ45_IO_P<11>
IO_L11N_SRCC_33	AP12	QUAD_RJ45_IO_N<11>
IO_L12P_VRN_33	AF13	QUAD_RJ45_IO_P<12>
IO_L12N_VRP_33	AG13	QUAD_RJ45_IO_N<12>
IO_L13P_33	AM12	QUAD_RJ45_IO_P<13>
IO_L13N_33	AN12	QUAD_RJ45_IO_N<13>
IO_L14P_33	AE14	QUAD_RJ45_IO_P<14>
IO_L14N_VREF_33	AF14	QUAD_RJ45_IO_N<14>
IO_L15P_33	AN13	QUAD_RJ45_IO_P<15>
IO_L15N_33	AM13	QUAD_RJ45_IO_N<15>
IO_L16P_33	AG12	QUAD_RJ45_IO_P<16>
IO_L16N_33	AH12	QUAD_RJ45_IO_N<16>
IO_L17P_33	AK13	QUAD_RJ45_IO_P<17>
IO_L17N_33	AL13	QUAD_RJ45_IO_N<17>
IO_L18P_33	AH13	QUAD_RJ45_IO_P<18>
IO_L18N_33	AH14	QUAD_RJ45_IO_N<18>
IO_L19P_33	AP14	QUAD_RJ45_IO_P<19>
IO_L19N_33	AN14	QUAD_RJ45_IO_N<19>

IC11
XC6VLX240T-1FFG1156CES

BANK 22

IO_L0P_22	AE21	QUAD_RJ45_IO_P<40>
IO_L0N_22	AD21	QUAD_RJ45_IO_N<40>
IO_L1P_22	AM18	QUAD_RJ45_IO_P<41>
IO_L1N_22	AL18	QUAD_RJ45_IO_N<41>
IO_L2P_22	AG22	QUAD_RJ45_IO_P<42>
IO_L2N_22	AH22	QUAD_RJ45_IO_N<42>
IO_L3P_22	AP19	QUAD_RJ45_IO_P<43>
IO_L3N_22	AN18	QUAD_RJ45_IO_N<43>
IO_L4P_22	AK22	QUAD_RJ45_IO_P<44>
IO_L4N_VREF_22	AJ22	QUAD_RJ45_IO_N<44>
IO_L5P_22	AN19	QUAD_RJ45_IO_P<45>
IO_L5N_22	AN20	QUAD_RJ45_IO_N<45>
IO_L6P_22	AC20	QUAD_RJ45_IO_P<46>
IO_L6N_22	AD20	QUAD_RJ45_IO_N<46>
IO_L7P_22	AM20	QUAD_RJ45_IO_P<47>
IO_L7N_22	AL20	QUAD_RJ45_IO_N<47>
IO_L8P_SRCC_22	AF19	QUAD_RJ45_IO_P<48>
IO_L8N_SRCC_22	AE19	QUAD_RJ45_IO_N<48>
IO_L9P_MRCC_22	AP20	QUAD_RJ45_IO_P<49>
IO_L9N_MRCC_22	AP21	QUAD_RJ45_IO_N<49>
IO_L10P_MRCC_22	AK19	QUAD_RJ45_IO_P<50>
IO_L10N_MRCC_22	AL19	QUAD_RJ45_IO_N<50>
IO_L11P_SRCC_22	AF20	QUAD_RJ45_IO_P<51>
IO_L11N_SRCC_22	AF21	QUAD_RJ45_IO_N<51>
IO_L12P_VRN_22	AJ20	QUAD_RJ45_IO_P<52>
IO_L12N_VRP_22	AH20	QUAD_RJ45_IO_N<52>
IO_L13P_22	AM21	QUAD_RJ45_IO_P<53>
IO_L13N_22	AL21	QUAD_RJ45_IO_N<53>
IO_L14P_22	AC19	QUAD_RJ45_IO_P<54>
IO_L14N_VREF_22	AD19	QUAD_RJ45_IO_N<54>
IO_L15P_22	AM23	QUAD_RJ45_IO_P<55>
IO_L15N_22	AL23	QUAD_RJ45_IO_N<55>
IO_L16P_22	AK21	QUAD_RJ45_IO_P<56>
IO_L16N_22	AJ21	QUAD_RJ45_IO_N<56>
IO_L17P_22	AM22	QUAD_RJ45_IO_P<57>
IO_L17N_22	AN22	QUAD_RJ45_IO_N<57>
IO_L18P_22	AG20	QUAD_RJ45_IO_P<58>
IO_L18N_22	AG21	QUAD_RJ45_IO_N<58>
IO_L19P_22	AP22	QUAD_RJ45_IO_P<59>
IO_L19N_22	AN23	QUAD_RJ45_IO_N<59>

BANK 33,32,22,23

IO QUAD_RJ45_IO_P<0..79>

IO QUAD_RJ45_IO_N<0..79>

NOTE:

QUAD_RJ45_IO PINS ARE SWAPPED IN THE PCB.

IC11
XC6VLX240T-1FFG1156CES

BANK 32

IO_L0P_32	AG15	QUAD_RJ45_IO_P<20>
IO_L0N_32	AF15	QUAD_RJ45_IO_N<20>
IO_L1P_32	AK14	QUAD_RJ45_IO_P<21>
IO_L1N_32	AJ14	QUAD_RJ45_IO_N<21>
IO_L2P_32	AJ15	QUAD_RJ45_IO_P<22>
IO_L2N_32	AH15	QUAD_RJ45_IO_N<22>
IO_L3P_32	AL15	QUAD_RJ45_IO_P<23>
IO_L3N_32	AL14	QUAD_RJ45_IO_N<23>
IO_L4P_32	AG16	QUAD_RJ45_IO_P<24>
IO_L4N_VREF_32	AF16	QUAD_RJ45_IO_N<24>
IO_L5P_32	AN15	QUAD_RJ45_IO_P<25>
IO_L5N_32	AM15	QUAD_RJ45_IO_N<25>
IO_L6P_32	AJ17	QUAD_RJ45_IO_P<26>
IO_L6N_32	AJ16	QUAD_RJ45_IO_N<26>
IO_L7P_32	AP16	QUAD_RJ45_IO_P<27>
IO_L7N_32	AP15	QUAD_RJ45_IO_N<27>
IO_L8P_SRCC_32	AH17	QUAD_RJ45_IO_P<28>
IO_L8N_SRCC_32	AG17	QUAD_RJ45_IO_N<28>
IO_L9P_MRCC_32	AC15	QUAD_RJ45_IO_P<29>
IO_L9N_MRCC_32	AD15	QUAD_RJ45_IO_N<29>
IO_L10P_MRCC_32	AE16	QUAD_RJ45_IO_P<30>
IO_L10N_MRCC_32	AD16	QUAD_RJ45_IO_N<30>
IO_L11P_SRCC_32	AC18	QUAD_RJ45_IO_P<31>
IO_L11N_SRCC_32	AC17	QUAD_RJ45_IO_N<31>
IO_L12P_VRN_32	AH18	QUAD_RJ45_IO_P<32>
IO_L12N_VRP_32	AG18	QUAD_RJ45_IO_N<32>
IO_L13P_32	AN17	QUAD_RJ45_IO_P<33>
IO_L13N_32	AP17	QUAD_RJ45_IO_N<33>
IO_L14P_32	AJ19	QUAD_RJ45_IO_P<34>
IO_L14N_VREF_32	AH19	QUAD_RJ45_IO_N<34>
IO_L15P_32	AM17	QUAD_RJ45_IO_P<35>
IO_L15N_32	AM16	QUAD_RJ45_IO_N<35>
IO_L16P_32	AD17	QUAD_RJ45_IO_P<36>
IO_L16N_32	AE17	QUAD_RJ45_IO_N<36>
IO_L17P_32	AK18	QUAD_RJ45_IO_P<37>
IO_L17N_32	AK17	QUAD_RJ45_IO_N<37>
IO_L18P_32	AE18	QUAD_RJ45_IO_P<38>
IO_L18N_32	AF18	QUAD_RJ45_IO_N<38>
IO_L19P_32	AL16	QUAD_RJ45_IO_P<39>
IO_L19N_32	AK16	QUAD_RJ45_IO_N<39>

IC11
XC6VLX240T-1FFG1156CES

BANK 23

IO_L0P_23	AH27	QUAD_RJ45_IO_P<60>
IO_L0N_23	AH28	QUAD_RJ45_IO_N<60>
IO_L1P_23	AN30	QUAD_RJ45_IO_P<61>
IO_L1N_23	AM30	QUAD_RJ45_IO_N<61>
IO_L2P_23	AG25	QUAD_RJ45_IO_P<62>
IO_L2N_23	AG26	QUAD_RJ45_IO_N<62>
IO_L3P_23	AP30	QUAD_RJ45_IO_P<63>
IO_L3N_23	AP31	QUAD_RJ45_IO_N<63>
IO_L4P_23	AL29	QUAD_RJ45_IO_P<64>
IO_L4N_VREF_23	AK29	QUAD_RJ45_IO_N<64>
IO_L5P_23	AN29	QUAD_RJ45_IO_P<65>
IO_L5N_23	AP29	QUAD_RJ45_IO_N<65>
IO_L6P_23	AL28	QUAD_RJ45_IO_P<66>
IO_L6N_23	AK28	QUAD_RJ45_IO_N<66>
IO_L7P_23	AN28	QUAD_RJ45_IO_P<67>
IO_L7N_23	AM28	QUAD_RJ45_IO_N<67>
IO_L8P_SRCC_23	AH25	QUAD_RJ45_IO_P<68>
IO_L8N_SRCC_23	AJ25	QUAD_RJ45_IO_N<68>
IO_L9P_MRCC_23	AN27	QUAD_RJ45_IO_P<69>
IO_L9N_MRCC_23	AM27	QUAD_RJ45_IO_N<69>
IO_L10P_MRCC_23	AK27	QUAD_RJ45_IO_P<70>
IO_L10N_MRCC_23	AJ27	QUAD_RJ45_IO_N<70>
IO_L11P_SRCC_23	AH23	QUAD_RJ45_IO_P<71>
IO_L11N_SRCC_23	AH24	QUAD_RJ45_IO_N<71>
IO_L12P_VRN_23	AK26	QUAD_RJ45_IO_P<72>
IO_L12N_VRP_23	AJ26	QUAD_RJ45_IO_N<72>
IO_L13P_23	AL26	QUAD_RJ45_IO_P<73>
IO_L13N_23	AM26	QUAD_RJ45_IO_N<73>
IO_L14P_23	AJ24	QUAD_RJ45_IO_P<74>
IO_L14N_VREF_23	AK24	QUAD_RJ45_IO_N<74>
IO_L15P_23	AP27	QUAD_RJ45_IO_P<75>
IO_L15N_23	AP26	QUAD_RJ45_IO_N<75>
IO_L16P_23	AM25	QUAD_RJ45_IO_P<76>
IO_L16N_23	AL25	QUAD_RJ45_IO_N<76>
IO_L17P_23	AN25	QUAD_RJ45_IO_P<77>
IO_L17N_23	AN24	QUAD_RJ45_IO_N<77>
IO_L18P_23	AK23	QUAD_RJ45_IO_P<78>
IO_L18N_23	AL24	QUAD_RJ45_IO_N<78>
IO_L19P_23	AP25	QUAD_RJ45_IO_P<79>
IO_L19N_23	AP24	QUAD_RJ45_IO_N<79>

Project file:sru_rev2.cpm SYSTEM:

CERN TE/MPE
European Organization
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1211 GENEVA 23
SWITZERLAND

PROJECT:SRU v2.0

MODULE:fpga Sheet: 2/7 Module: 2/7 Project: 5/81

LAST_MODIFIED=Fri Dec 09 11:01:36 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

IC11
XC6VLX240T-1FFG1156CES

BANK 12

IO_L0P_12	AD25	QUAD_RJ45_IO_P<80>
IO_L0N_12	AD26	QUAD_RJ45_IO_N<80>
IO_L1P_12	AE27	QUAD_RJ45_IO_P<81>
IO_L1N_12	AD27	QUAD_RJ45_IO_N<81>
IO_L2P_12	AH33	QUAD_RJ45_IO_P<82>
IO_L2N_12	AH32	QUAD_RJ45_IO_N<82>
IO_L3P_12	AE28	QUAD_RJ45_IO_P<83>
IO_L3N_12	AE29	QUAD_RJ45_IO_N<83>
IO_L4P_12	AJ34	QUAD_RJ45_IO_P<84>
IO_L4N_VREF_12	AH34	QUAD_RJ45_IO_N<84>
IO_L5P_12	AF28	QUAD_RJ45_IO_P<85>
IO_L5N_12	AF29	QUAD_RJ45_IO_N<85>
IO_L6P_12	AL34	QUAD_RJ45_IO_P<86>
IO_L6N_12	AK34	QUAD_RJ45_IO_N<86>
IO_L7P_12	AH29	QUAD_RJ45_IO_P<87>
IO_L7N_12	AH30	QUAD_RJ45_IO_N<87>
IO_L8P_SRCC_12	AN33	QUAD_RJ45_IO_P<88>
IO_L8N_SRCC_12	AN34	QUAD_RJ45_IO_N<88>
IO_L9P_MRCC_12	AG27	QUAD_RJ45_IO_P<89>
IO_L9N_MRCC_12	AG28	QUAD_RJ45_IO_N<89>
IO_L10P_MRCC_12	AF30	QUAD_RJ45_IO_P<90>
IO_L10N_MRCC_12	AG30	QUAD_RJ45_IO_N<90>
IO_L11P_SRCC_12	AF26	QUAD_RJ45_IO_P<91>
IO_L11N_SRCC_12	AE26	QUAD_RJ45_IO_N<91>
IO_L12P_VRN_12	AJ31	QUAD_RJ45_IO_P<92>
IO_L12N_VRP_12	AJ32	QUAD_RJ45_IO_N<92>
IO_L13P_12	AJ29	QUAD_RJ45_IO_P<93>
IO_L13N_12	AJ30	QUAD_RJ45_IO_N<93>
IO_L14P_12	AK33	QUAD_RJ45_IO_P<94>
IO_L14N_VREF_12	AK32	QUAD_RJ45_IO_N<94>
IO_L15P_12	AL31	QUAD_RJ45_IO_P<95>
IO_L15N_12	AK31	QUAD_RJ45_IO_N<95>
IO_L16P_12	AM33	QUAD_RJ45_IO_P<96>
IO_L16N_12	AL33	QUAD_RJ45_IO_N<96>
IO_L17P_12	AN32	QUAD_RJ45_IO_P<97>
IO_L17N_12	AM32	QUAD_RJ45_IO_N<97>
IO_L18P_12	AP32	QUAD_RJ45_IO_P<98>
IO_L18N_12	AP33	QUAD_RJ45_IO_N<98>
IO_L19P_12	AL30	QUAD_RJ45_IO_P<99>
IO_L19N_12	AM31	QUAD_RJ45_IO_N<99>

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BANK 14

IO_L0P_14	U25	QUAD_RJ45_IO_P<120>
IO_L0N_14	T25	QUAD_RJ45_IO_N<120>
IO_L1P_14	T28	QUAD_RJ45_IO_P<121>
IO_L1N_14	T29	QUAD_RJ45_IO_N<121>
IO_L2P_14	R33	QUAD_RJ45_IO_P<122>
IO_L2N_14	R34	QUAD_RJ45_IO_N<122>
IO_L3P_14	T30	QUAD_RJ45_IO_P<123>
IO_L3N_14	T31	QUAD_RJ45_IO_N<123>
IO_L4P_14	T33	QUAD_RJ45_IO_P<124>
IO_L4N_VREF_14	T34	QUAD_RJ45_IO_N<124>
IO_L5P_14	U26	QUAD_RJ45_IO_P<125>
IO_L5N_14	U27	QUAD_RJ45_IO_N<125>
IO_L6P_14	U33	QUAD_RJ45_IO_P<126>
IO_L6N_14	U32	QUAD_RJ45_IO_N<126>
IO_L7P_14	U28	QUAD_RJ45_IO_P<127>
IO_L7N_14	V29	QUAD_RJ45_IO_N<127>
IO_L8P_SRCC_14	U31	QUAD_RJ45_IO_P<128>
IO_L8N_SRCC_14	U30	QUAD_RJ45_IO_N<128>
IO_L9P_MRCC_14	V30	QUAD_RJ45_IO_P<129>
IO_L9N_MRCC_14	W30	QUAD_RJ45_IO_N<129>
IO_L10P_MRCC_14	V34	QUAD_RJ45_IO_P<130>
IO_L10N_MRCC_14	W34	QUAD_RJ45_IO_N<130>
IO_L11P_SRCC_14	V28	QUAD_RJ45_IO_P<131>
IO_L11N_SRCC_14	V27	QUAD_RJ45_IO_N<131>
IO_L12P_VRN_14	V32	QUAD_RJ45_IO_P<132>
IO_L12N_VRP_14	V33	QUAD_RJ45_IO_N<132>
IO_L13P_14	Y32	QUAD_RJ45_IO_P<133>
IO_L13N_14	Y31	QUAD_RJ45_IO_N<133>
IO_L14P_14	Y33	QUAD_RJ45_IO_P<134>
IO_L14N_VREF_14	Y34	QUAD_RJ45_IO_N<134>
IO_L15P_14	W29	QUAD_RJ45_IO_P<135>
IO_L15N_14	Y29	QUAD_RJ45_IO_N<135>
IO_L16P_14	W31	QUAD_RJ45_IO_P<136>
IO_L16N_14	W32	QUAD_RJ45_IO_N<136>
IO_L17P_14	Y28	QUAD_RJ45_IO_P<137>
IO_L17N_14	Y27	QUAD_RJ45_IO_N<137>
IO_L18P_14	W25	QUAD_RJ45_IO_P<138>
IO_L18N_14	V25	QUAD_RJ45_IO_N<138>
IO_L19P_14	W27	QUAD_RJ45_IO_P<139>
IO_L19N_14	W26	QUAD_RJ45_IO_N<139>

BANK 12,13,14,15

IO QUAD_RJ45_IO_P<80..159>

IO QUAD_RJ45_IO_N<80..159>

NOTE:

QUAD_RJ45_IO PINS ARE SWAPPED IN THE PCB.

IC11
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BANK 15

IO_L0P_15	M31	QUAD_RJ45_IO_P<140>
IO_L0N_15	L31	QUAD_RJ45_IO_N<140>
IO_L1P_15	N25	QUAD_RJ45_IO_P<141>
IO_L1N_15	M25	QUAD_RJ45_IO_N<141>
IO_L2P_SM8P_15	K32	QUAD_RJ45_IO_P<142>
IO_L2N_SM8N_15	K31	QUAD_RJ45_IO_N<142>
IO_L3P_SM9P_15	M26	QUAD_RJ45_IO_P<143>
IO_L3N_SM9N_15	M27	QUAD_RJ45_IO_N<143>
IO_L4P_15	P31	QUAD_RJ45_IO_P<144>
IO_L4N_VREF_15	P30	QUAD_RJ45_IO_N<144>
IO_L5P_SM10P_15	N27	QUAD_RJ45_IO_P<145>
IO_L5N_SM10N_15	P27	QUAD_RJ45_IO_N<145>
IO_L6P_SM11P_15	L33	QUAD_RJ45_IO_P<146>
IO_L6N_SM11N_15	M32	QUAD_RJ45_IO_N<146>
IO_L7P_SM12P_15	L28	QUAD_RJ45_IO_P<147>
IO_L7N_SM12N_15	M28	QUAD_RJ45_IO_N<147>
IO_L8P_SRCC_15	N32	QUAD_RJ45_IO_P<148>
IO_L8N_SRCC_15	P32	QUAD_RJ45_IO_N<148>
IO_L9P_MRCC_15	N28	QUAD_RJ45_IO_P<149>
IO_L9N_MRCC_15	N29	QUAD_RJ45_IO_N<149>
IO_L10P_MRCC_15	N33	QUAD_RJ45_IO_P<150>
IO_L10N_MRCC_15	M33	QUAD_RJ45_IO_N<150>
IO_L11P_SRCC_15	L29	QUAD_RJ45_IO_P<151>
IO_L11N_SRCC_15	L30	QUAD_RJ45_IO_N<151>
IO_L12P_SM13P_15	P25	QUAD_RJ45_IO_P<152>
IO_L12N_SM13N_15	P26	QUAD_RJ45_IO_N<152>
IO_L13P_SM14P_15	R28	QUAD_RJ45_IO_P<153>
IO_L13N_SM14N_15	R27	QUAD_RJ45_IO_N<153>
IO_L14P_15	R31	QUAD_RJ45_IO_P<154>
IO_L14N_VREF_15	R32	QUAD_RJ45_IO_N<154>
IO_L15P_SM15P_15	R26	QUAD_RJ45_IO_P<155>
IO_L15N_SM15N_15	T26	QUAD_RJ45_IO_N<155>
IO_L16P_VRN_15	K34	QUAD_RJ45_IO_P<156>
IO_L16N_VRP_15	L34	QUAD_RJ45_IO_N<156>
IO_L17P_15	M30	QUAD_RJ45_IO_P<157>
IO_L17N_15	N30	QUAD_RJ45_IO_N<157>
IO_L18P_15	N34	QUAD_RJ45_IO_P<158>
IO_L18N_15	P34	QUAD_RJ45_IO_N<158>
IO_L19P_15	P29	QUAD_RJ45_IO_P<159>
IO_L19N_15	R29	QUAD_RJ45_IO_N<159>

IC11
XC6VLX240T-1FFG1156CES

BANK 13

IO_L0P_13	AA34	QUAD_RJ45_IO_P<100>
IO_L0N_13	AA33	QUAD_RJ45_IO_N<100>
IO_L1P_13	AA30	QUAD_RJ45_IO_P<101>
IO_L1N_13	AA31	QUAD_RJ45_IO_N<101>
IO_L2P_13	AD34	QUAD_RJ45_IO_P<102>
IO_L2N_13	AC34	QUAD_RJ45_IO_N<102>
IO_L3P_13	AB30	QUAD_RJ45_IO_P<103>
IO_L3N_13	AB31	QUAD_RJ45_IO_N<103>
IO_L4P_13	AC33	QUAD_RJ45_IO_P<104>
IO_L4N_VREF_13	AB33	QUAD_RJ45_IO_N<104>
IO_L5P_13	AE31	QUAD_RJ45_IO_P<105>
IO_L5N_13	AD31	QUAD_RJ45_IO_N<105>
IO_L6P_13	AA25	QUAD_RJ45_IO_P<106>
IO_L6N_13	Y26	QUAD_RJ45_IO_N<106>
IO_L7P_13	AA28	QUAD_RJ45_IO_P<107>
IO_L7N_13	AA29	QUAD_RJ45_IO_N<107>
IO_L8P_SRCC_13	AE34	QUAD_RJ45_IO_P<108>
IO_L8N_SRCC_13	AF34	QUAD_RJ45_IO_N<108>
IO_L9P_MRCC_13	AD30	QUAD_RJ45_IO_P<109>
IO_L9N_MRCC_13	AC30	QUAD_RJ45_IO_N<109>
IO_L10P_MRCC_13	AE33	QUAD_RJ45_IO_P<110>
IO_L10N_MRCC_13	AF33	QUAD_RJ45_IO_N<110>
IO_L11P_SRCC_13	AD29	QUAD_RJ45_IO_P<111>
IO_L11N_SRCC_13	AC29	QUAD_RJ45_IO_N<111>
IO_L12P_VRN_13	AB32	QUAD_RJ45_IO_P<112>
IO_L12N_VRP_13	AC32	QUAD_RJ45_IO_N<112>
IO_L13P_13	AB28	QUAD_RJ45_IO_P<113>
IO_L13N_13	AC28	QUAD_RJ45_IO_N<113>
IO_L14P_13	AD32	QUAD_RJ45_IO_P<114>
IO_L14N_VREF_13	AE32	QUAD_RJ45_IO_N<114>
IO_L15P_13	AB27	QUAD_RJ45_IO_P<115>
IO_L15N_13	AC27	QUAD_RJ45_IO_N<115>
IO_L16P_13	AG33	QUAD_RJ45_IO_P<116>
IO_L16N_13	AG32	QUAD_RJ45_IO_N<116>
IO_L17P_13	AA26	QUAD_RJ45_IO_P<117>
IO_L17N_13	AB26	QUAD_RJ45_IO_N<117>
IO_L18P_13	AG31	QUAD_RJ45_IO_P<118>
IO_L18N_13	AF31	QUAD_RJ45_IO_N<118>
IO_L19P_13	AB25	QUAD_RJ45_IO_P<119>
IO_L19N_13	AC25	QUAD_RJ45_IO_N<119>

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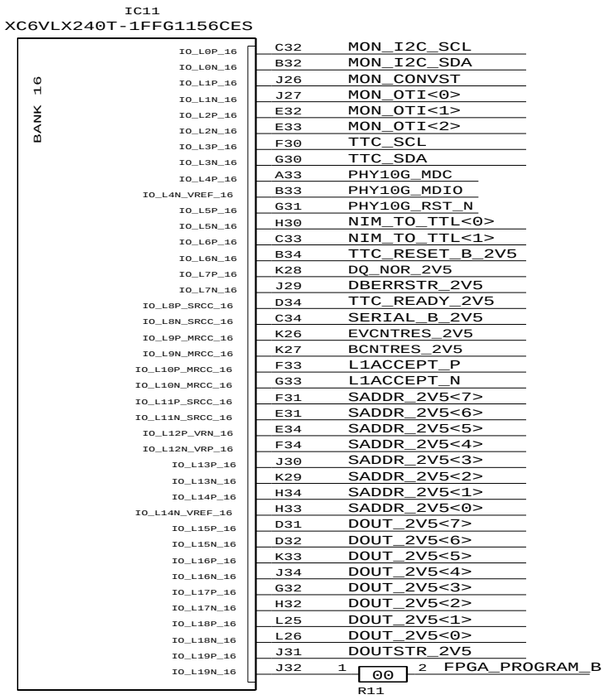
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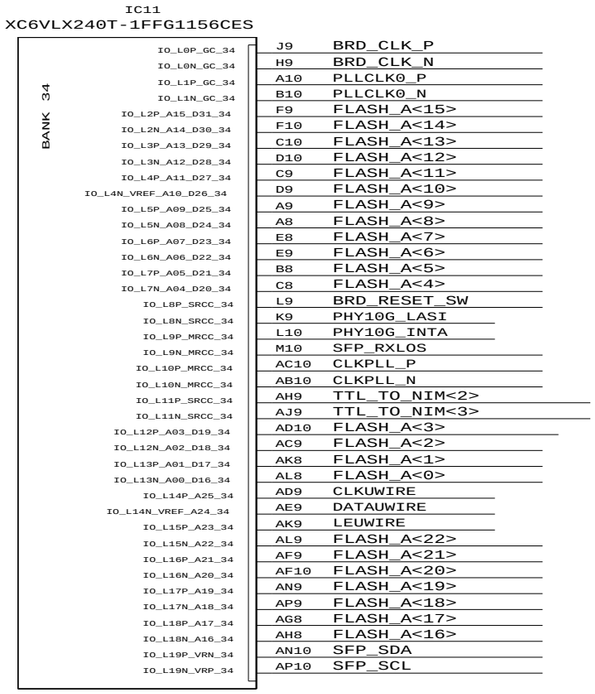
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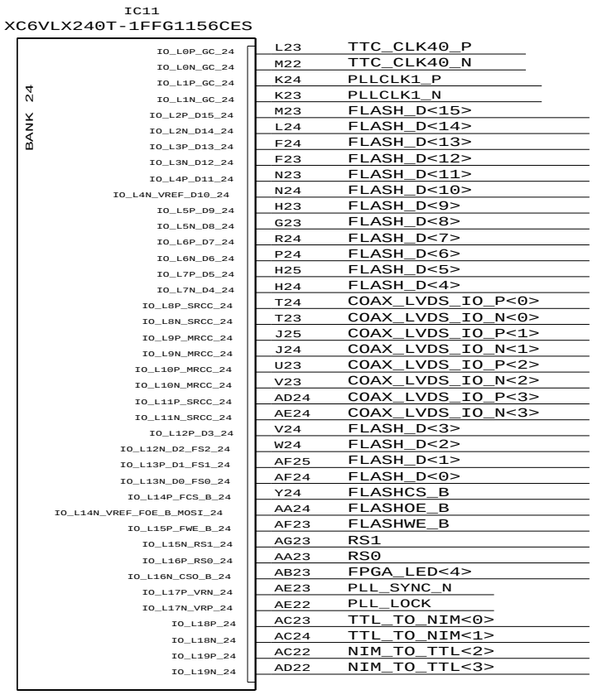
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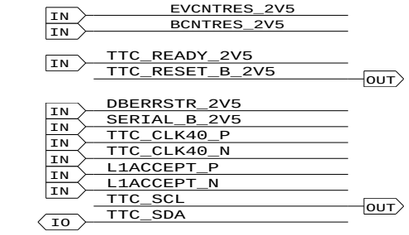
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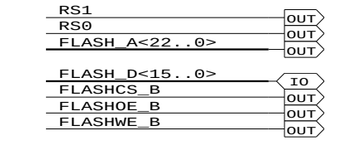
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

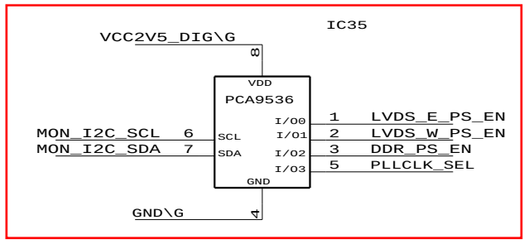


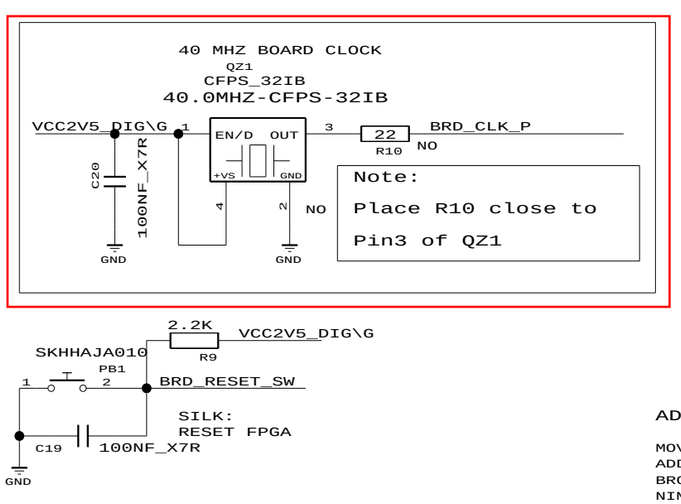


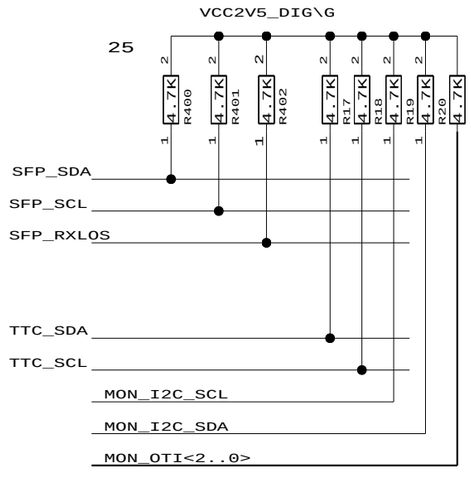


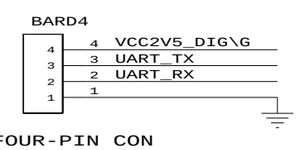


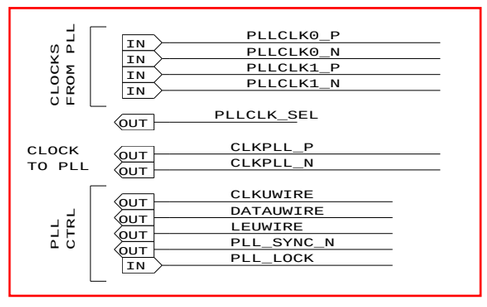












ADDED FRONT-PANNEL DOUBLE LED

MOVED TTC_CLK40M TO BANK 34 (GC)
ADDED EVCNTRES AND BCNTRES
BRCST SIGNALS ELIMINATED
NIM_TO_TTL<0:1> MOVED FROM L23, M22 TO H30, C33

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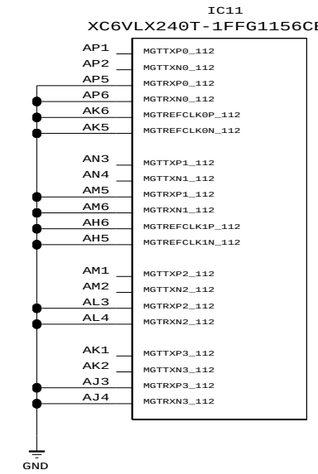
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1211 GENEVA 23
SWITZERLAND
TE/MPE

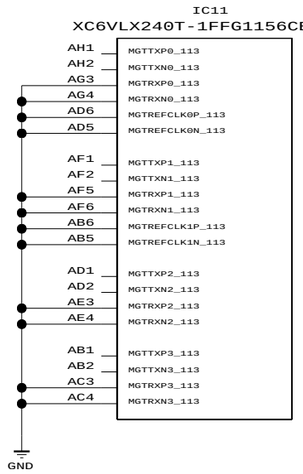
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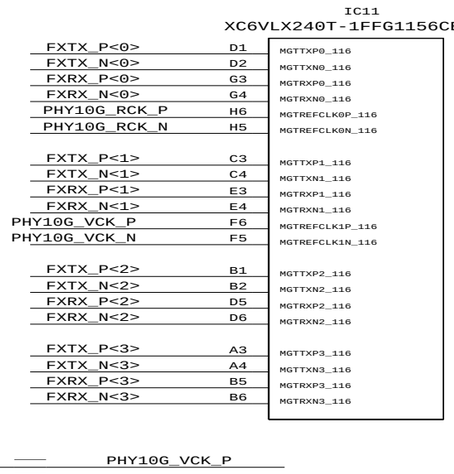
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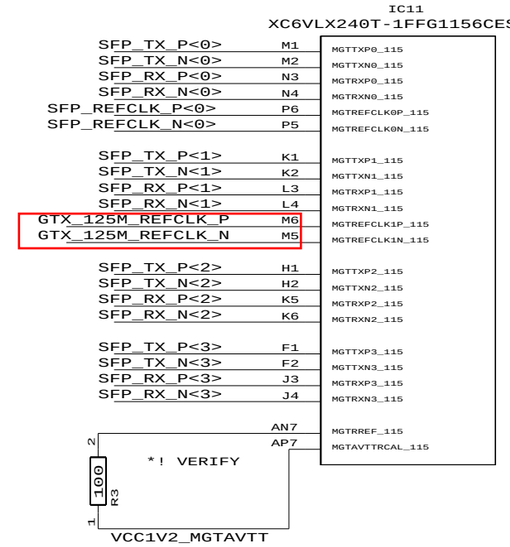
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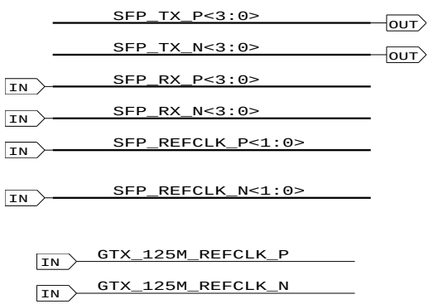
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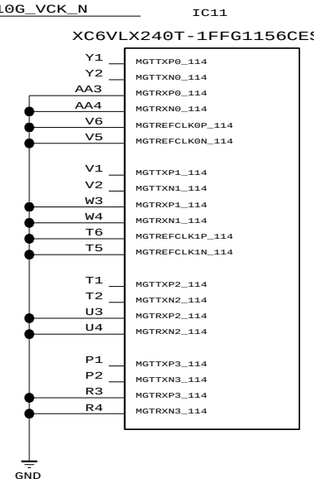


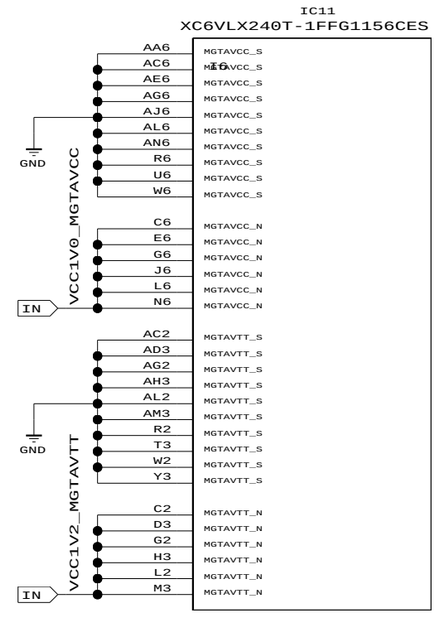
NOTE:

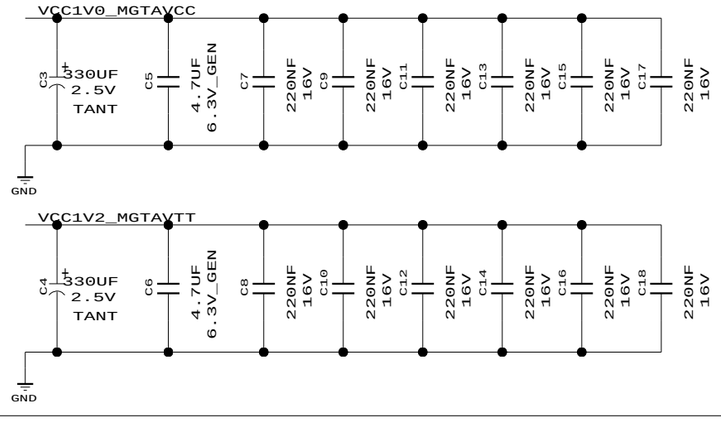
UNUSED QUARD PINS:

INPUT : GND
OUTPUT: FLOAT

SOUTH POWER: GND







NOTE: POWER SUPPLY DECAP FOR GTX

1. ONE 0.22UF, SIZE 0402, CERAMIC CAPACITOR PER POWER SUPPLY PIN
2. ONE 4.7 UF, SIZE 0402, CERAMIC CAPACITOR PER TWO QUADS
3. ONE 330UF BULK CAPACITOR FOR EACH POWER SUPPLY

Project file:sru_rev2.cpm SYSTEM:

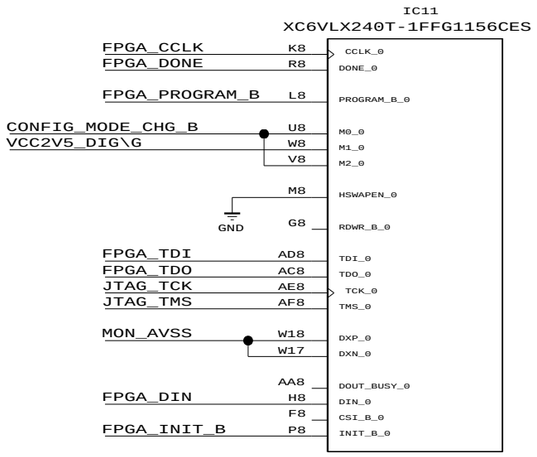
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

PROJECT:SRU v2.0

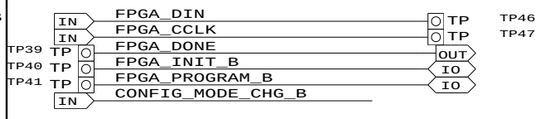
MODULE:fpga Sheet: 5/7 Module: Project: 8/81

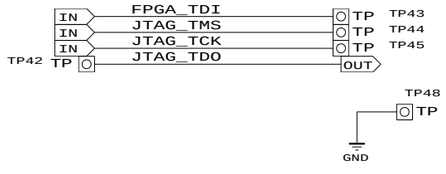
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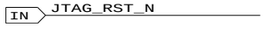
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

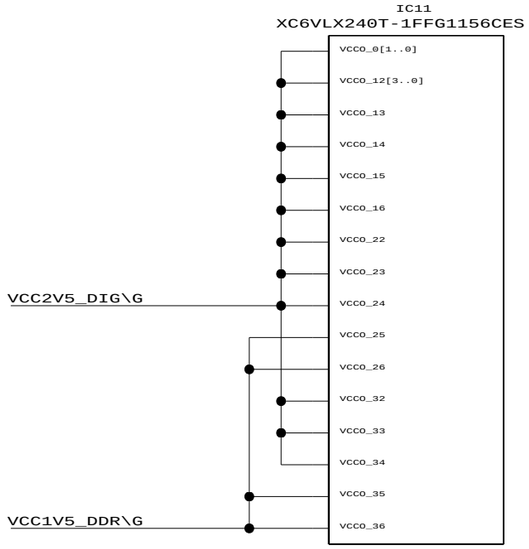


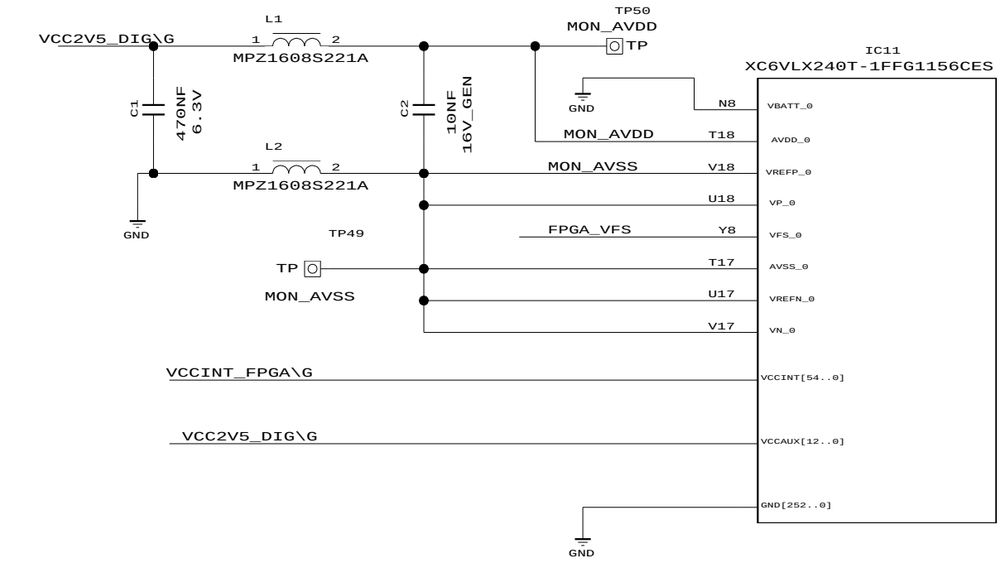
CONFIGURATION MODE	M2	M1	M0
SLAVE SERIAL	1	1	1
MASTER BPI-UP	0	1	0

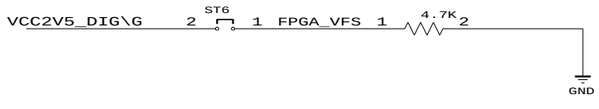












Note:
Put Sig_name close
to all TP points

Project file:sru_rev2.cpm			SYSTEM:
CERN TE/MPE — European Organization for Nuclear Research, 1211 GENEVA 23, SWITZERLAND	PROJECT:SRU v2.0		
	MODULE:fpga	Sheet: Module: 6/7 Project: 9/81	
	LAST_MODIFIED=Fri Dec 09 11:01:35 2011		
	Design by: FZhang/SMartoiu	PCB by: EXT	DATE: 29/07/2010

VCCINT_FPGA\G

C26 330UF 2.5V TANT

C32 330UF 2.5V TANT

GND

C27 2.2UF 10V X7R

C35 2.2UF 10V X7R

C42 2.2UF 10V X7R

C46 2.2UF 10V X7R

GND

C28 220NF 16V X7R

C36 220NF 16V X7R

C43 220NF 16V X7R

C47 220NF 16V X7R

C53 220NF 16V X7R

C59 220NF 16V X7R

C63 220NF 16V X7R

C69 220NF 16V X7R

GND

VCC2V5_DIG\G

C79 33UF 6.3V

C81 2.2UF 10V X7R

C82 220NF 16V X7R

GND

BANK12

VCC2V5_DIG\G

C25 47UF 6.3V

C34 2.2UF 10V X7R

C41 220NF 16V X7R

GND

BANK22

VCC2V5_DIG\G

C50 47UF 6.3V

C56 2.2UF 10V X7R

C62 220NF 16V X7R

GND

BANK32

VCC2V5_DIG\G

C64 47UF 6.3V

C212 2.2UF 10V X7R

C75 220NF 16V X7R

GND

BANK33

VCC2V5_DIG\G

C65 47UF 6.3V

C71 2.2UF 10V X7R

C76 220NF 16V X7R

GND

BANK13

VCC2V5_DIG\G

C24 47UF 6.3V

C33 2.2UF 10V X7R

C40 220NF 16V X7R

GND

BANK23

VCC2V5_DIG\G

C48 47UF 6.3V

C54 2.2UF 10V X7R

C60 220NF 16V X7R

GND

BANK14

VCC2V5_DIG\G

C21 47UF 6.3V

C29 2.2UF 10V X7R

C37 220NF 16V X7R

GND

BANK24

VCC2V5_DIG\G

C49 47UF 6.3V

C55 2.2UF 10V X7R

C61 220NF 16V X7R

GND

BANK34

VCC2V5_DIG\G

C66 47UF 6.3V

C72 2.2UF 10V X7R

C77 220NF 16V X7R

GND

BANK15

VCC2V5_DIG\G

C22 47UF 6.3V

C30 2.2UF 10V X7R

C38 220NF 16V X7R

GND

BANK25

VCC1V5_DDR\G

C45 47UF 6.3V

C52 2.2UF 10V X7R

C58 220NF 16V X7R

GND

BANK35

VCC1V5_DDR\G

C68 47UF 6.3V

C74 2.2UF 10V X7R

C80 220NF 16V X7R

GND

BANK16

VCC2V5_DIG\G

C23 47UF 6.3V

C31 2.2UF 10V X7R

C39 220NF 16V X7R

GND

BANK26

VCC1V5_DDR\G

C44 47UF 6.3V

C51 2.2UF 10V X7R

C57 220NF 16V X7R

GND

BANK36

VCC1V5_DDR\G

C67 47UF 6.3V

C73 2.2UF 10V X7R

C78 220NF 16V X7R

GND

Project file:sru_rev2.cpm

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PROJECT:SRU v2.0

MODULE:fpga

Sheet: 7/7 Module: Project: 10/81

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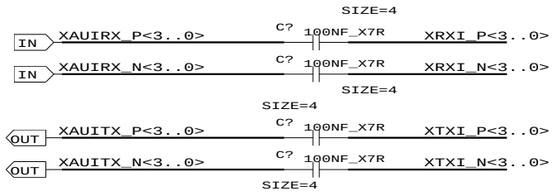
Design by: FZhang/SMartoiu

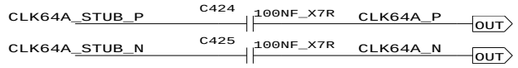
PCB by: EXT

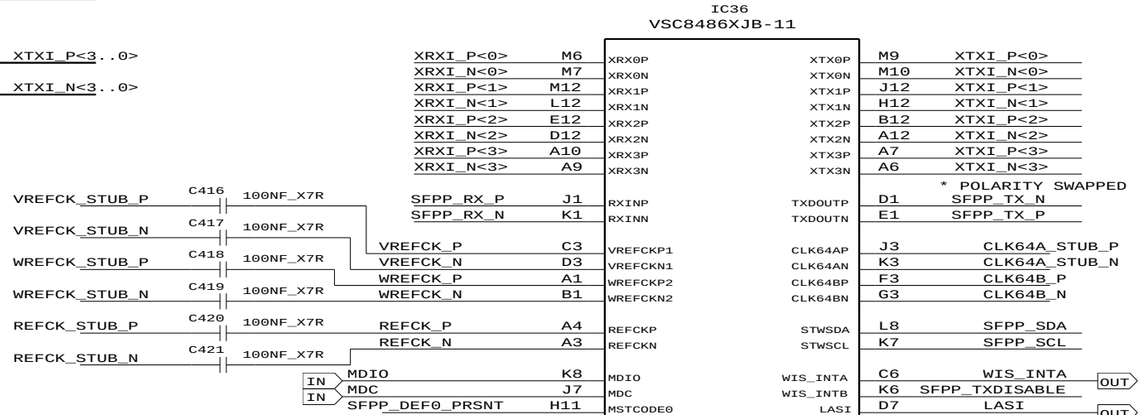
DATE: 29/07/2010

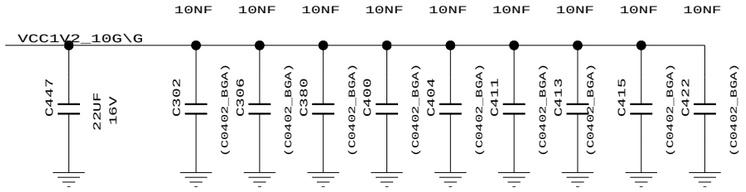
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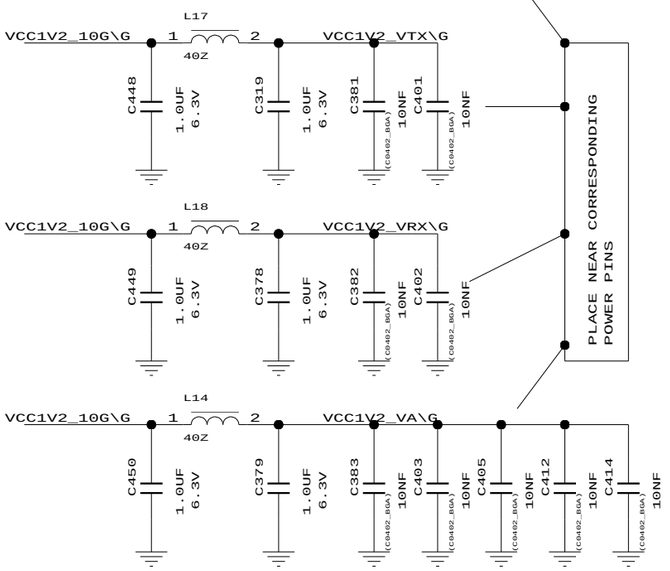
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

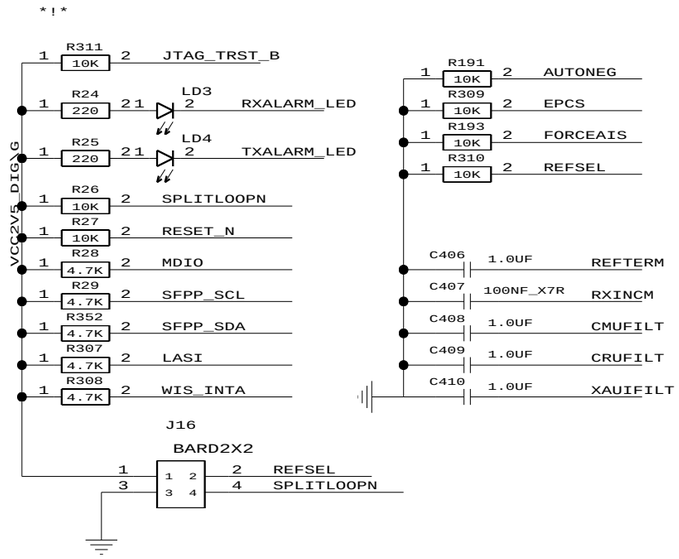


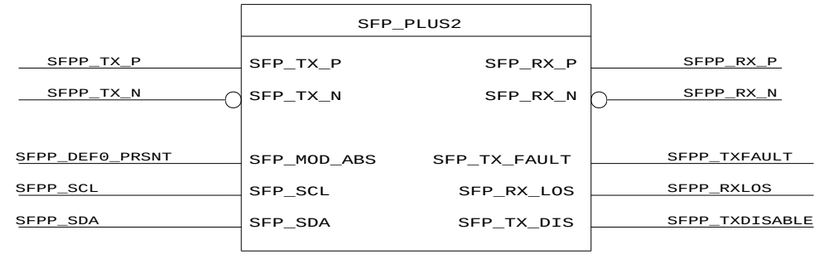




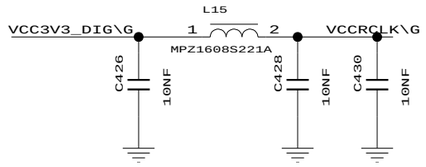


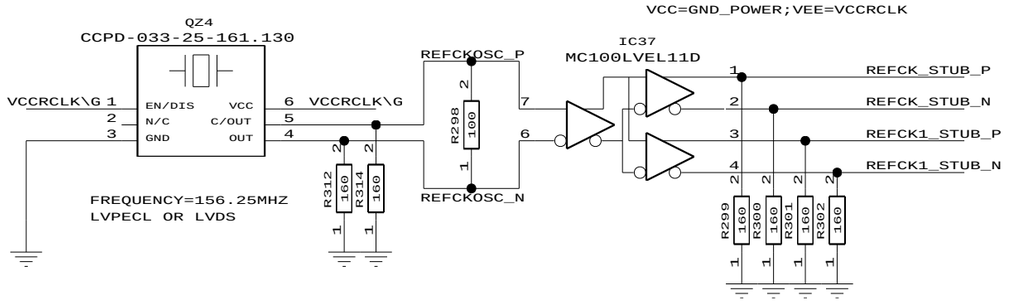






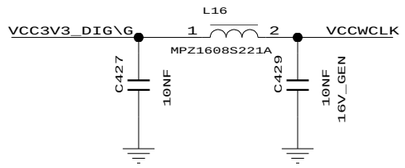
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European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (TE/MPE)	PROJECT:SRU v2.0		
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	LAST_MODIFIED=Fri Dec 09 11:01:42 2011		
	Design by: FZhang/SMartoiu	PCB by: EXT	DATE: 29/07/2010

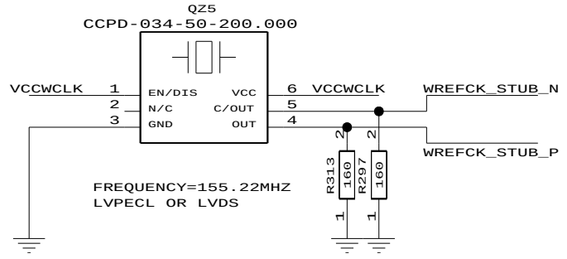


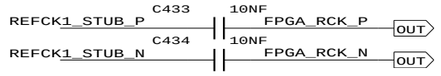


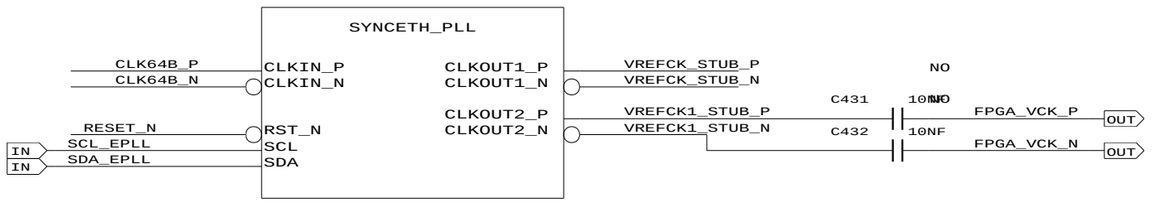
WAN CLOCK GENERATOR

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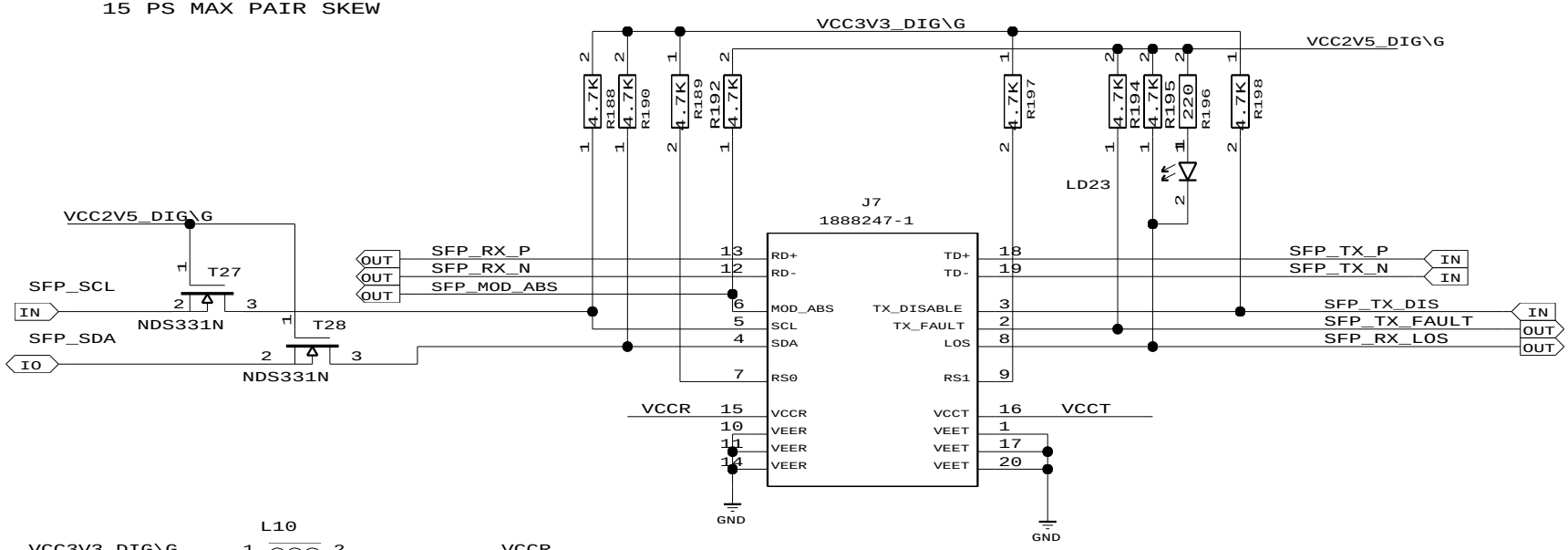


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European Organization for Nuclear Research, 1211 GENEVA 23, SWITZERLAND (TE/MPE)	PROJECT:SRU v2.0	
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	Design by: FZhang/SMartoiu	PCB by: EXT / DATE: 29/07/2010

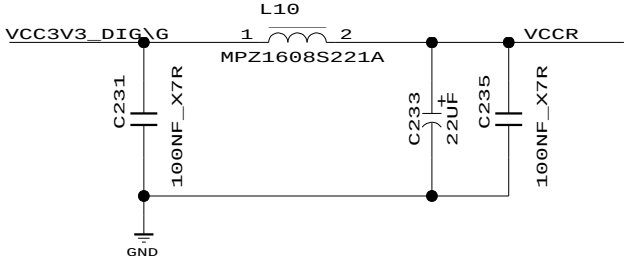
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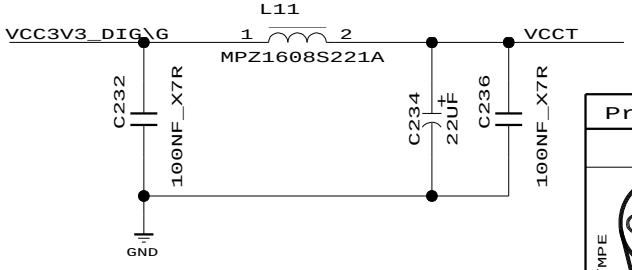
- TX AND RX PAIRS SHOULD BE ROUTED ONLY
  USING ONE ROUTING LAYER, 100 OHM DIFF.
  5 GBPS, 45 BENDS AND NO JOGS,
  15 PS MAX PAIR SKEW

SFP+ 10GB-ETH MODULE



1888247-1





Project file:sru_rev2.cpm

SYSTEM:

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

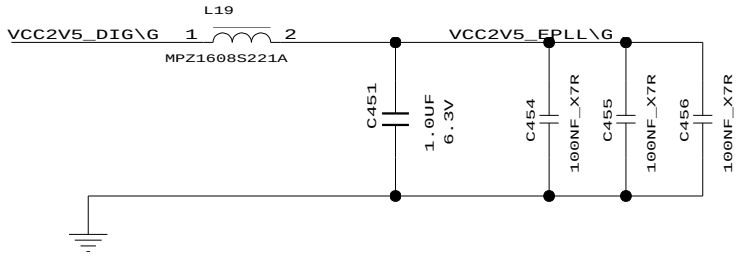
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MODULE:sfp_plus2

Sheet: Module: 1/1 Project: 13/81

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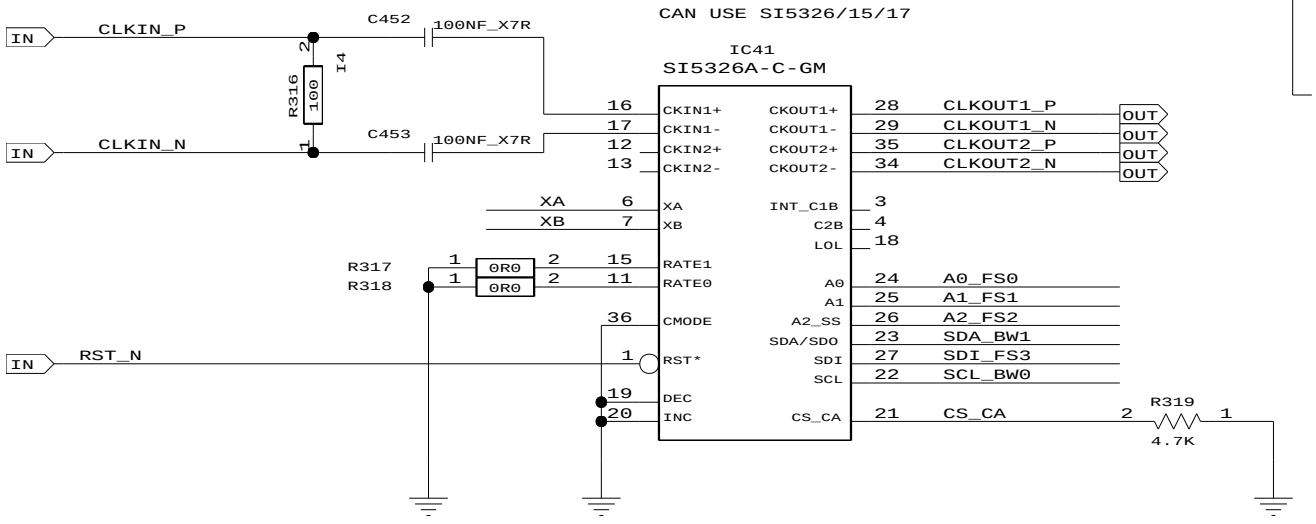
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

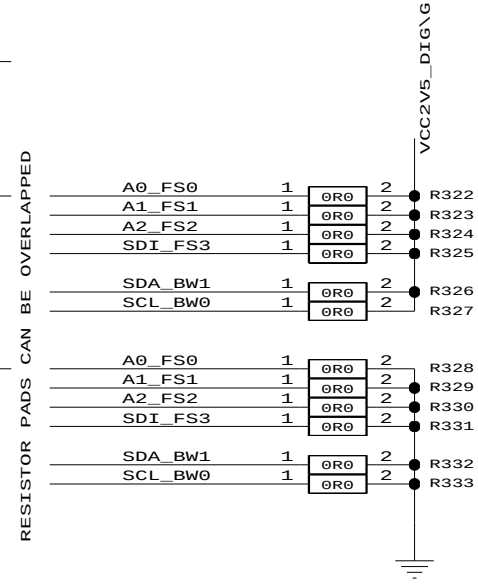


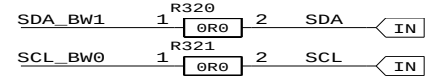
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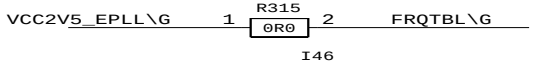






I2C ADDR = 1101HHH

(FRQTBL:2;GND:9,14,8,31,37;VCC2V5_EPLL:33;VDD:5,10,32)
VDD=VCC2V5_EPLL
(30)



Project file:sru_rev2.cpm

SYSTEM:

PROJECT:SRU v2.0

MODULE:synceth_pll

Sheet: Module: 1/1 Project: 14/81

LAST_MODIFIED=Fri Dec 09 11:01:45 2011

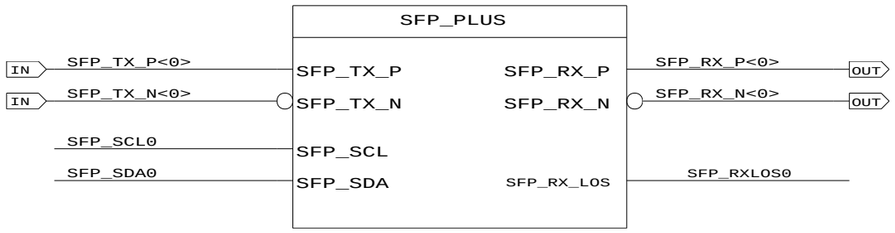
Design by: FZhang/SMartoiu

PCB by: EXT

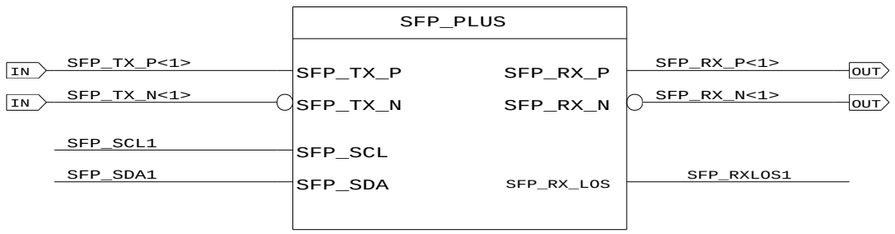
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European Organization
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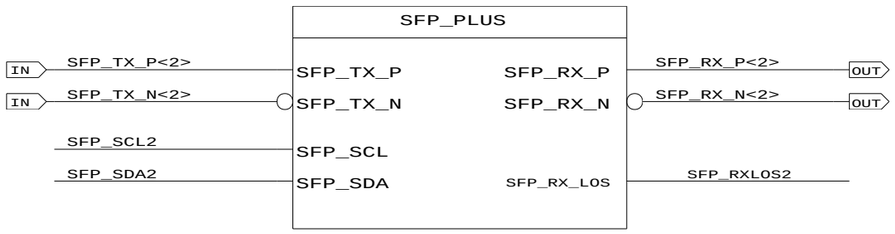
SFP+ A



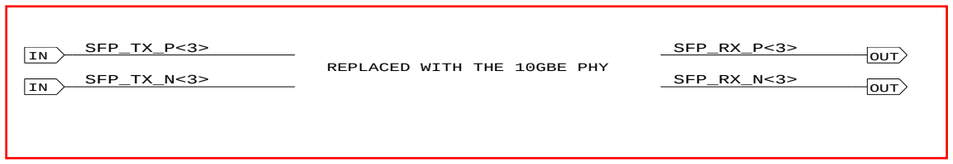
SFP+ B

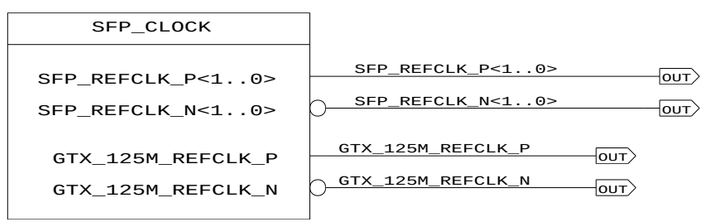


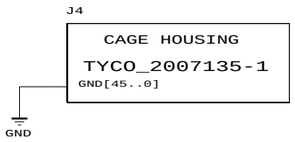
SFP+ C



SFP+ D

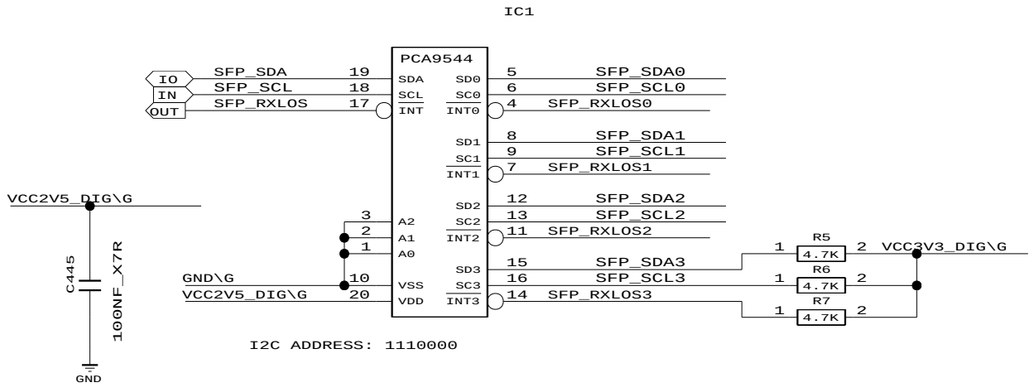






Tyco QUAD SFP+ 2007135-1

IC1



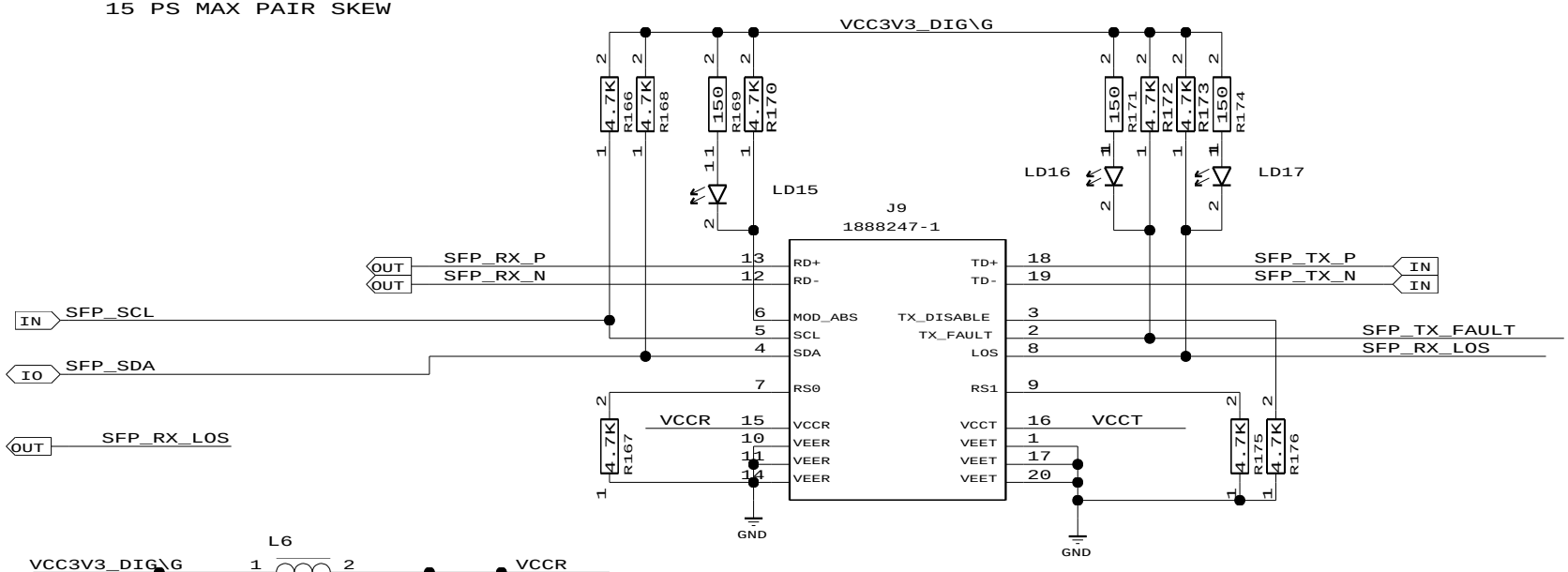
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TE/MPE CERN European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND	PROJECT:SRU v2.0		
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	LAST_MODIFIED=Fri Dec 09 11:01:30 2011		
	Design by: FZhang/SMartoiu	PCB by: EXT	DATE: 29/07/2010

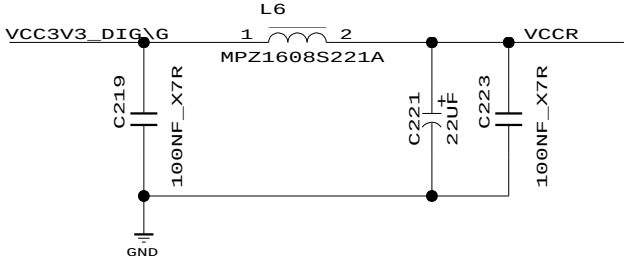
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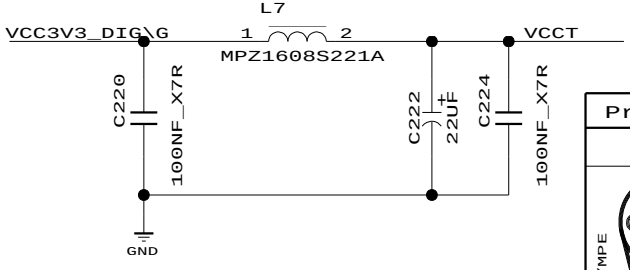
- TX AND RX PAIRS SHOULD BE ROUTED ONLY
  USING ONE ROUTING LAYER, 100 OHM DIFF.
  5 GBPS, 45 BENDS AND NO JOGS,
  15 PS MAX PAIR SKEW

SFP+ MODULE



1888247-1





Project file:sru_rev2.cpm

SYSTEM:

CERN
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

PROJECT:SRU v2.0

MODULE:sfp_plus

Sheet: Module: 1/1 Project: 16/81

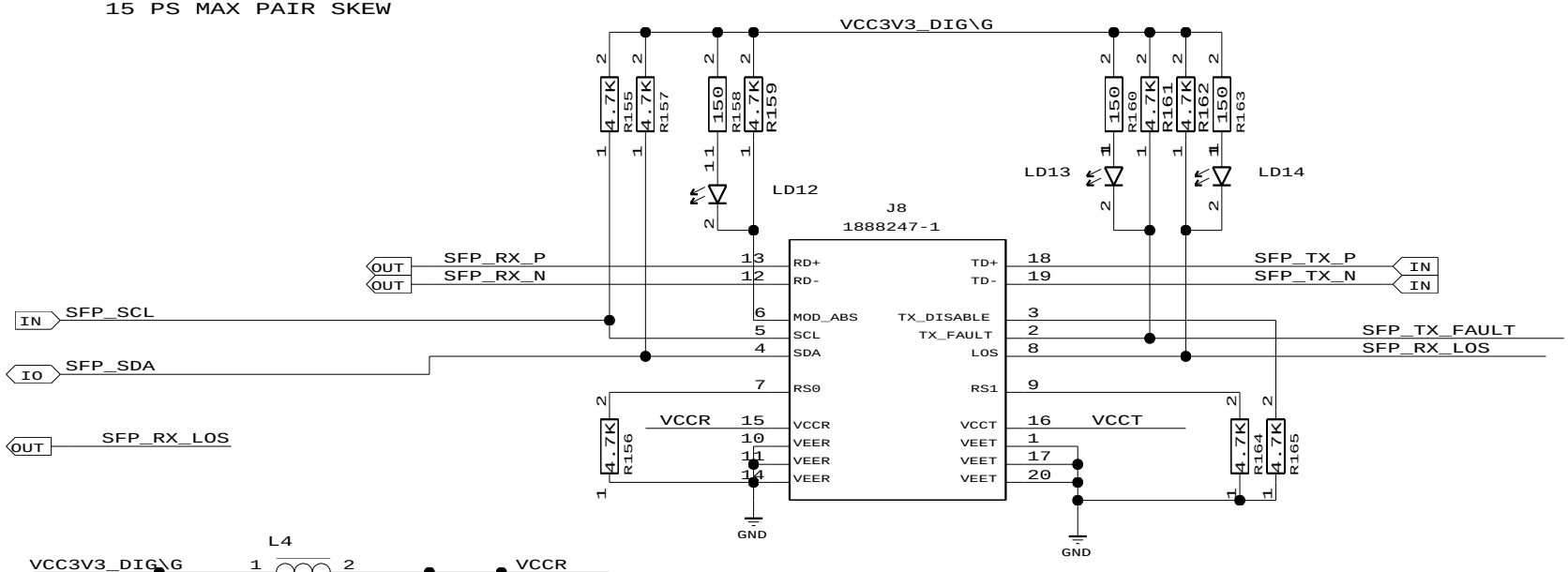
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Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

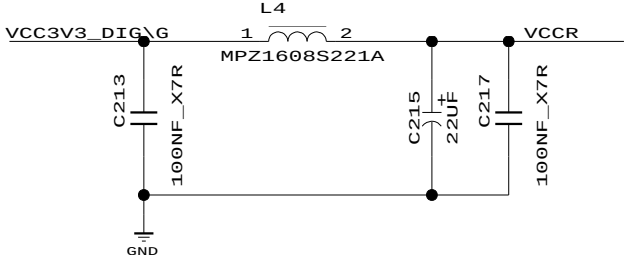
NOTE:

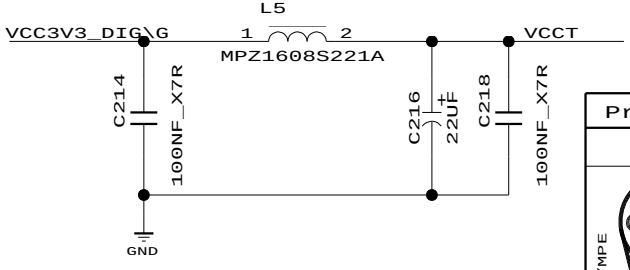
- TX AND RX PAIRS SHOULD BE ROUTED ONLY
  USING ONE ROUTING LAYER, 100 OHM DIFF.
  5 GBPS, 45 BENDS AND NO JOGS,
  15 PS MAX PAIR SKEW

SFP+ MODULE



1888247-1





Project file:sru_rev2.cpm

SYSTEM:

PROJECT:SRU v2.0

MODULE:sfp_plus

Sheet: Module: 1/1 Project: 17/81

LAST_MODIFIED=Mon Dec 12 10:52:10 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

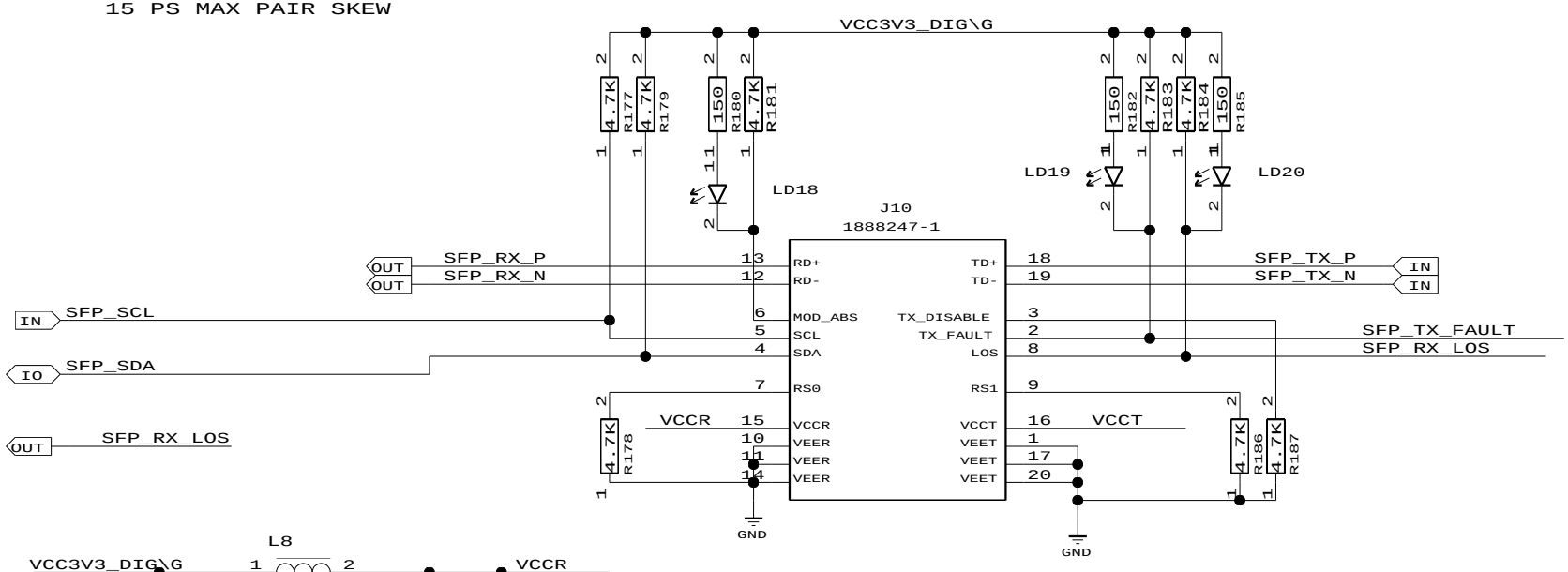
TE/MPE

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

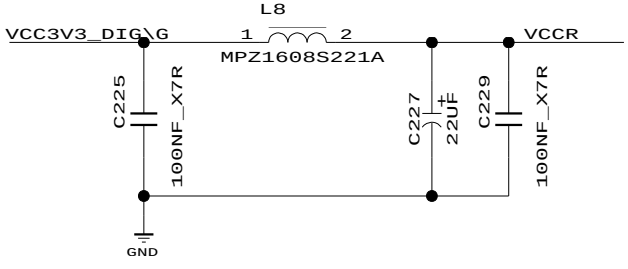
NOTE:

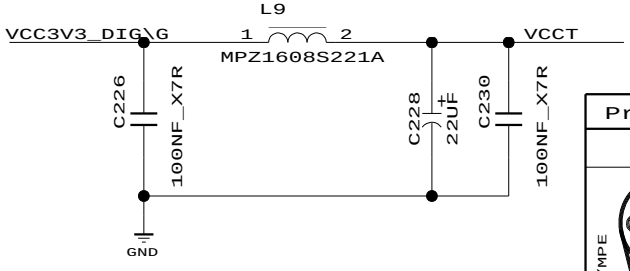
- TX AND RX PAIRS SHOULD BE ROUTED ONLY
  USING ONE ROUTING LAYER, 100 OHM DIFF.
  5 GBPS, 45 BENDS AND NO JOGS,
  15 PS MAX PAIR SKEW

SFP+ MODULE



1888247-1





Project file:sru_rev2.cpm

SYSTEM:

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European Organization
for Nuclear Research
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TE/MPE

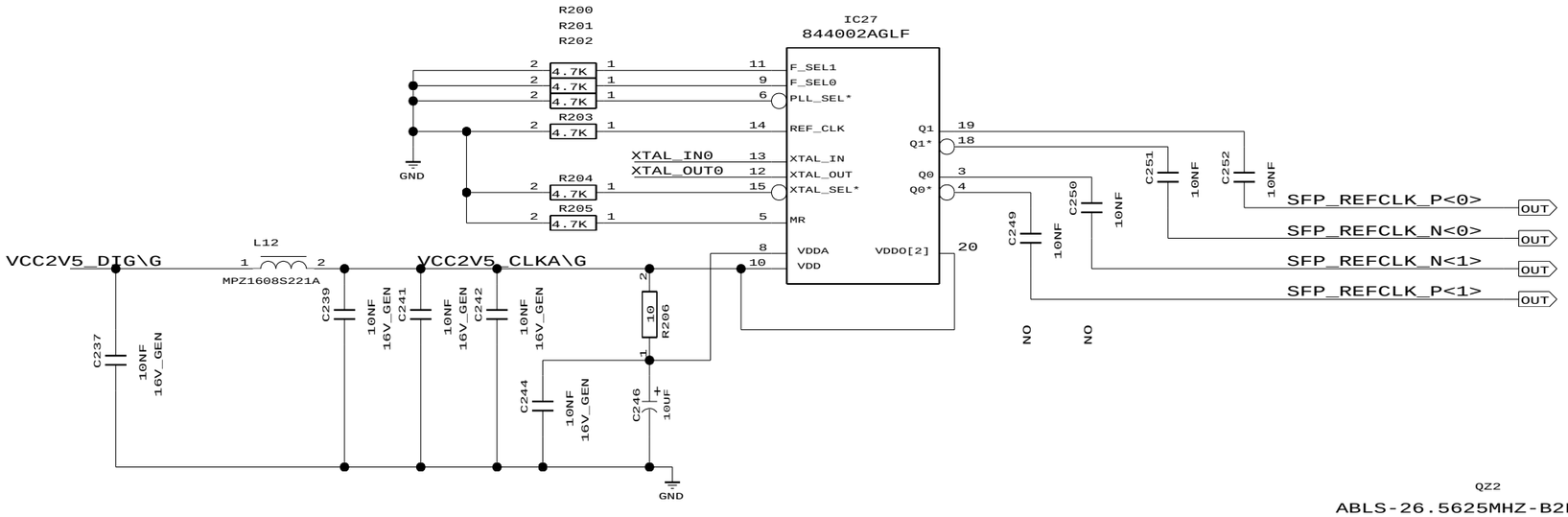
PROJECT:SRU v2.0

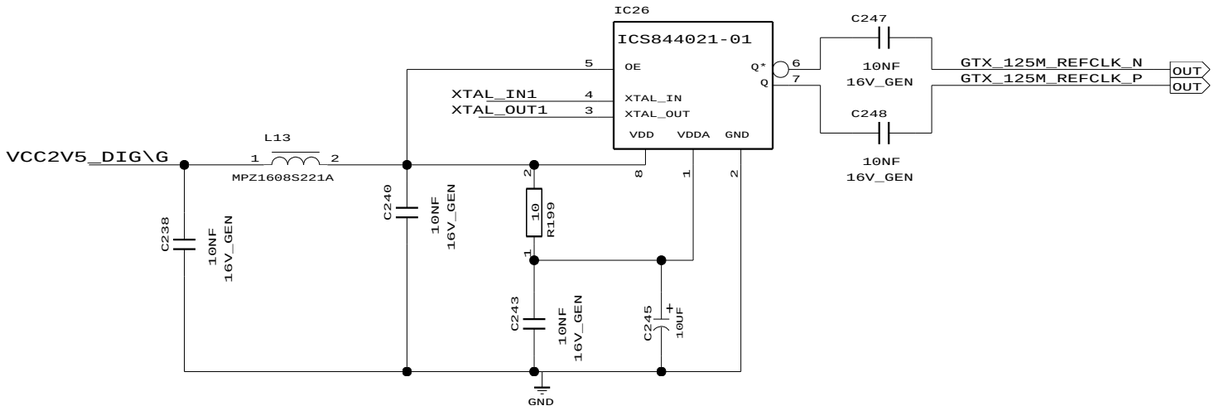
MODULE:sfp_plus

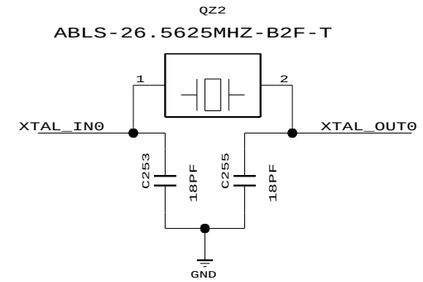
Sheet: Module: 1/1 Project: 18/81

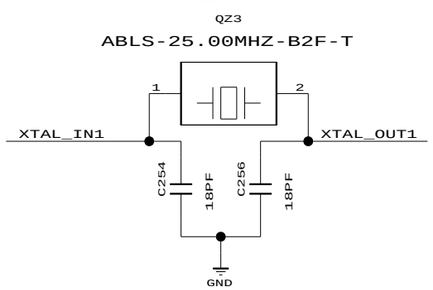
LAST_MODIFIED=Mon Dec 12 10:52:10 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010









NOTE FOR ICS844021-1 AND ICS844002

VDD,VDDA AND VDDO SHOULD BE INDIVIDUALLY CONNECTED TO POWER SUPPLY PLANE THROUGH VIA, AND ONE 10 NF CAP FOR EACH PIN.

Project file:sru_rev2.cpm SYSTEM:

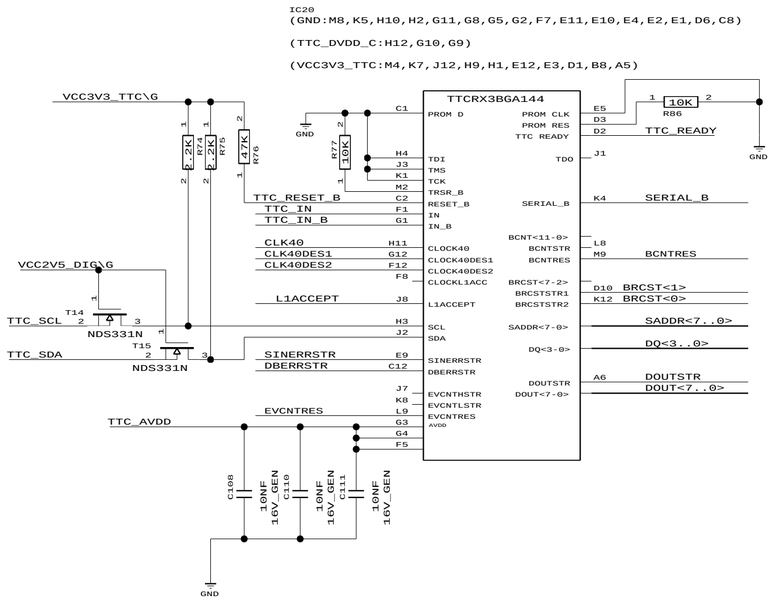
European Organization for Nuclear Research
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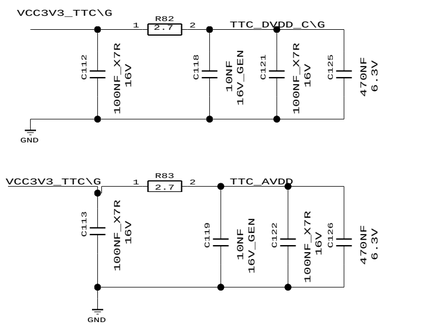
PROJECT:SRU v2.0

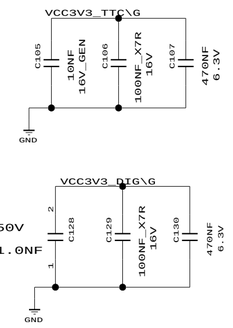
MODULE:sfp_clock | Sheet: 1/1 | Module: 1/1 | Project: 19/81

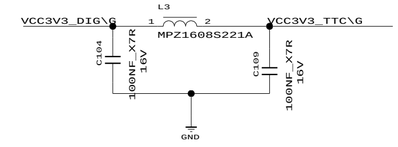
LAST_MODIFIED=Mon Dec 12 10:48:27 2011

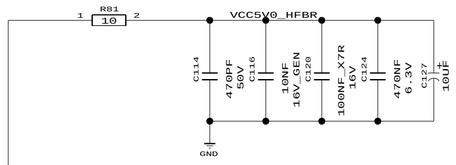
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

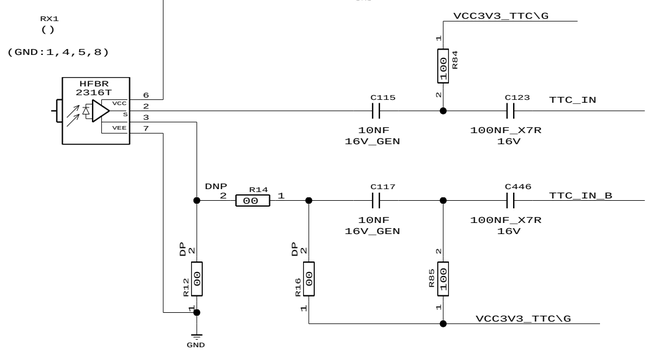


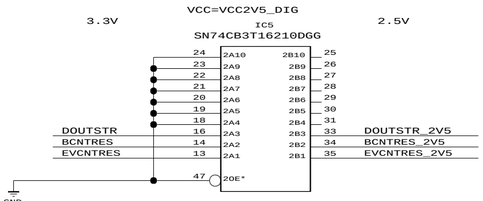


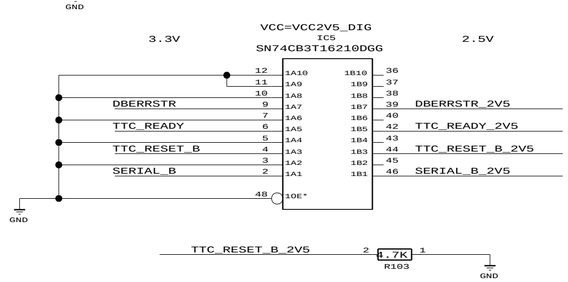


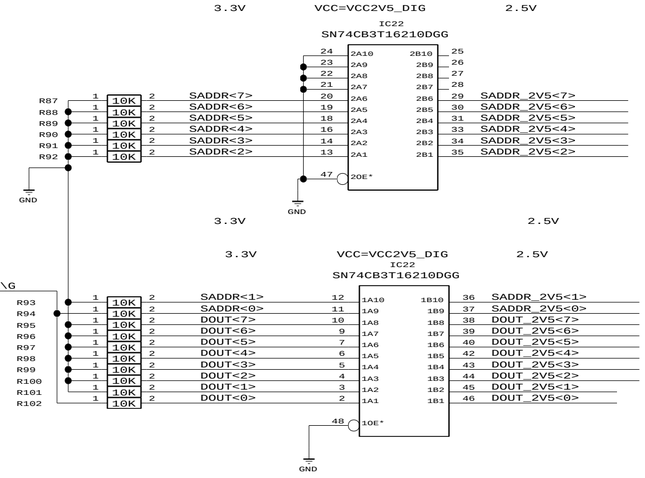










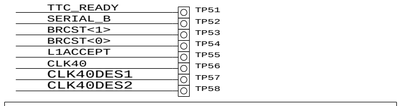


NOTE:

THE TTC_IN/TTC_IN_B SIGNALS MUST BE ROUTED

AS SHORT AS POSSIBLE TO THE TTC

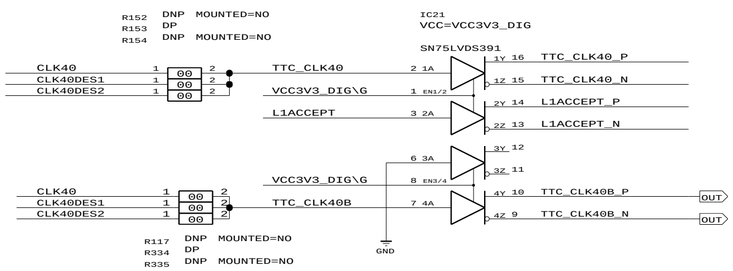
WITH MATCHED IMPEDANCE.

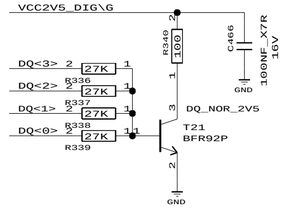


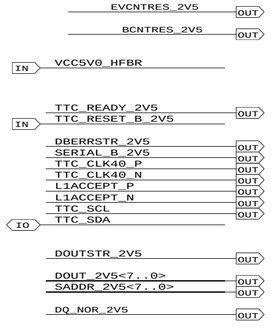
NOTE

PLACE SIG_NAME ON SILKSCRREN LAYER

CLOSE TO TP







2	TTC_IN CIRCUIT REVISED
	ADDED BCNTRES PORT

Project file:sru_rev2.cpm SYSTEM:

CERN TE/MPE European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND

PROJECT:SRU v2.0

MODULE:ttcrx Sheet: 1/1 Module: 1/1 Project: 20/81

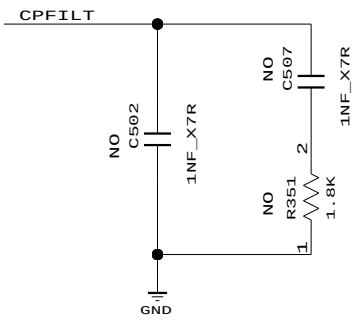
LAST_MODIFIED=Fri Dec 09 11:02:02 2011

Design by: FZhang/SMartoiu PCB by: EXT DATE: 29/07/2010

PLACE CLOSE TO IC
DNP FOR DS10CP152
DP FOR DS90CP22

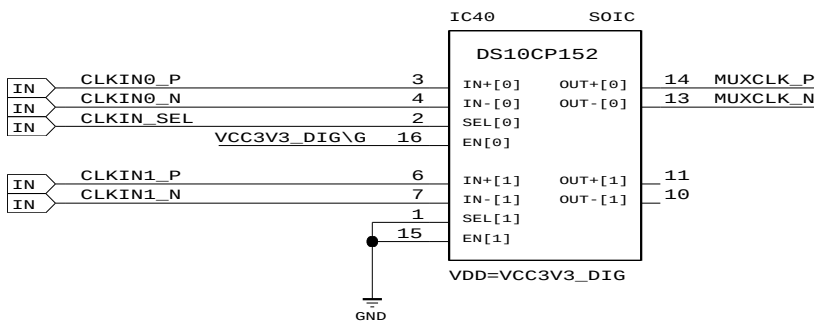
CLKIN0_P — R342 NO — CLKIN0_N
CLKIN1_P — R343 NO — CLKIN1_N

EXTERNAL PLL FILTER



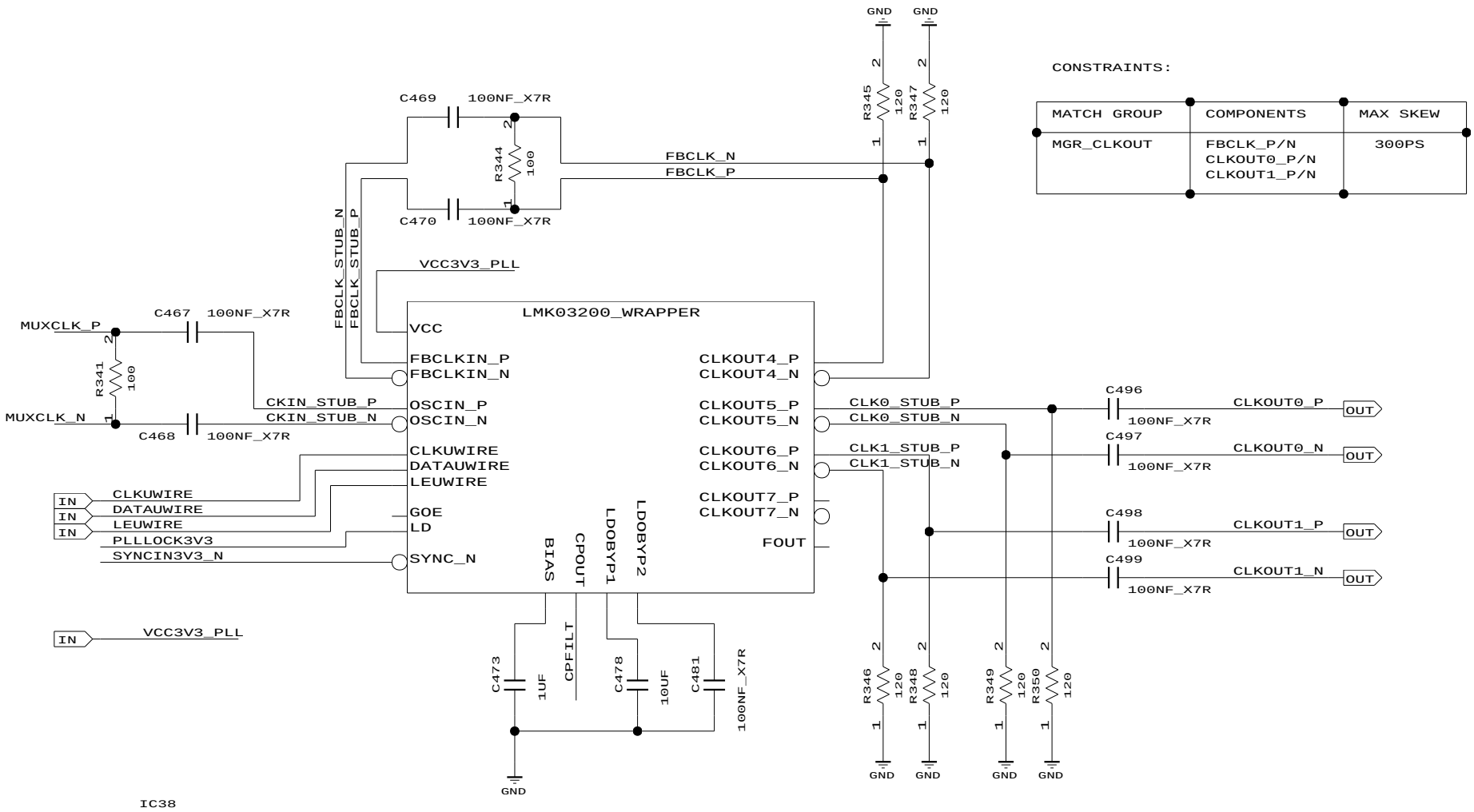
VALUES TO BE DECIDED

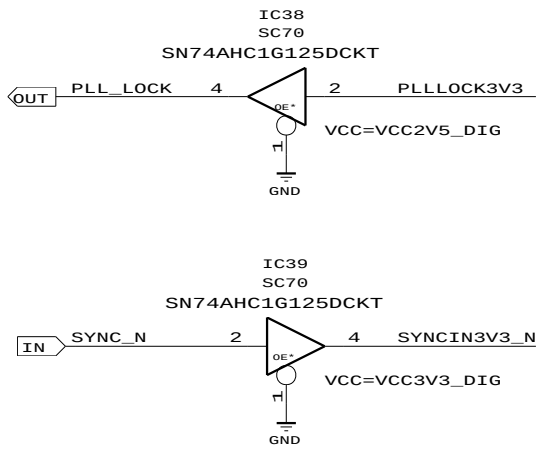
IC40 SOIC — DS10CP152

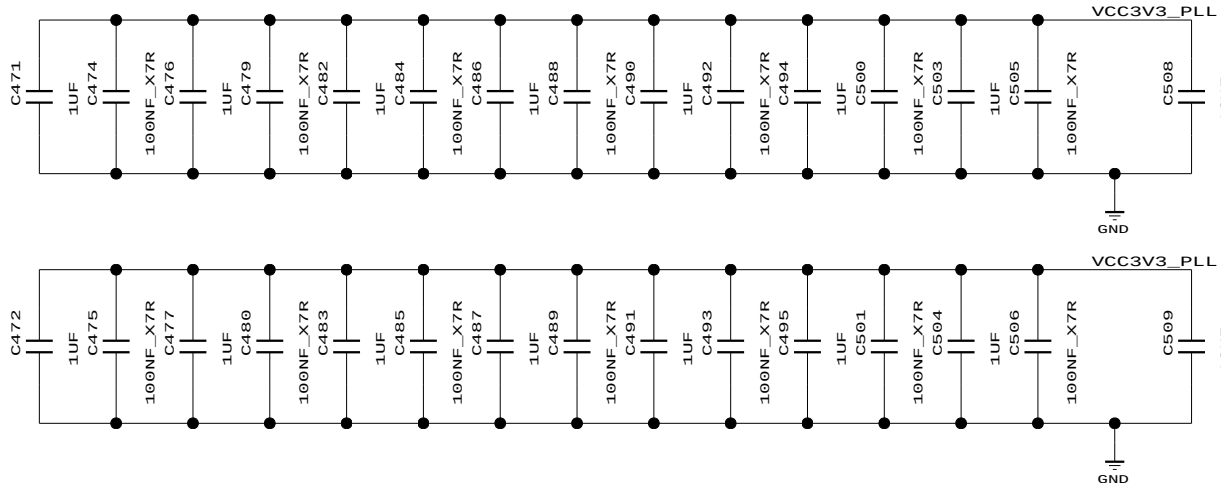


CONSTRAINTS:

MATCH GROUP	COMPONENTS	MAX SKEW
MGR_CLKOUT	FBCLK_P/N CLKOUT0_P/N CLKOUT1_P/N	300PS







Project file:sru_rev2.cpm — SYSTEM:

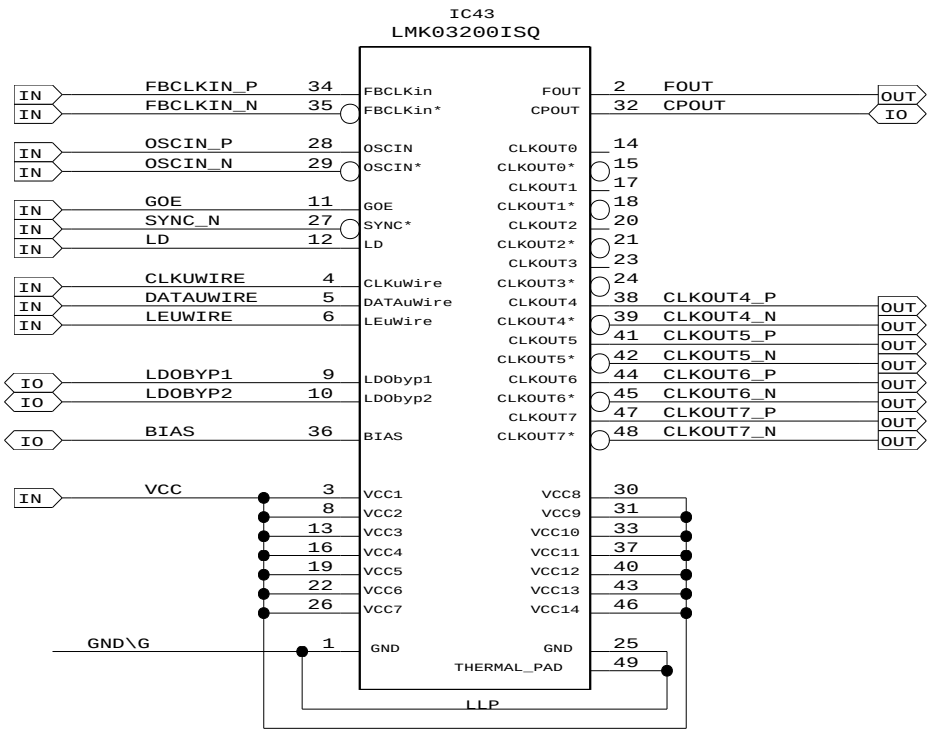
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TS/DEM

PROJECT:SRU v2.0

MODULE:jitter_cleaner — Sheet: Module: 1/1 Project: 21/81

LAST_MODIFIED=Fri Dec 09 11:02:09 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010



Project file:sru_rev2.cpm

SYSTEM:

PROJECT:SRU v2.0

MODULE:lmk03200_wrapper2

Sheet: Module: 1/1 Project: 22/81

LAST_MODIFIED=Fri Dec 09 11:02:11 2011

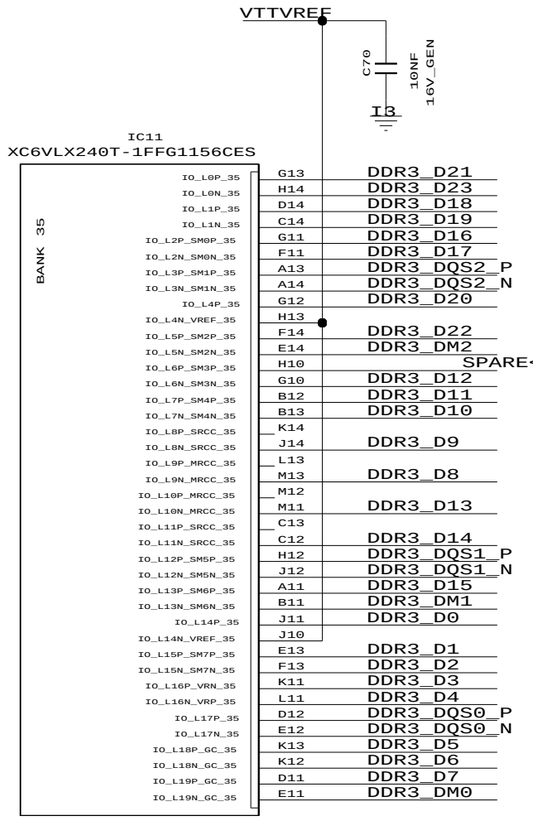
Design by: FZhang/SMartoiu

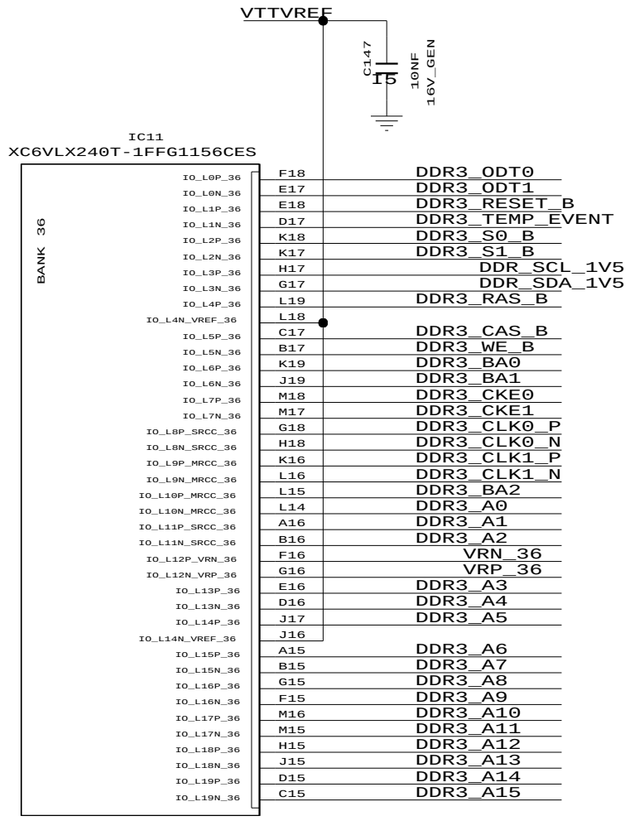
PCB by: EXT

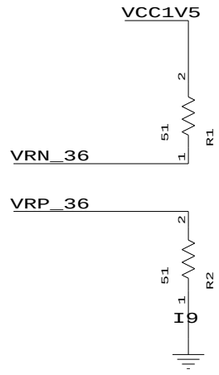
DATE: 29/07/2010

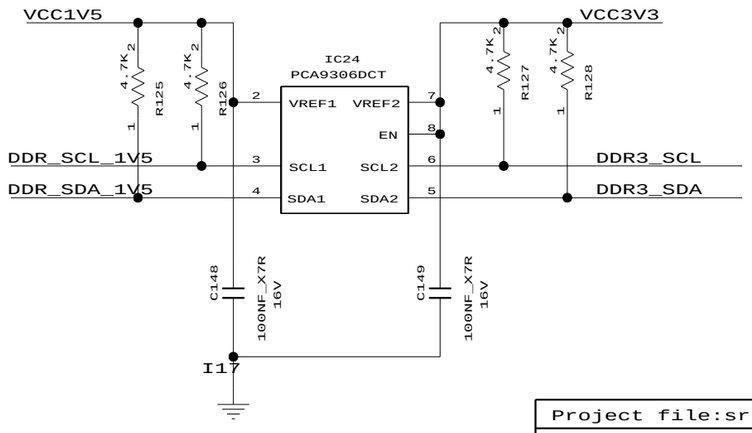
TS/DEM

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for Nuclear Research
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SWITZERLAND









Project file:sru_rev2.cpm SYSTEM:

TE/MPE

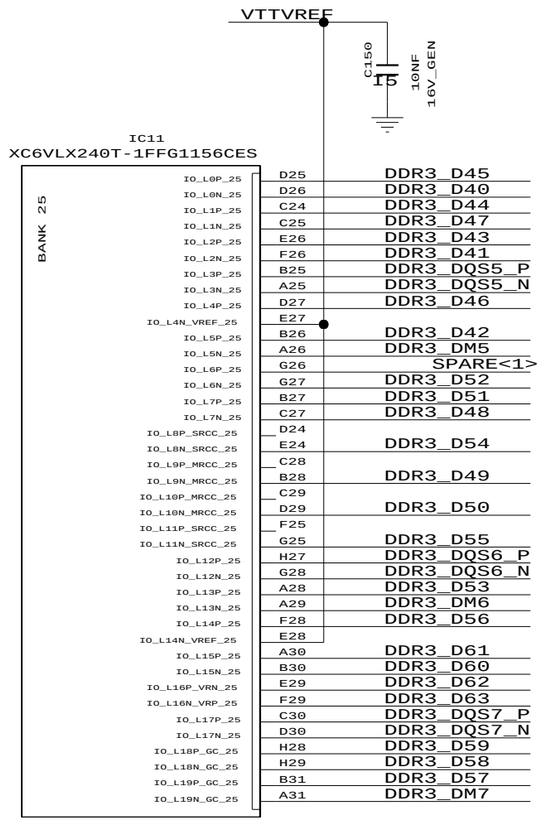
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

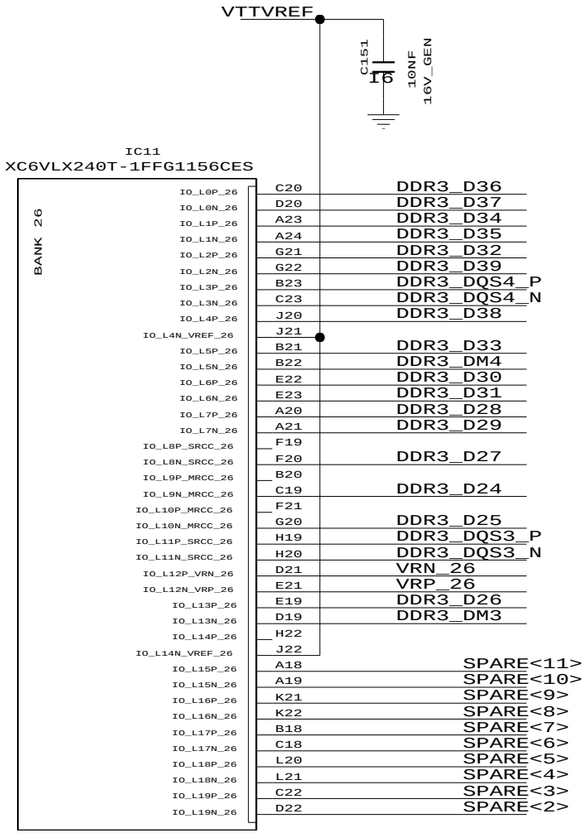
PROJECT:SRU v2.0

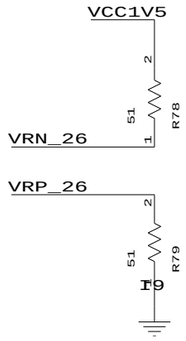
MODULE:ddr3_interface Sheet: 1/4 Module: Project: 23/81

LAST_MODIFIED=Fri Dec 09 11:02:05 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010







Project file:sru_rev2.cpm SYSTEM:

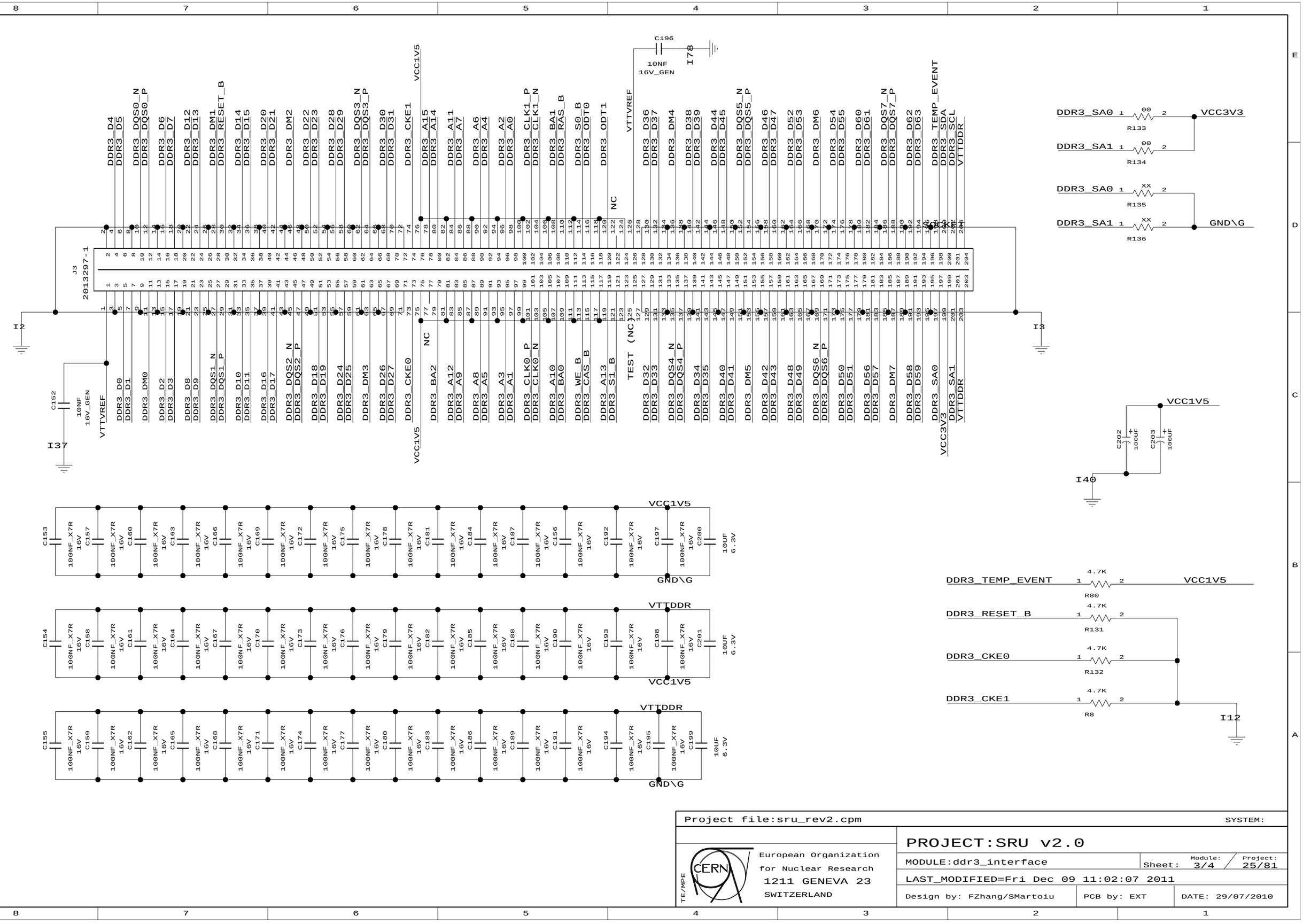
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

PROJECT:SRU v2.0

MODULE:ddr3_interface Sheet: 2/4 Module: Project: 24/81

LAST_MODIFIED=Fri Dec 09 11:02:06 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010



Project file:sru_rev2.cpm SYSTEM:

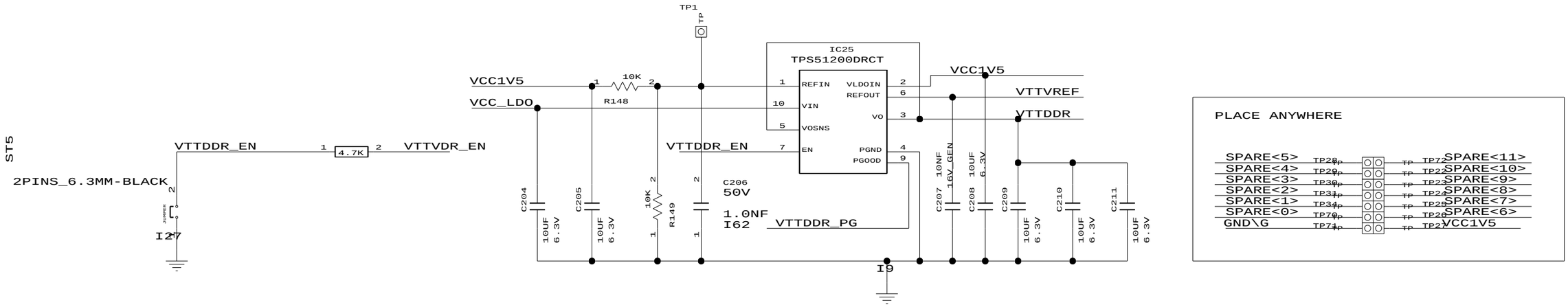
European Organization
for Nuclear Research
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SWITZERLAND
TE/MPE

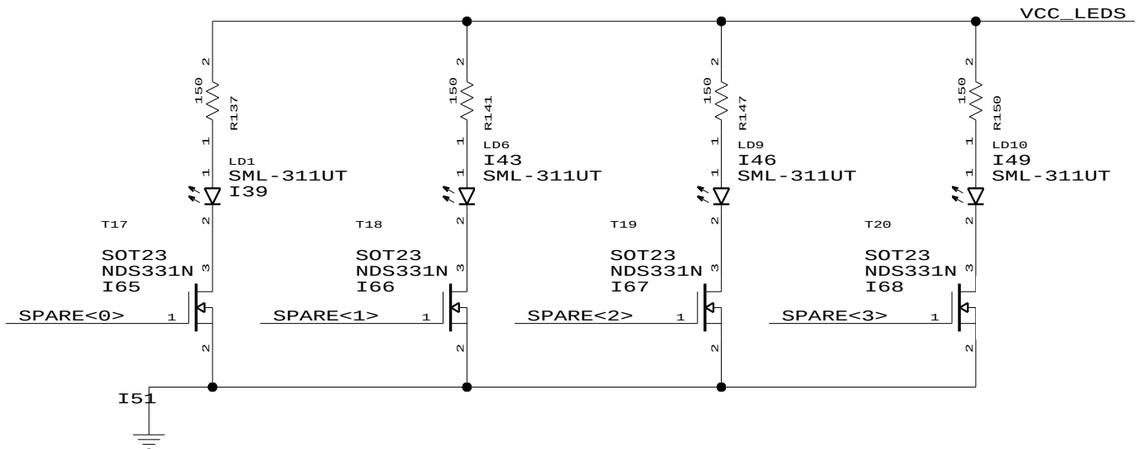
PROJECT:SRU v2.0

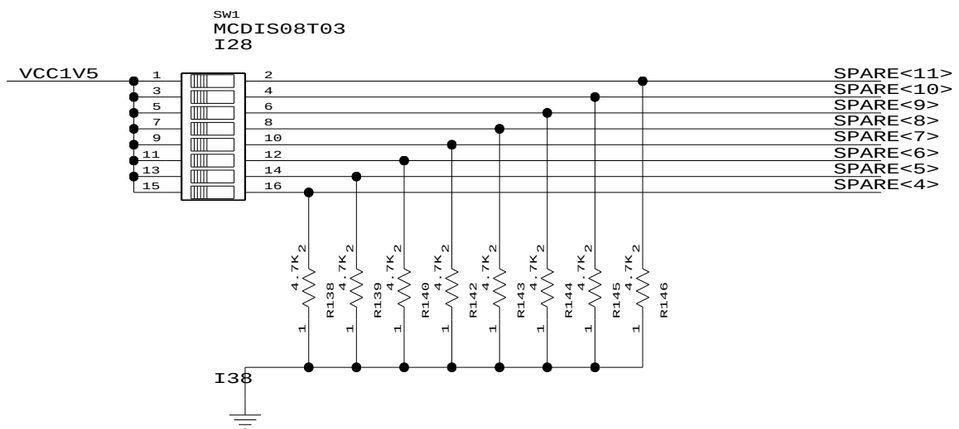
MODULE:ddr3_interface Sheet: 3/4 Module: 3/4 Project: 25/81

LAST_MODIFIED=Fri Dec 09 11:02:07 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010







IO SPARE<11:0>

IN VCC1V5

IN VCC3V3

IN VCC_LEDS

IN VCC_LDO

IN VTTVDR_EN

OUT VTTDDR_PG

Project file:sru_rev2.cpm SYSTEM:

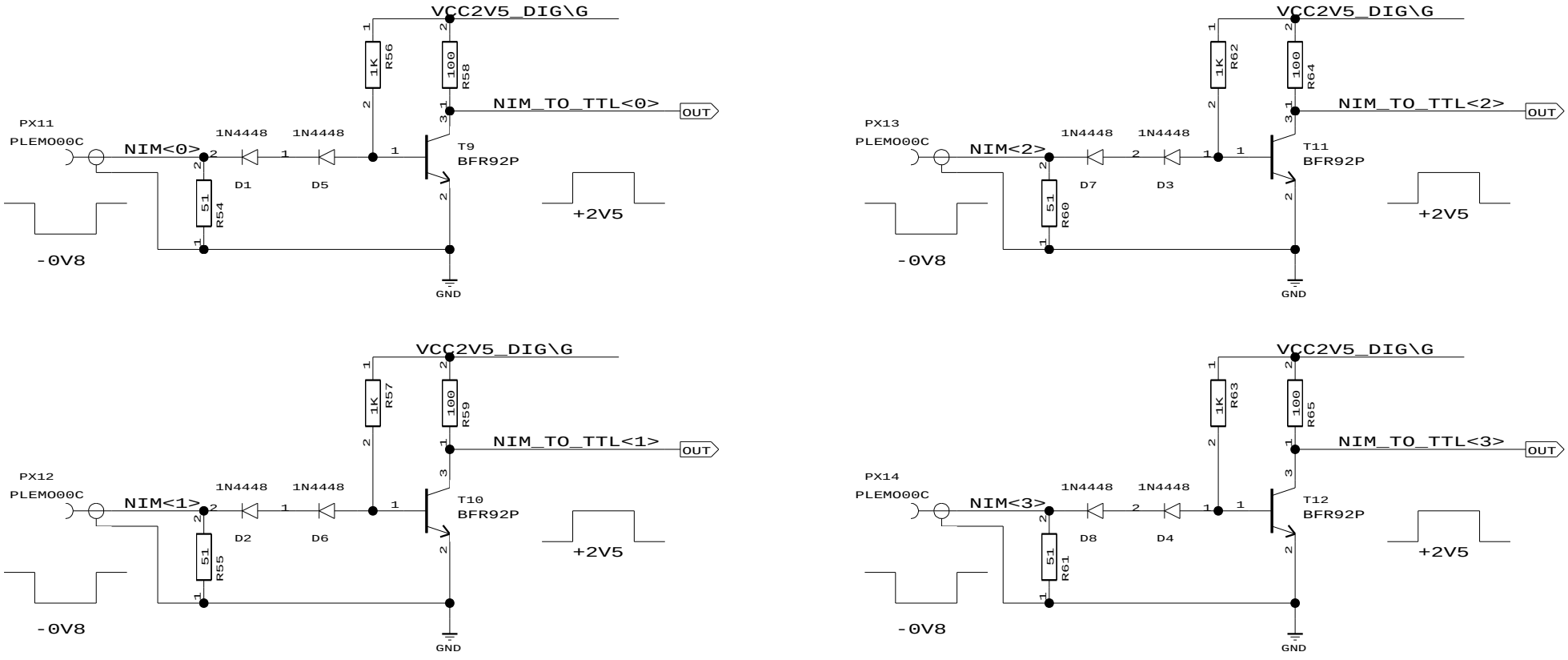
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CERN
European Organization
for Nuclear Research
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SWITZERLAND

PROJECT:SRU v2.0

MODULE:ddr3_interface Sheet: 4/4 Module: 4/4 Project: 26/81

LAST_MODIFIED=Fri Dec 09 11:02:06 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010



Note

100R pull up resistor value need to be verify

Project file:sru_rev2.cpm

SYSTEM:

PROJECT:SRU v2.0

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TE/MPE

MODULE:nim_input

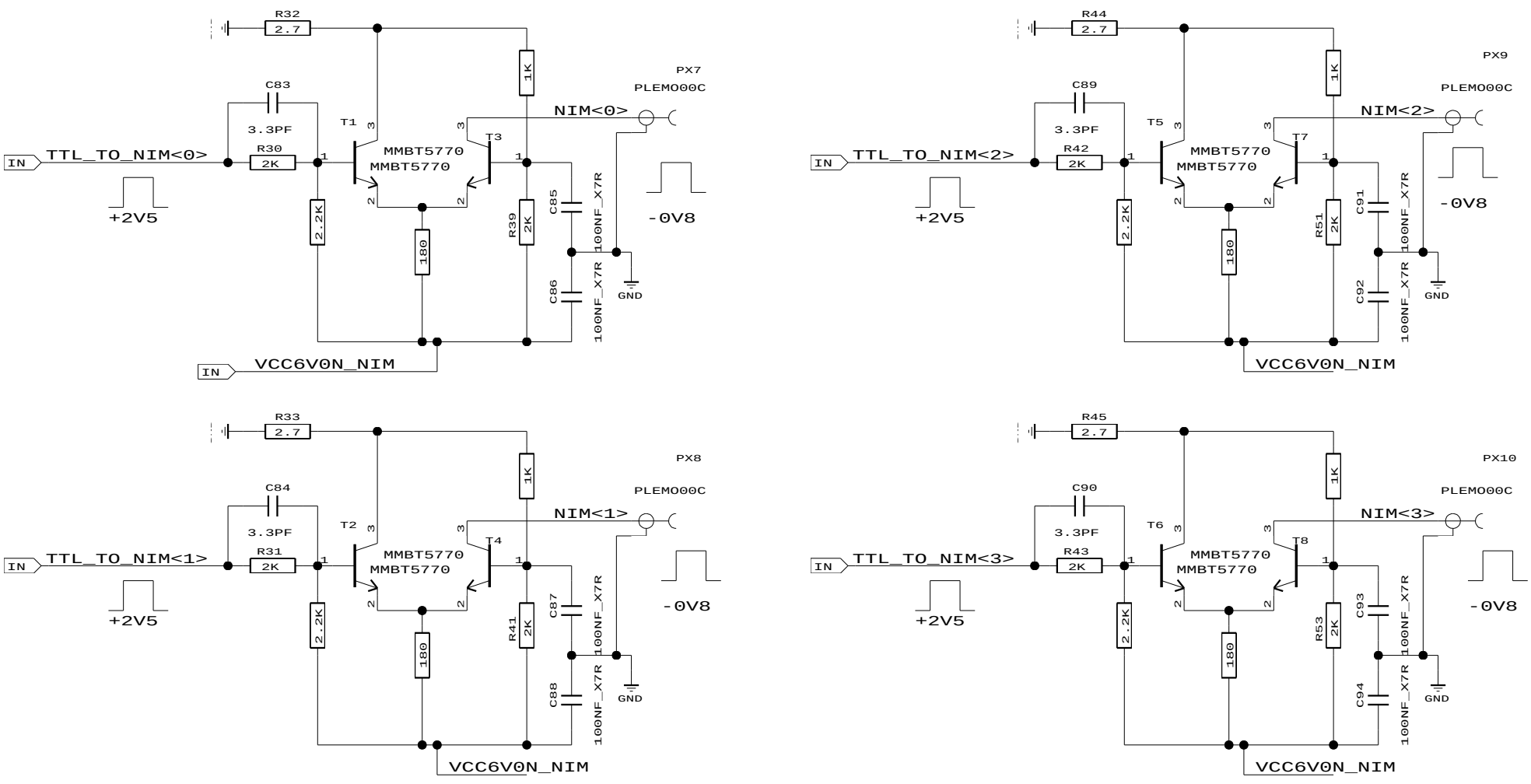
Sheet: Module: 1/1 Project: 27/81

LAST_MODIFIED=Fri Dec 09 11:01:48 2011

Design by: FZhang/SMartoiu

PCB by: EXT

DATE: 29/07/2010



Note:
NIM<3..0> must be
terminated with 50 Ohm

Project file:sru_rev2.cpm

SYSTEM:

TE/MPE

CERN

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

PROJECT:SRU v2.0

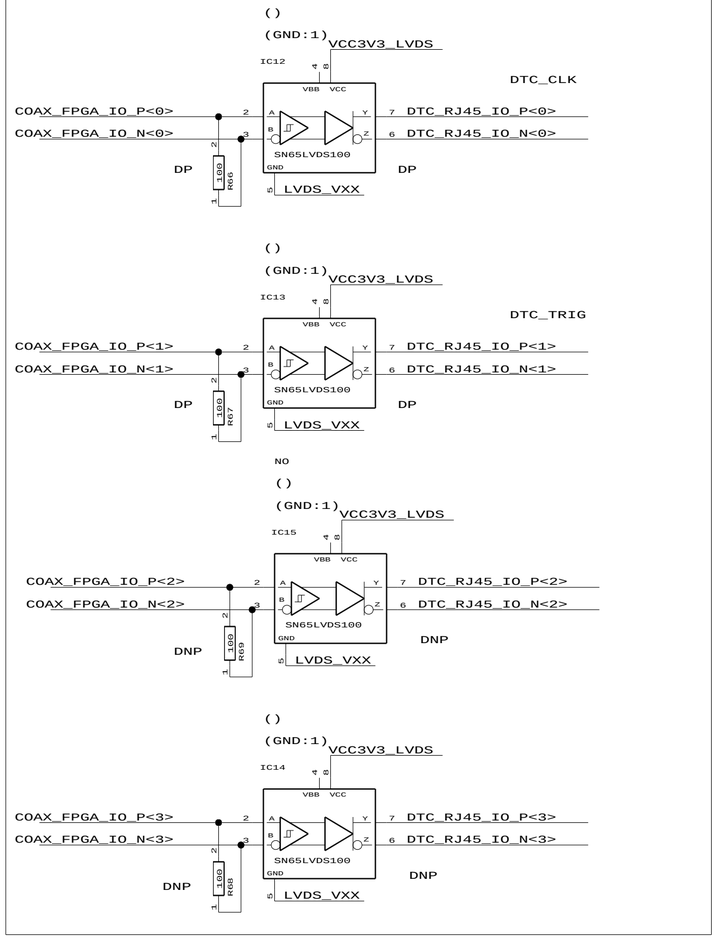
MODULE:nim_output

Sheet: Module: 1/1 Project: 28/81

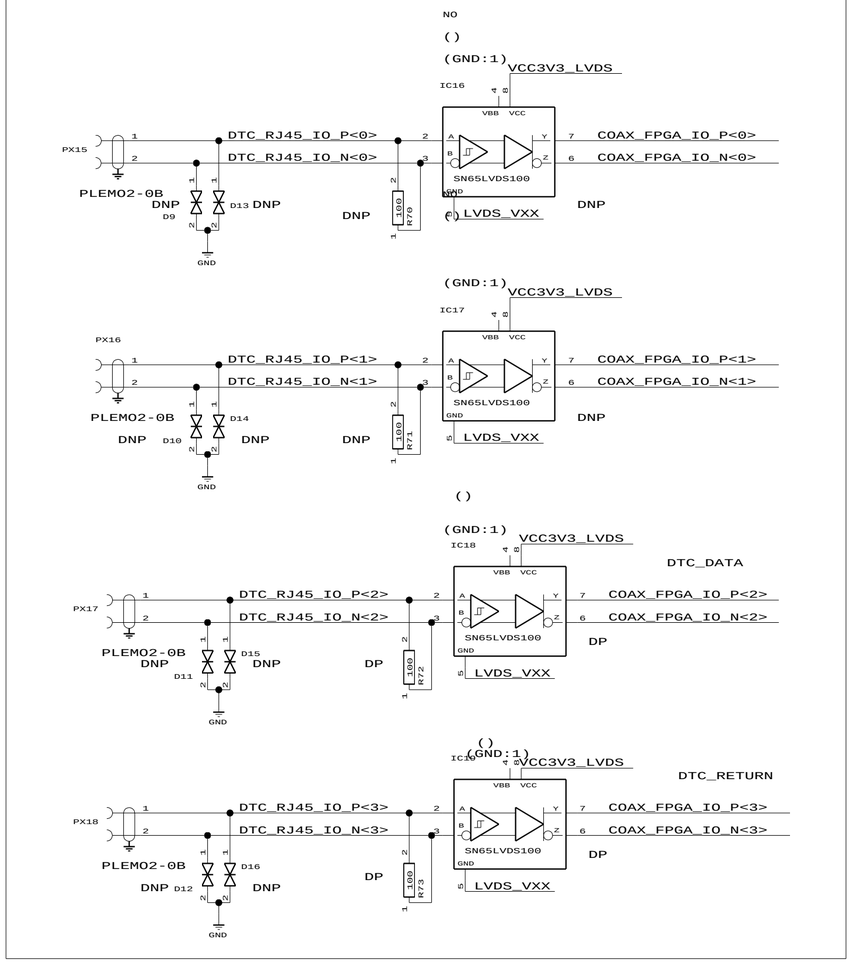
LAST_MODIFIED=Fri Dec 09 11:01:47 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

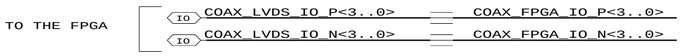
OUTPUTS

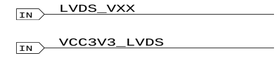


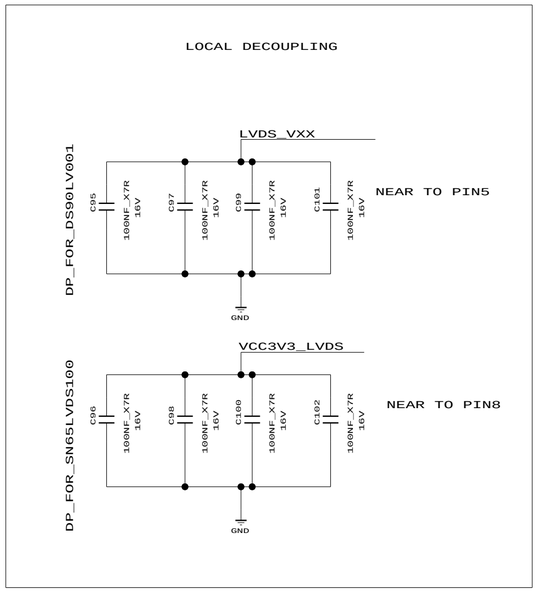
INPUTS

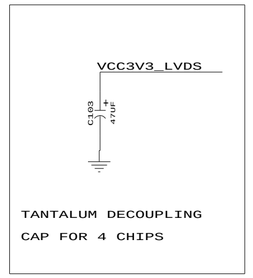


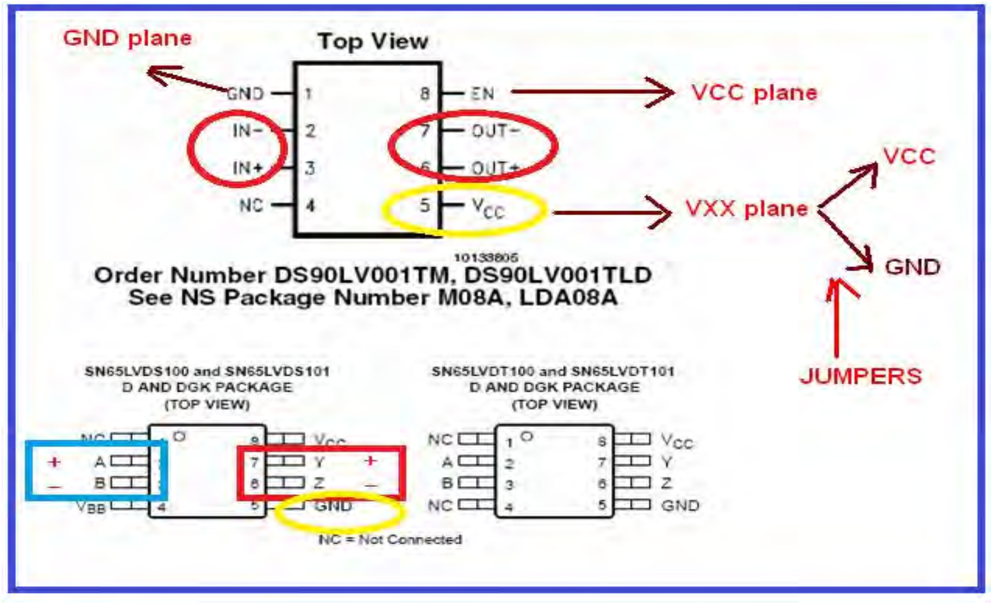
TO THE FPGA











- Only mount RIGHT or LEFT chip.
- Place the chips one direction on TOP, the other direction on BOTTOM, and depending on the bill of material the connection to the connector will be a IN or OUT.
- 100 Ohm termination resistor should be placed near input or after.
- All DIFF. PAIRS set to 100 Ohm and keep the skew no more than 250 mils.
- Two local decoupling capacitor for each mounted chip. One capacitor is placed near PIN 5, one capacitor is placed near PIN 8.
- One ESD diode per differential line from connector.

Project file:sru_rev2.cpm SYSTEM:

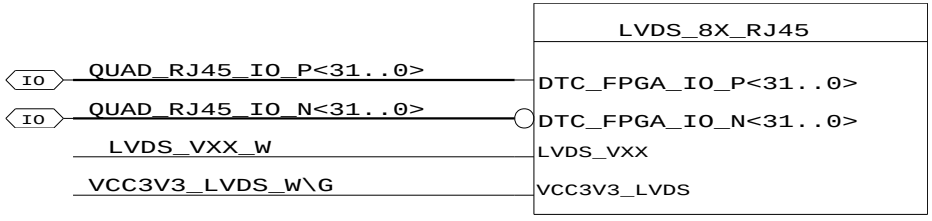
PROJECT:SRU v2.0

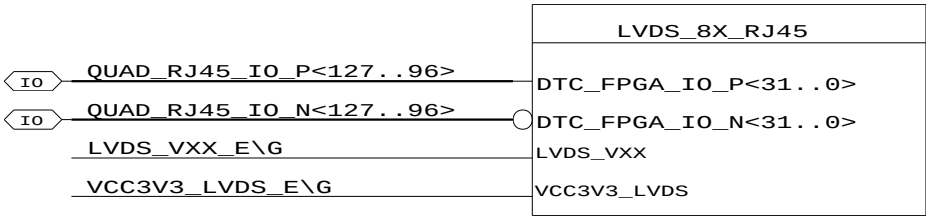
MODULE:lvds_coax Sheet: 1/1 Module: Project: 29/81

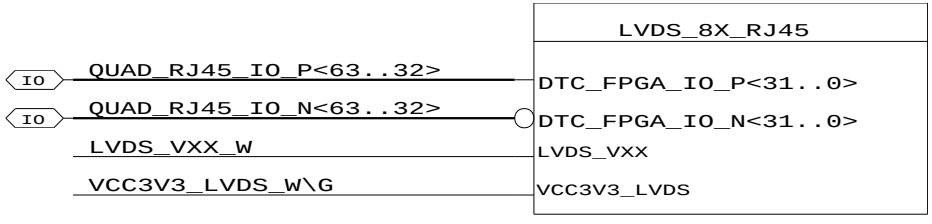
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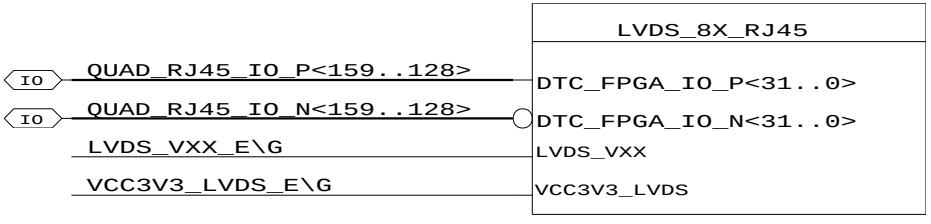
Design by: FZhang/SMartoiu PCB by: EXT DATE: 29/07/2010

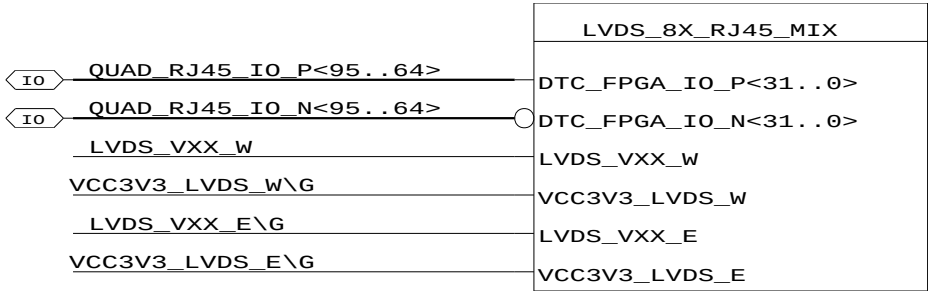
TE/MPE
CERN
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

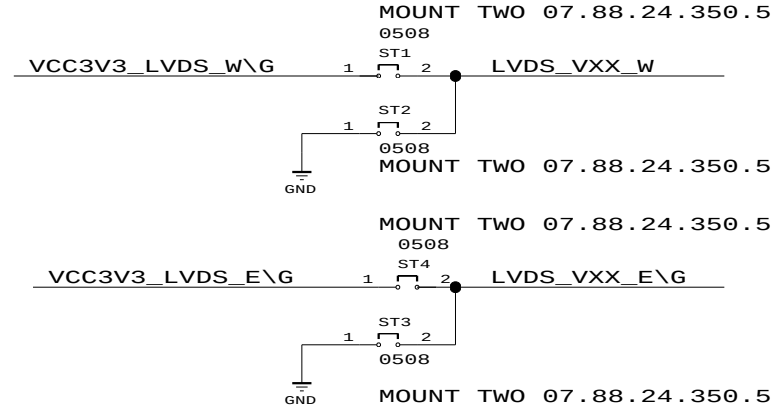












NOTE:

JUMPER SETTING FOR TWO KIND OF LVDS CHIPS

1. FOR SN65LVDS100D: SHORT ST2 AND ST3
2. FOR DS90LV001TM-ND: SHORT ST1 AND ST4

Project file:sru_rev2.cpm SYSTEM:

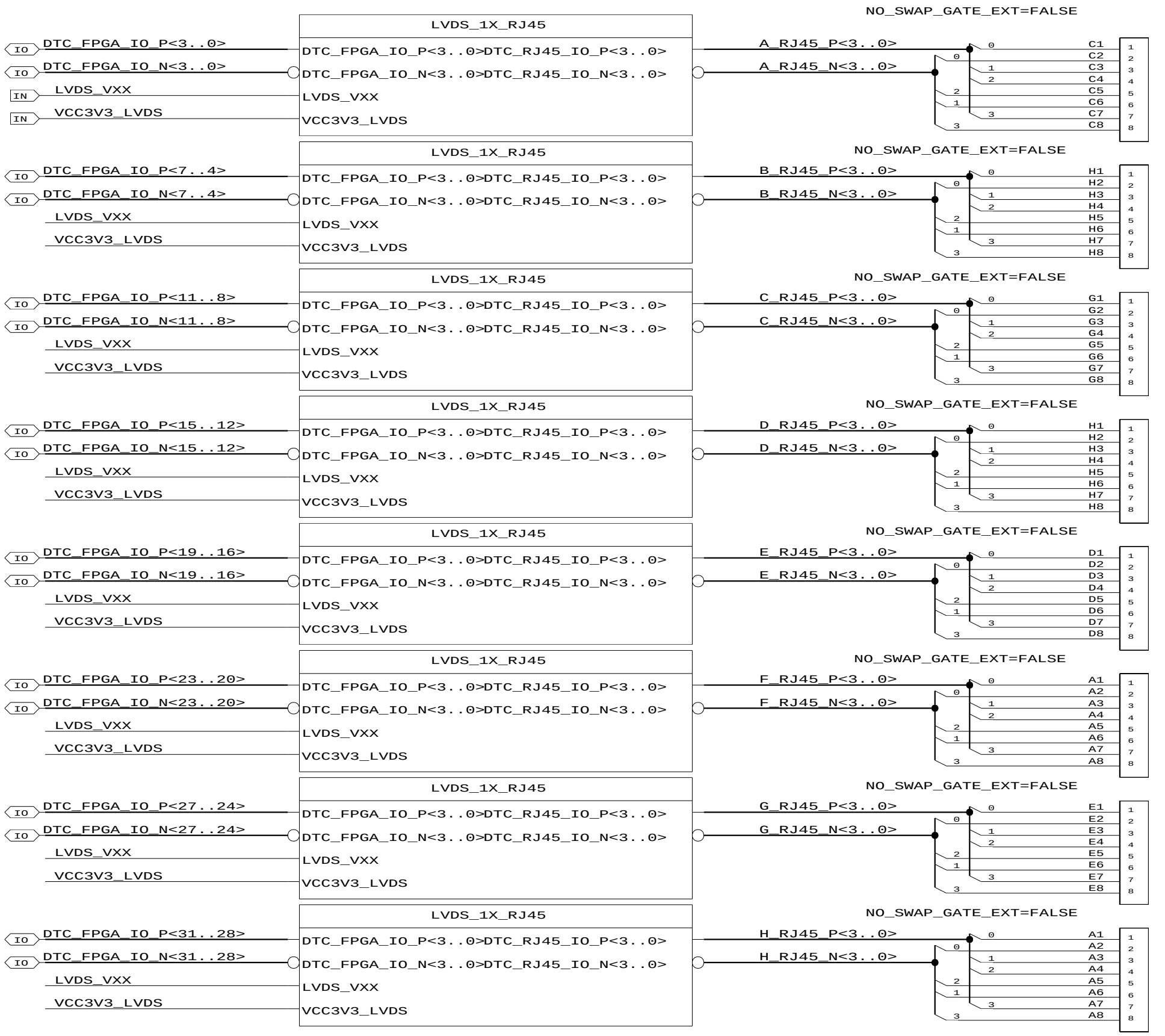
CERN
TE/MPE
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

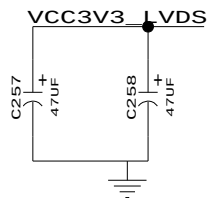
PROJECT:SRU v2.0

MODULE:lvds_40x_rj45 Sheet: Module: 1/1 Project: 30/81

LAST_MODIFIED=Fri Dec 09 11:01:51 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010





PLACE THIS DECOUPLING CAPACITORS
AROUND THE AROUND THE AREA
OF THIS 2*4 RJ45

Project file:sru_rev2.cpm

SYSTEM:

PROJECT:SRU v2.0

MODULE:lvds_8x_rj45

Sheet: Module: 1/1 Project: 31/81

LAST_MODIFIED=Fri Dec 09 11:01:52 2011

Design by: FZhang/SMartoiu

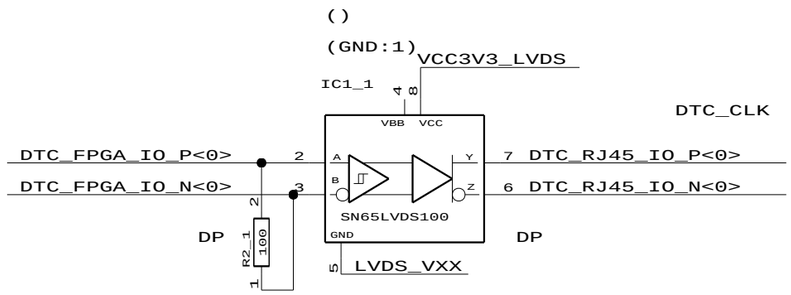
PCB by: EXT

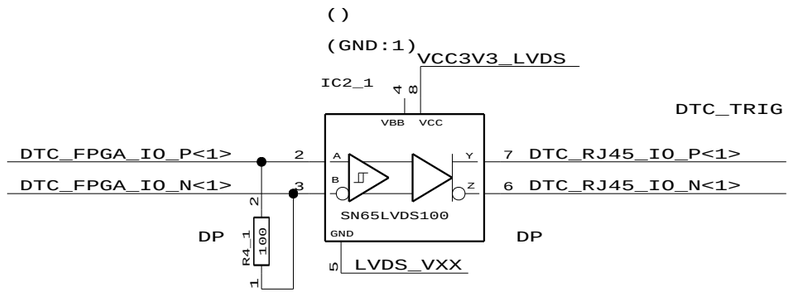
DATE: 29/07/2010

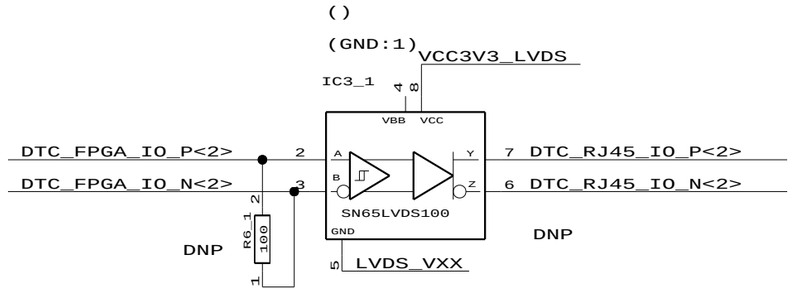
TS/DEM

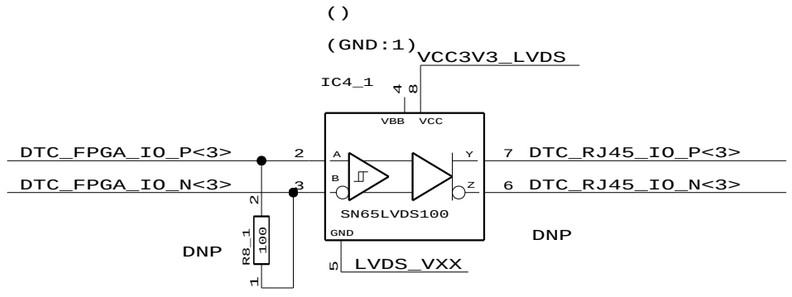
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

OUTPUTS

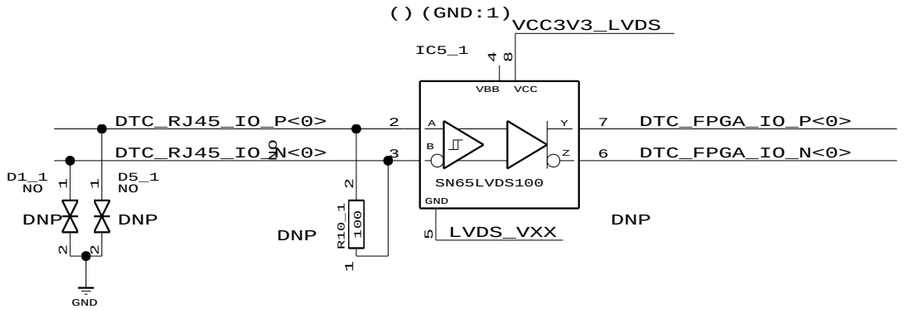


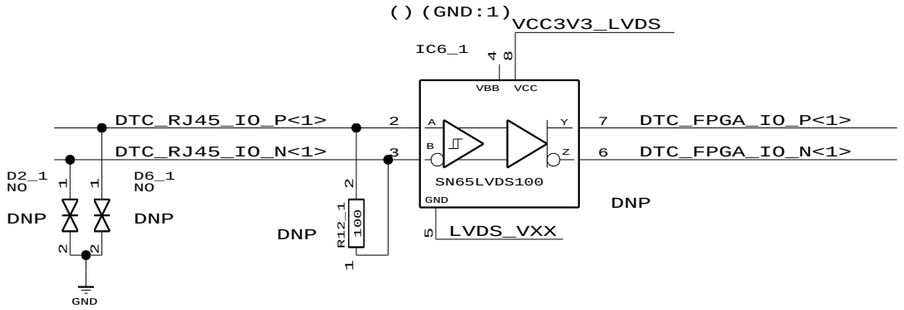


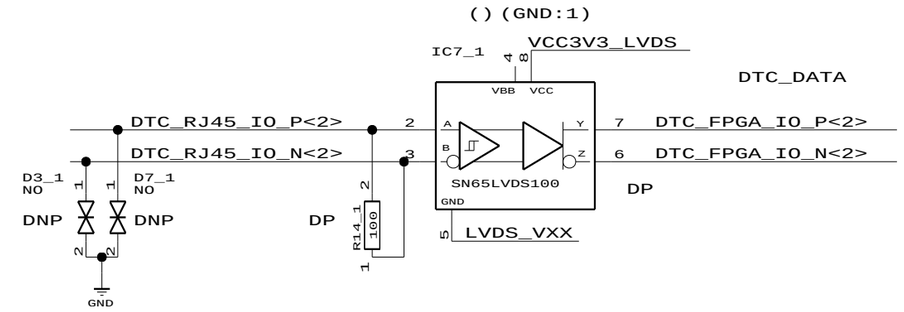


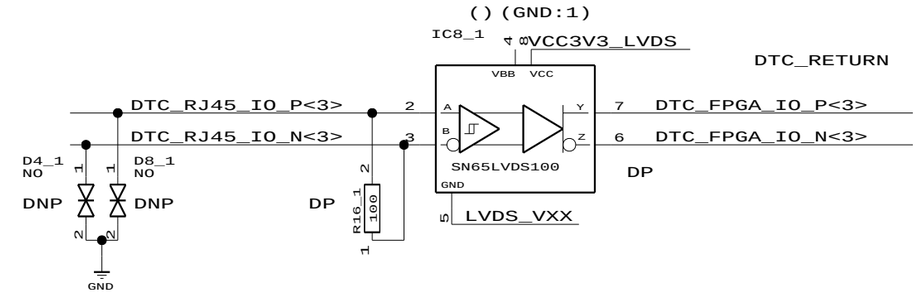


INPUTS

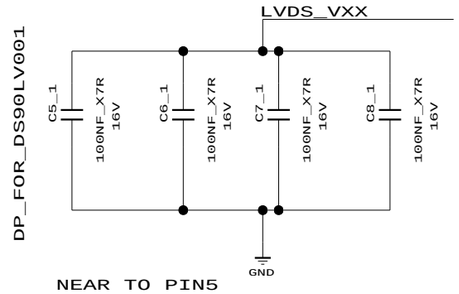


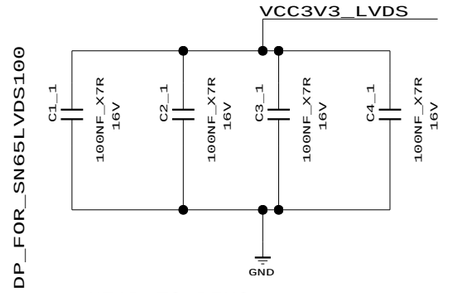






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

TE/MPE

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SWITZERLAND

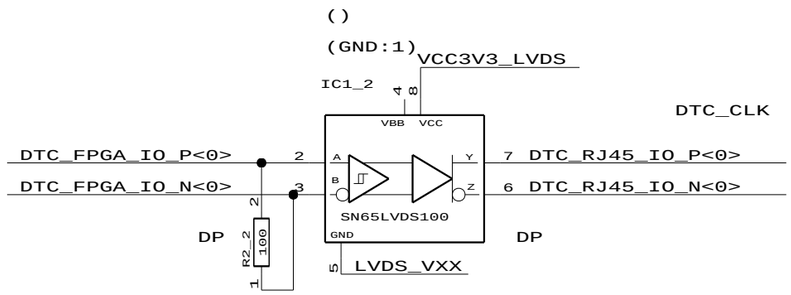
PROJECT:SRU v2.0

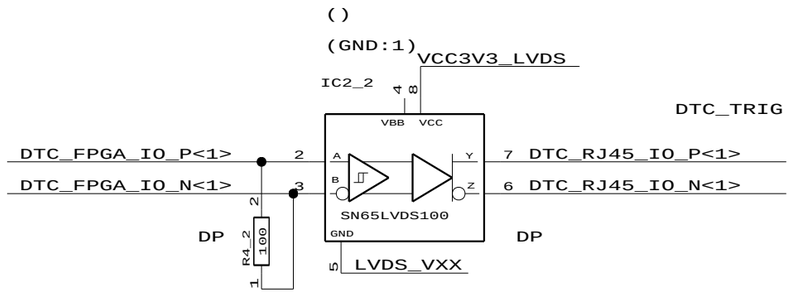
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 32/81

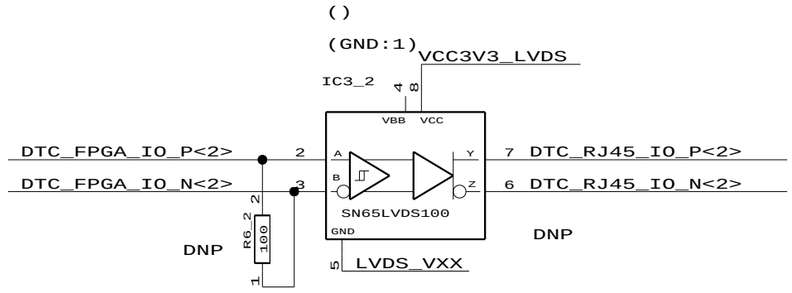
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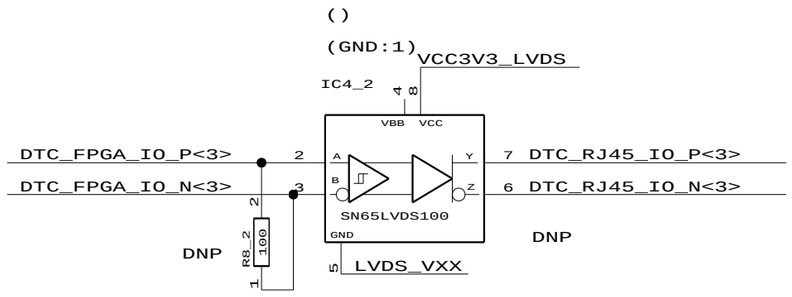
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

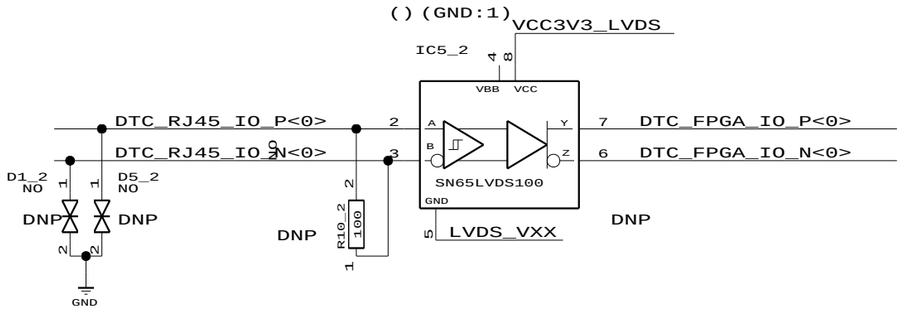


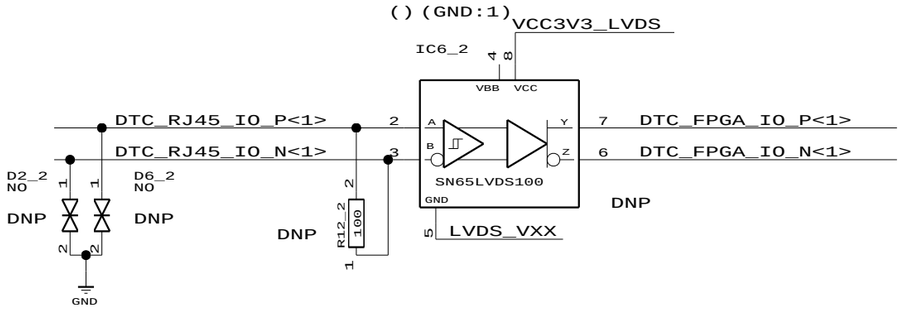


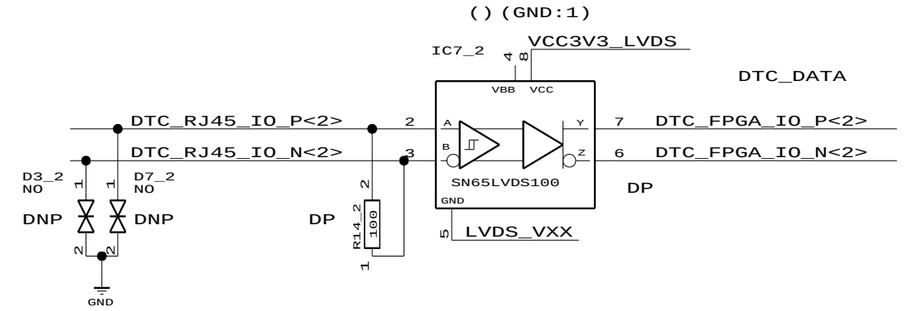


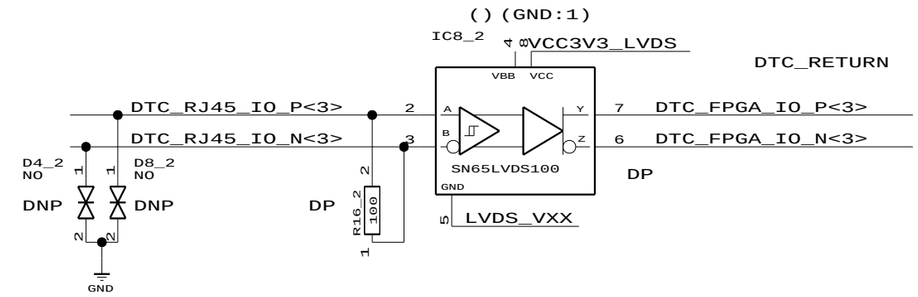


INPUTS

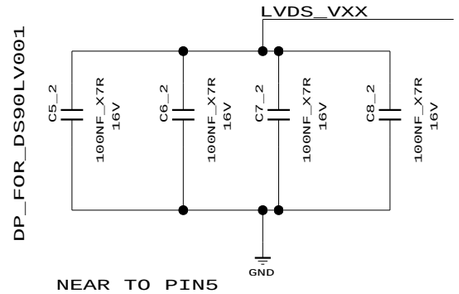


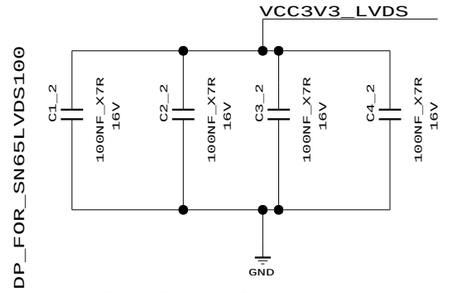






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

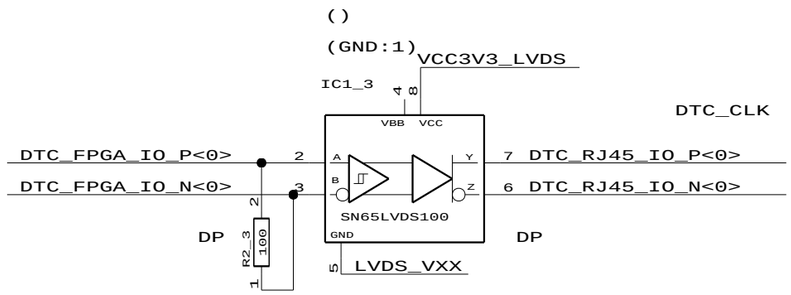
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

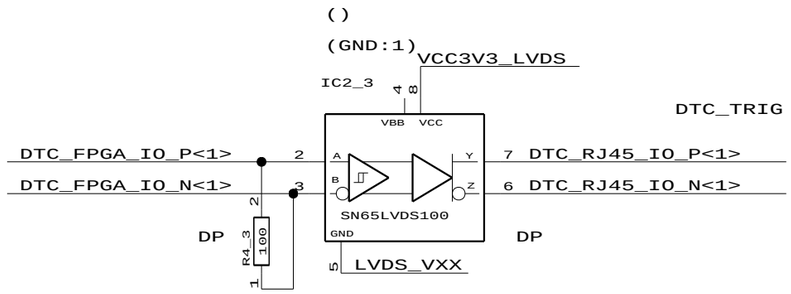
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 33/81

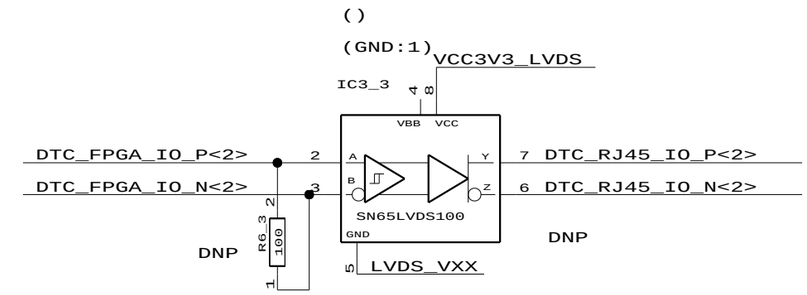
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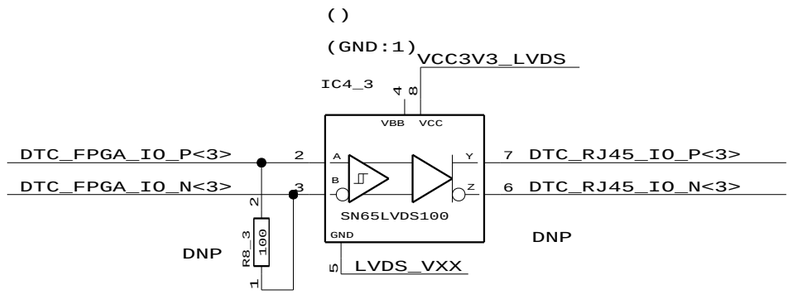
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

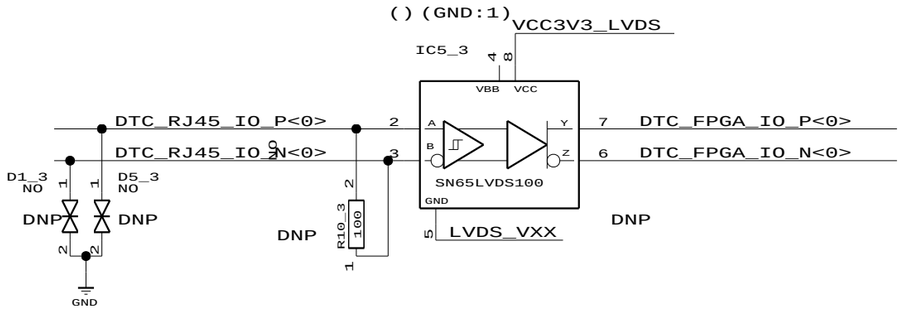


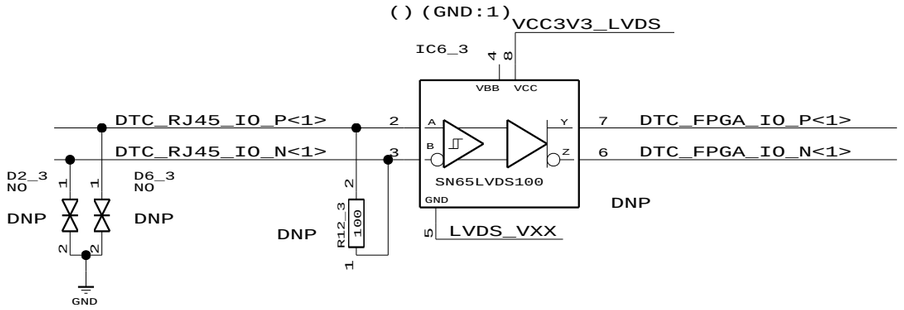


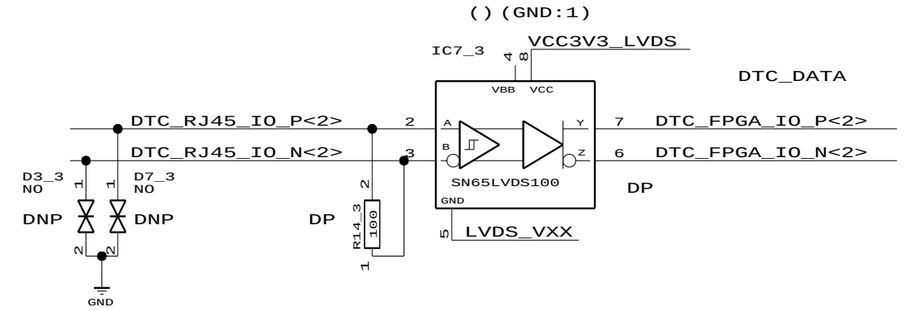


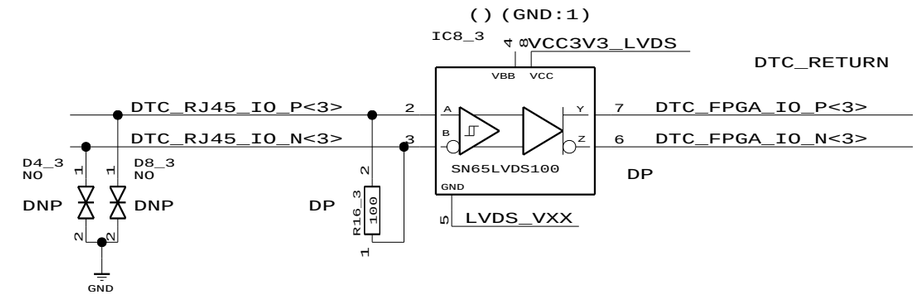


INPUTS

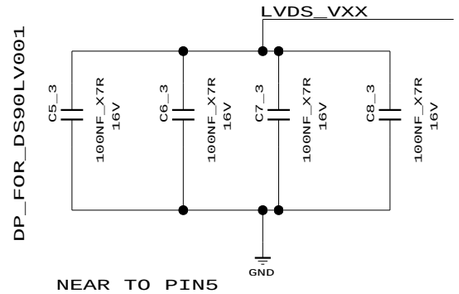


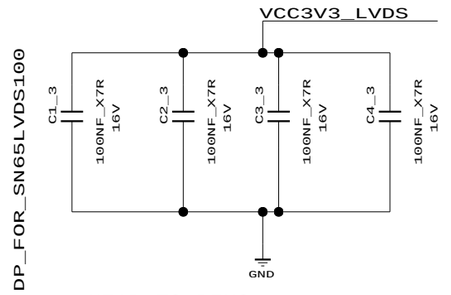






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

TE/MPE

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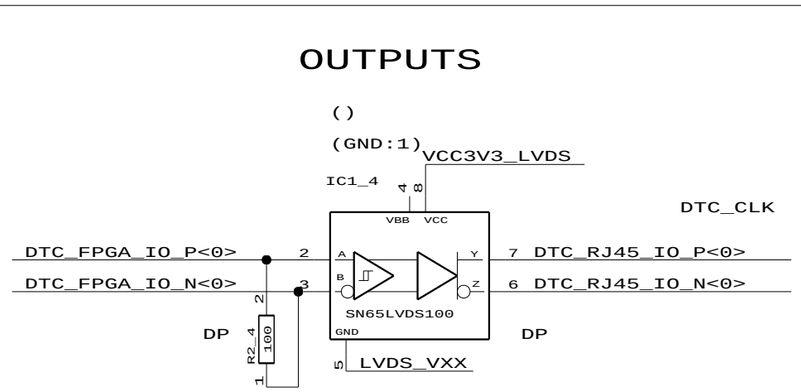
PROJECT:SRU v2.0

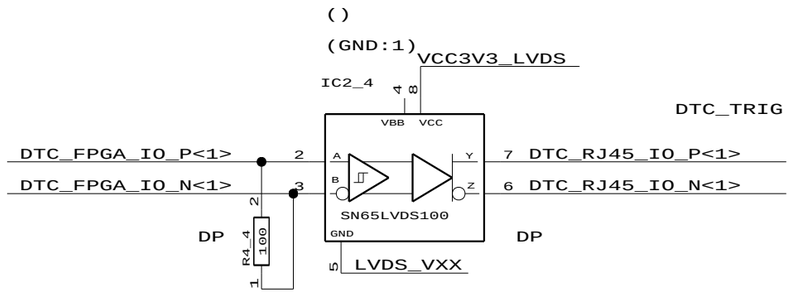
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: Project: 34/81

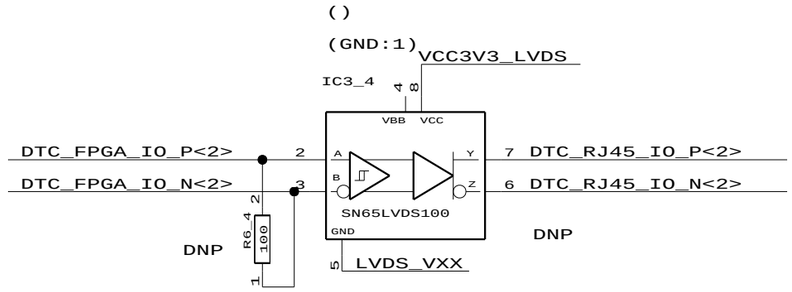
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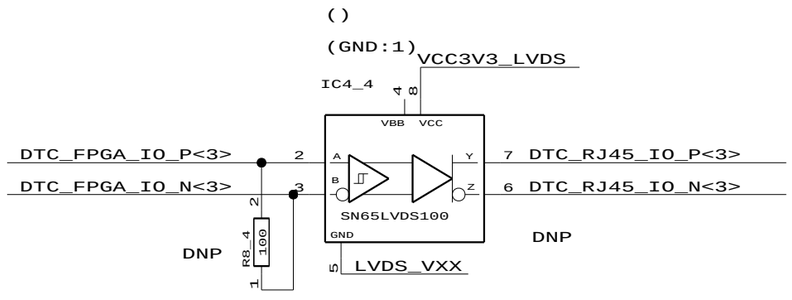
Design by: FZhang/SMartoiu PCB by: EXT DATE: 29/07/2010

OUTPUTS

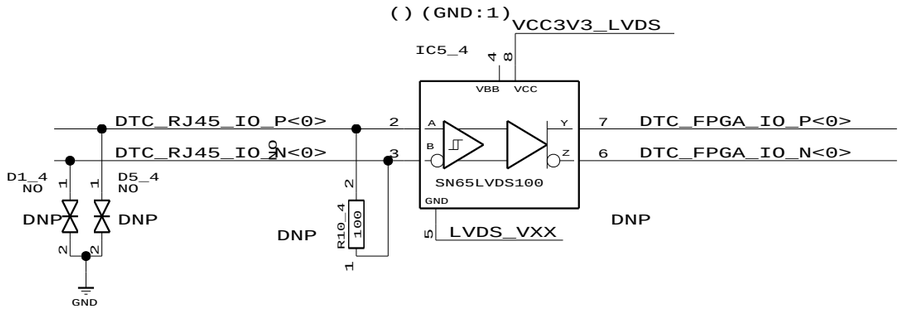


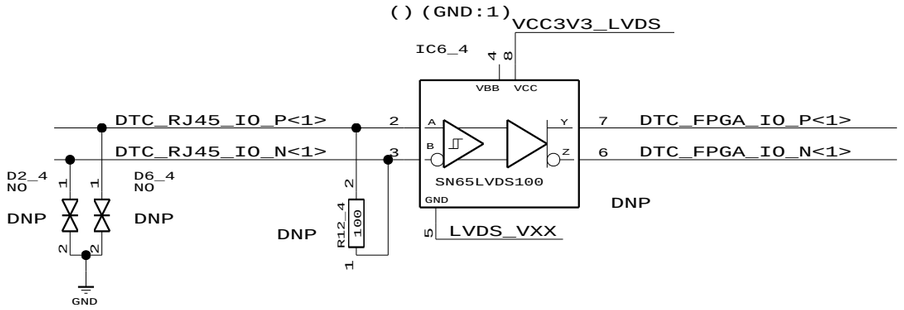


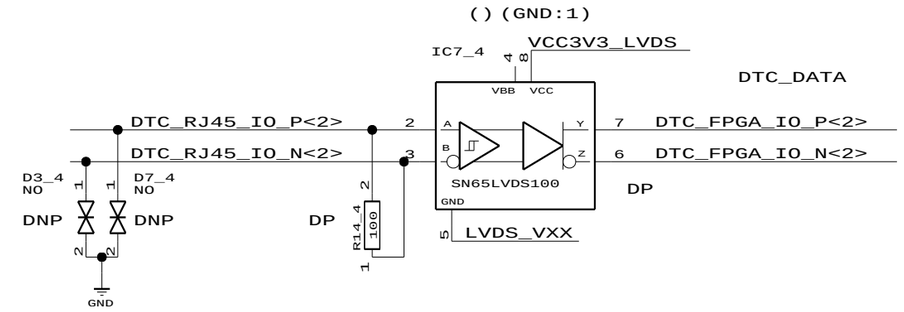


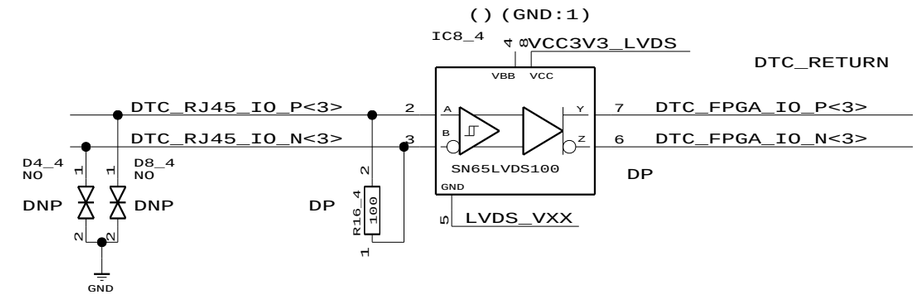


INPUTS

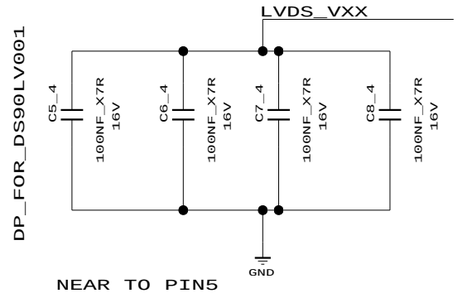


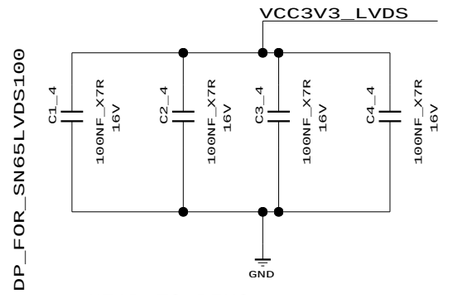






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

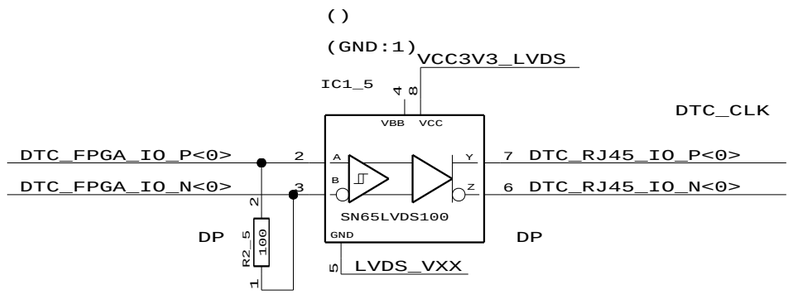
TE/MPE

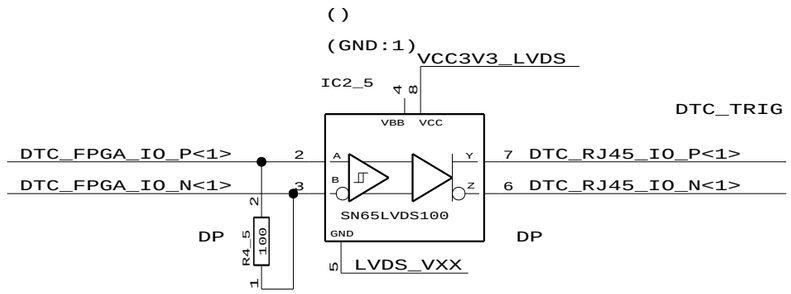
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 35/81

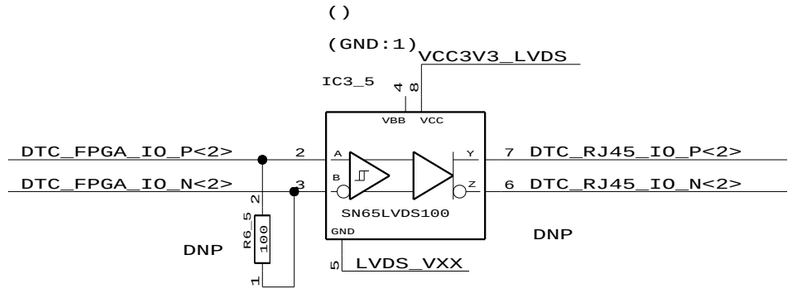
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

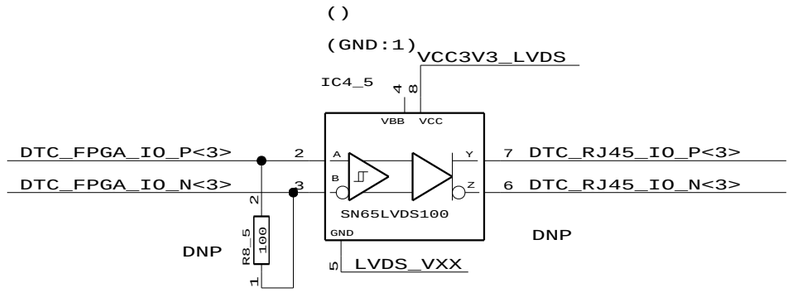
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

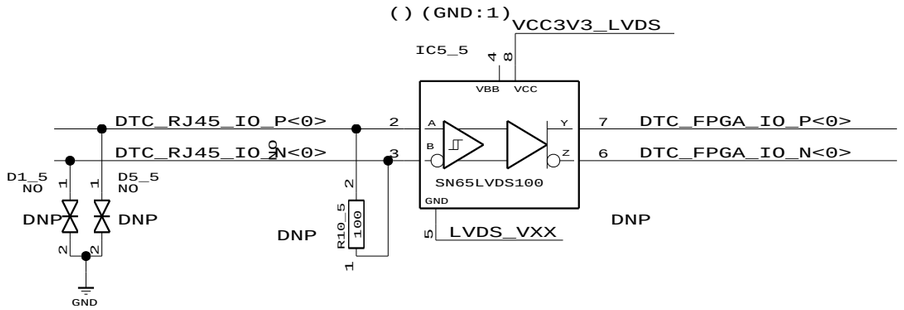


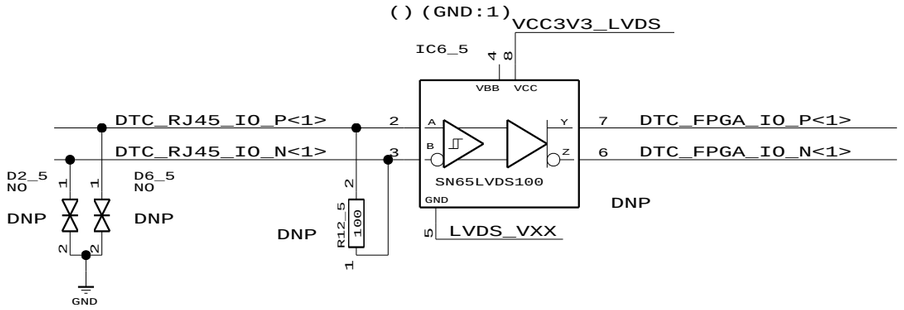


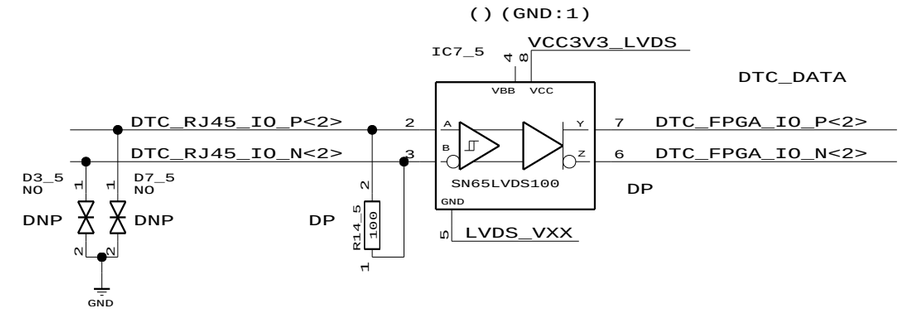


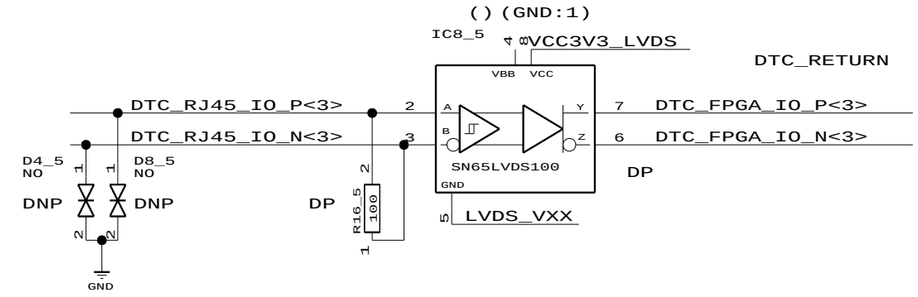


INPUTS

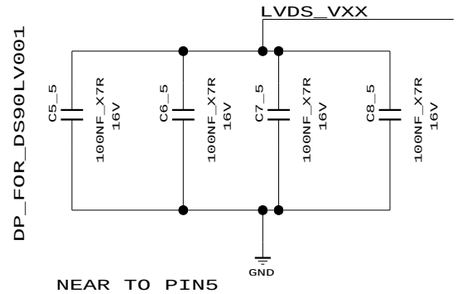


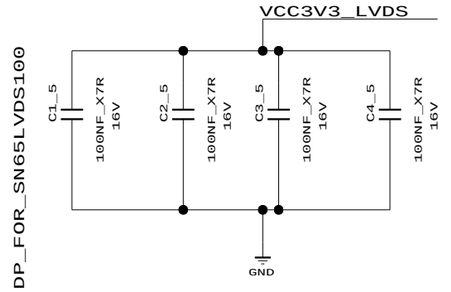






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

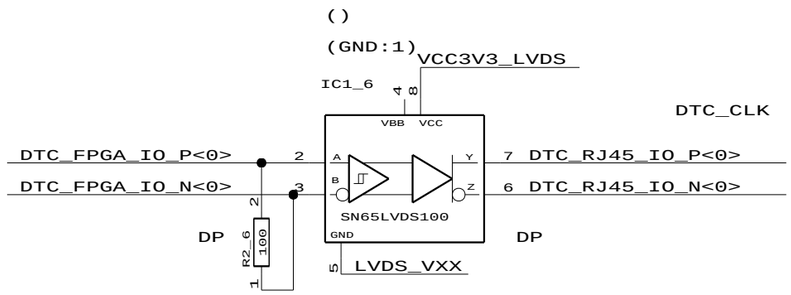
European Organization for Nuclear Research
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TE/MPE

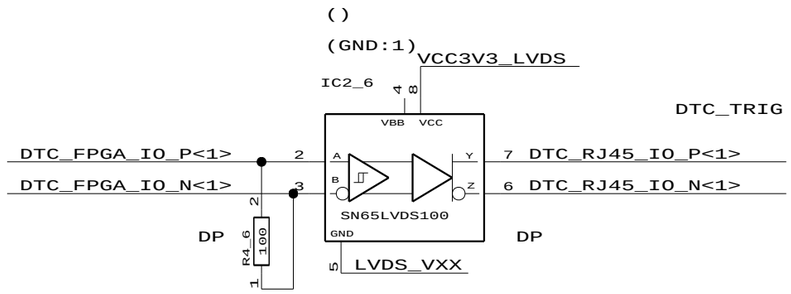
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 36/81

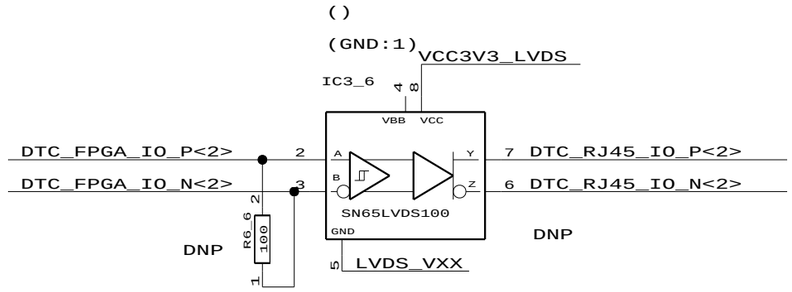
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

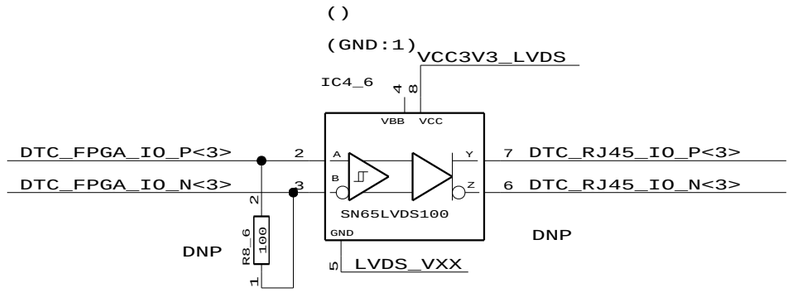
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

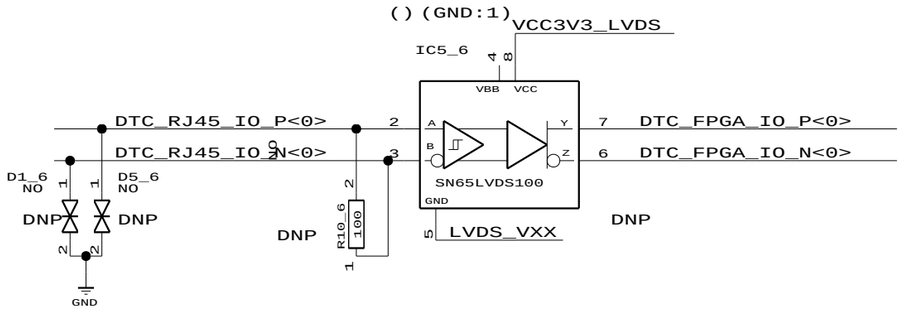


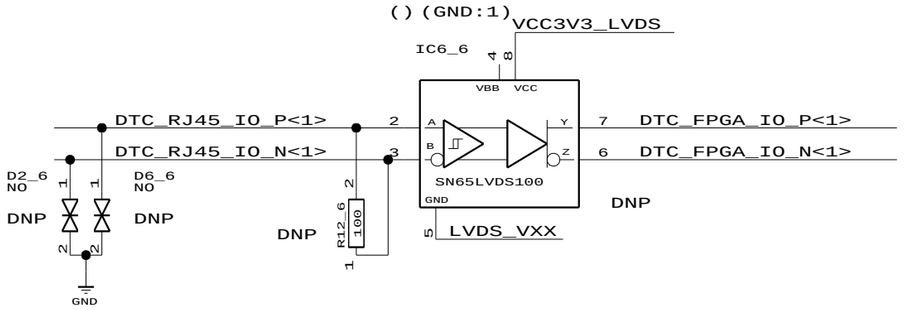


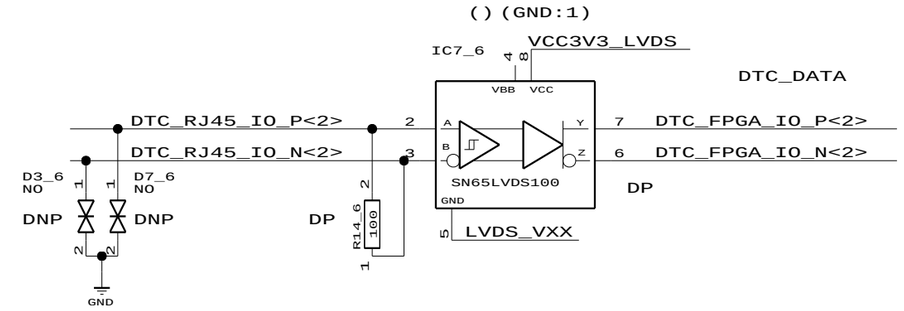


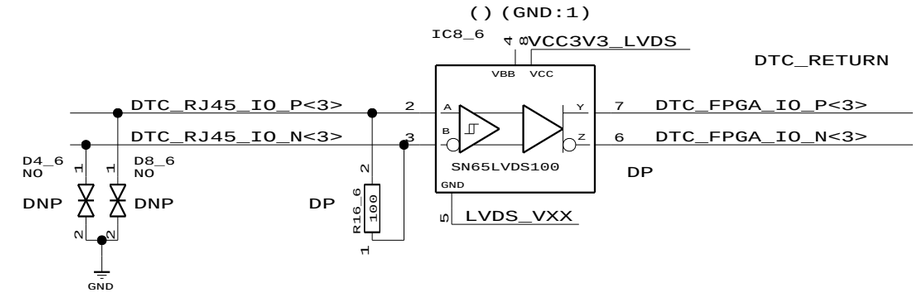


INPUTS

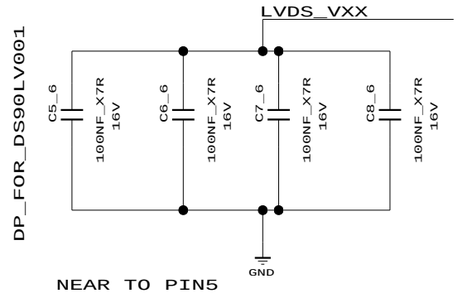


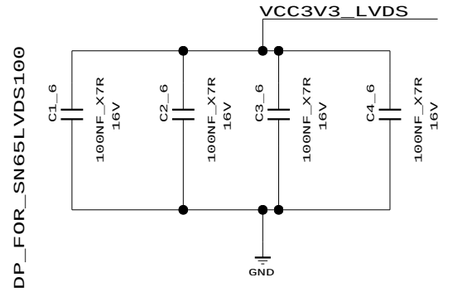






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

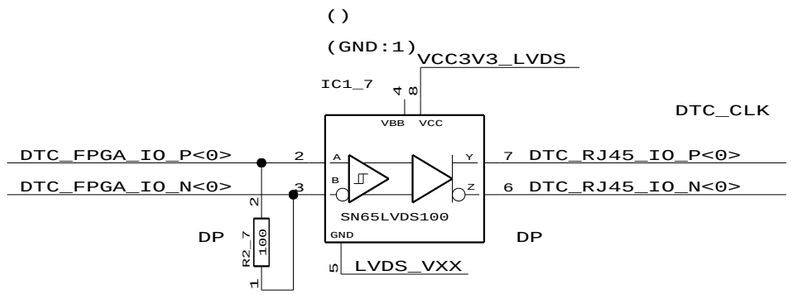
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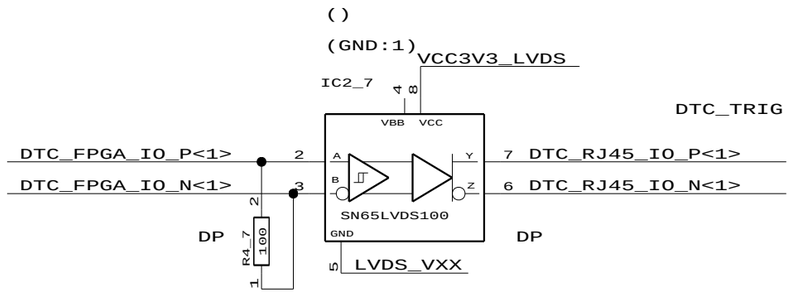
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 37/81

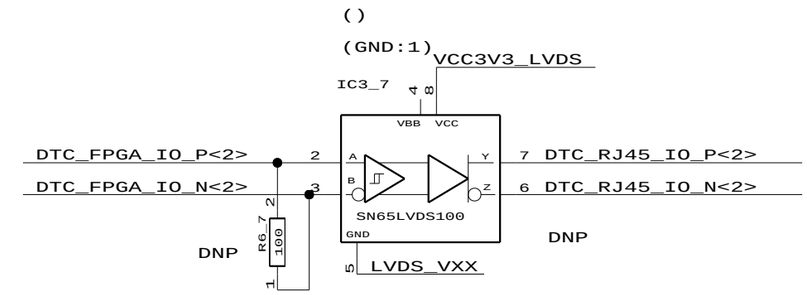
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

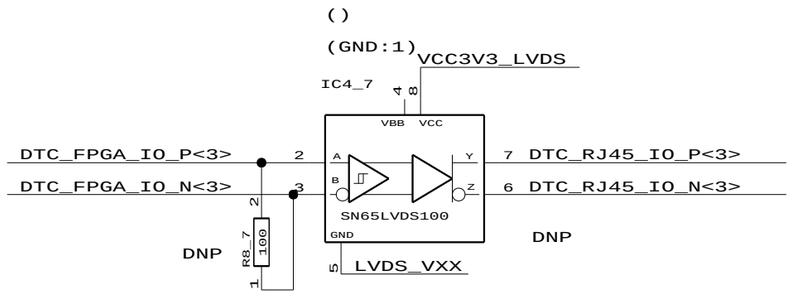
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

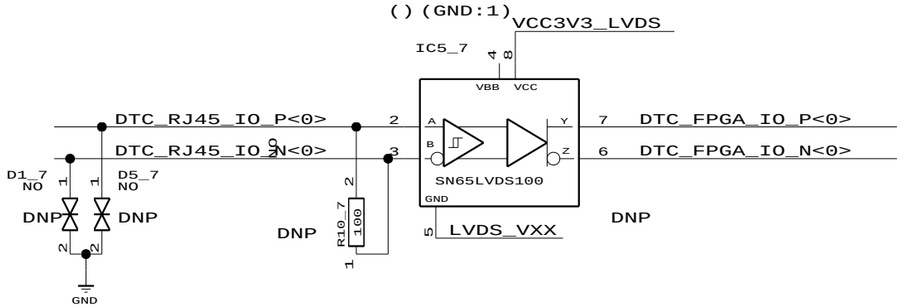


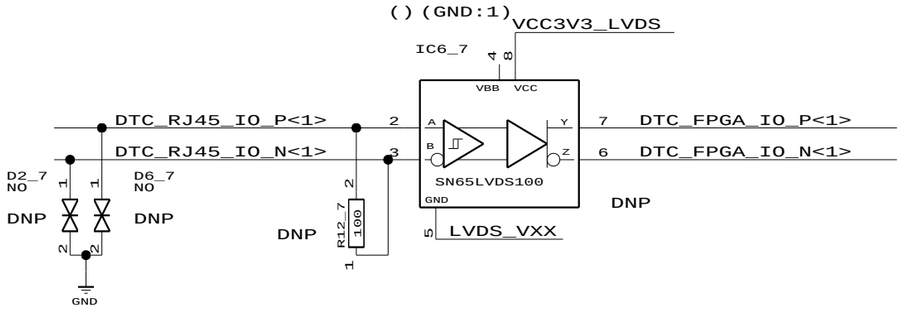


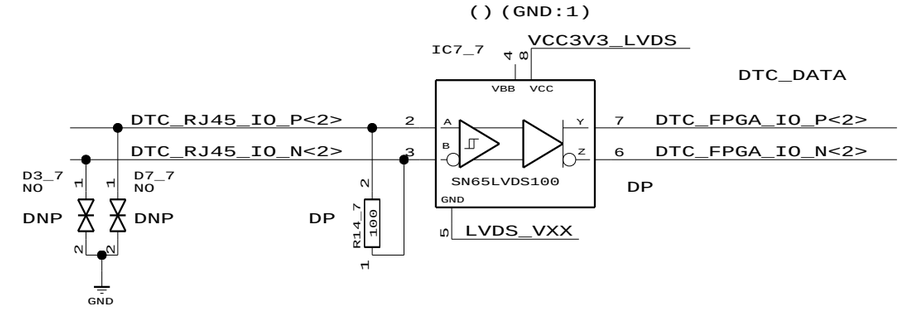


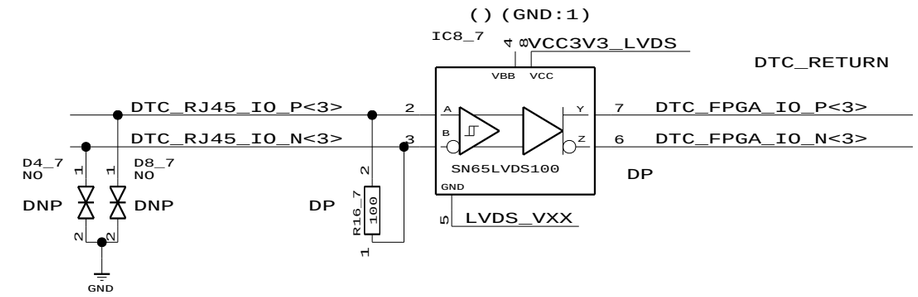


INPUTS

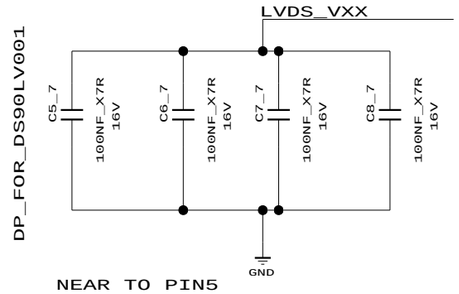




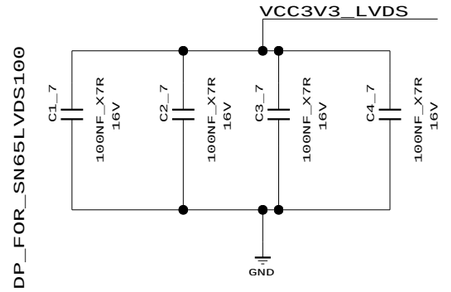




LOCAL DECOUPLING



NEAR TO PIN5



NEAR TO PIN8

IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

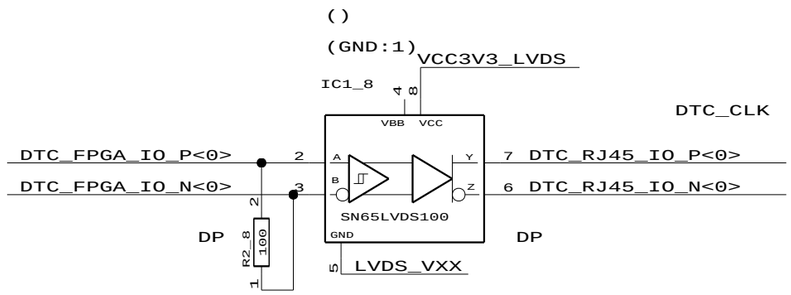
European Organization
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SWITZERLAND
TE/MPE

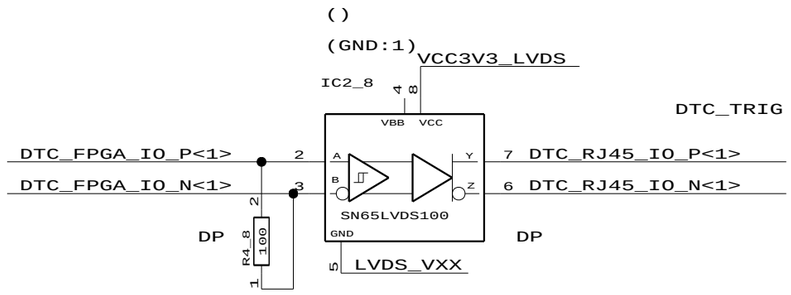
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 38/81

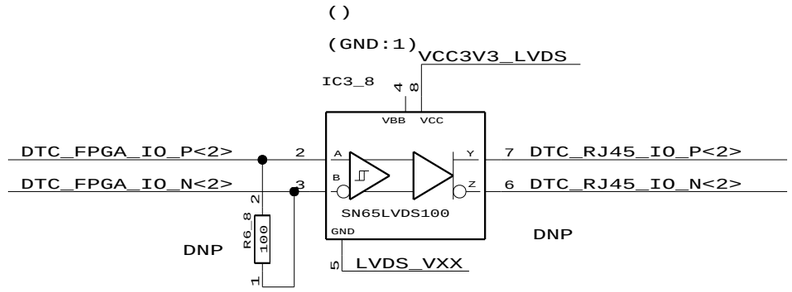
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

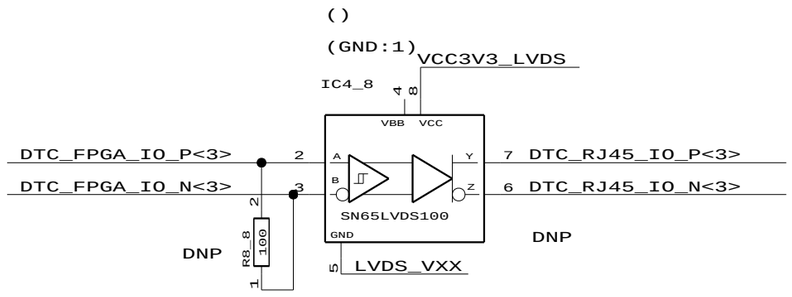
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

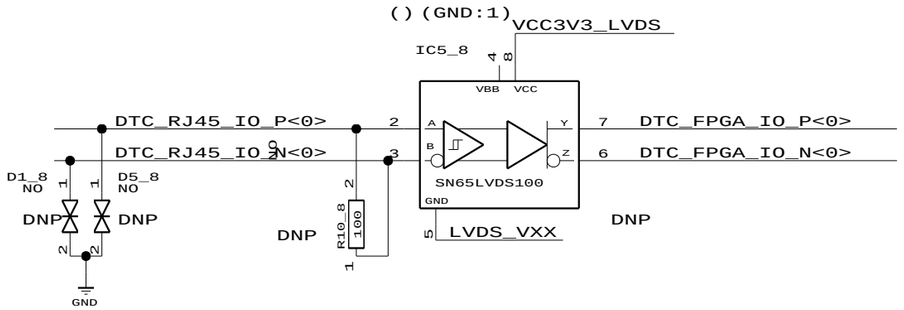


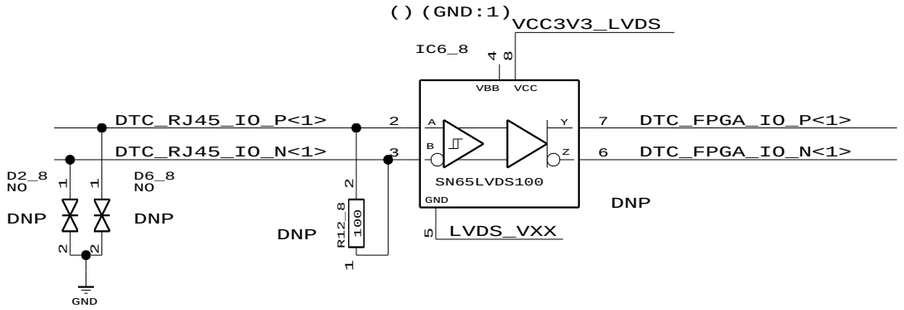


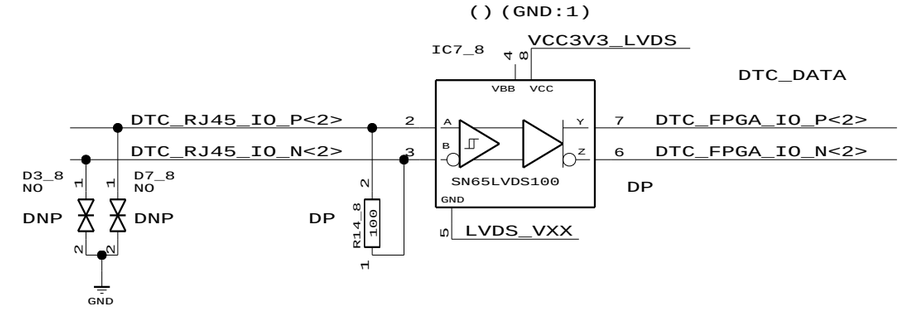


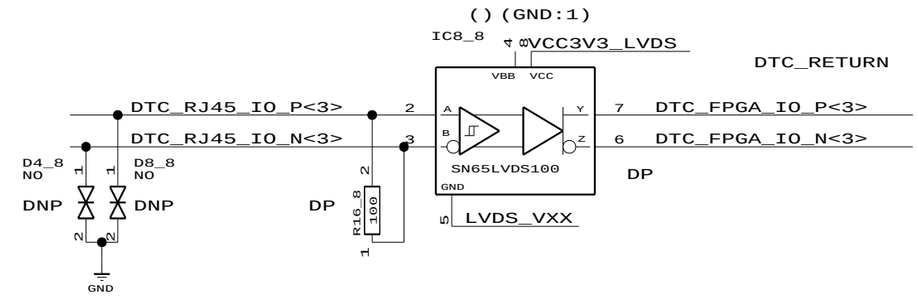


INPUTS

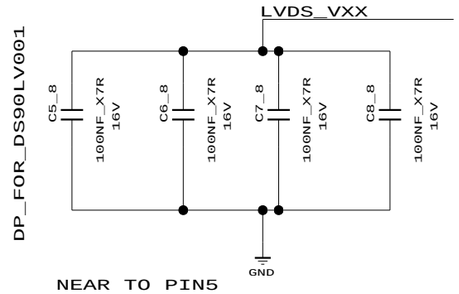


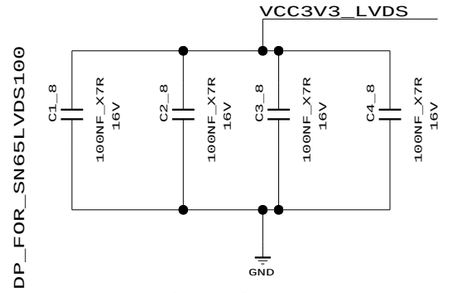






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

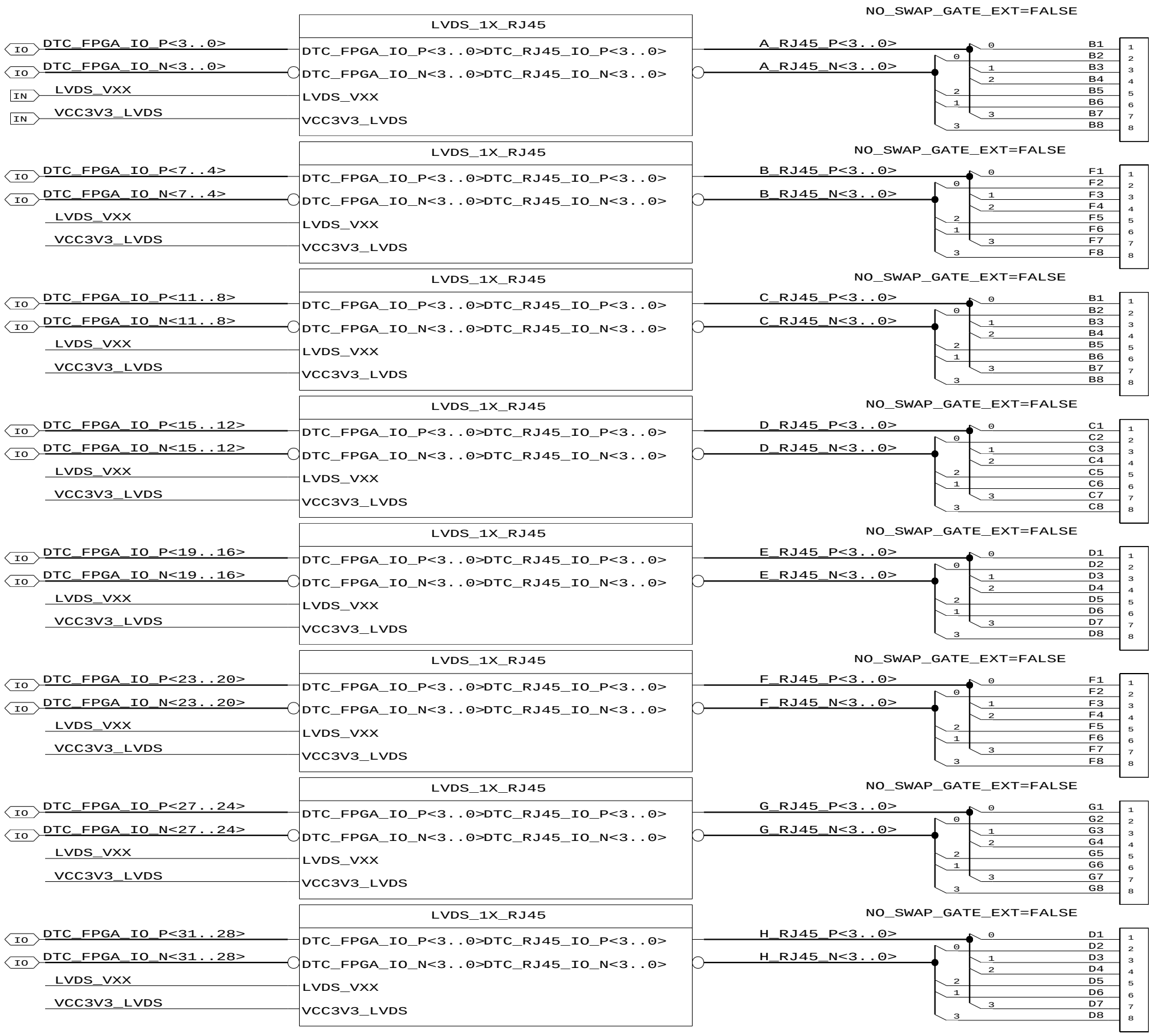
PROJECT:SRU v2.0

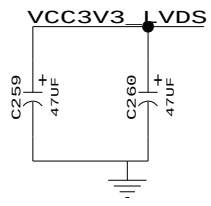
European Organization for Nuclear Research
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SWITZERLAND
TE/MPE

MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 39/81

LAST_MODIFIED=Mon Dec 12 10:53:50 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010





PLACE THIS DECOUPLING CAPACITORS
AROUND THE AROUND THE AREA
OF THIS 2*4 RJ45

Project file:sru_rev2.cpm

SYSTEM:

PROJECT:SRU v2.0

MODULE:lvds_8x_rj45

Sheet: Module: 1/1 Project: 40/81

LAST_MODIFIED=Fri Dec 09 11:01:52 2011

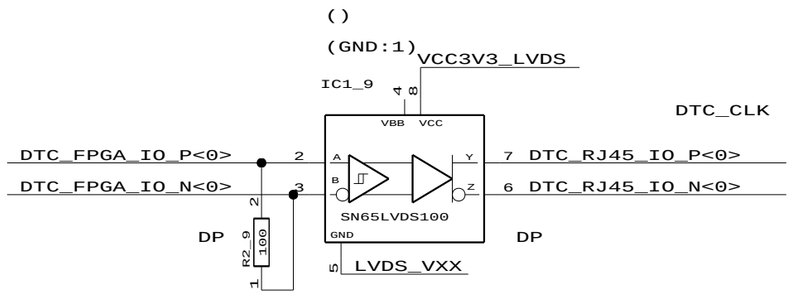
Design by: FZhang/SMartoiu

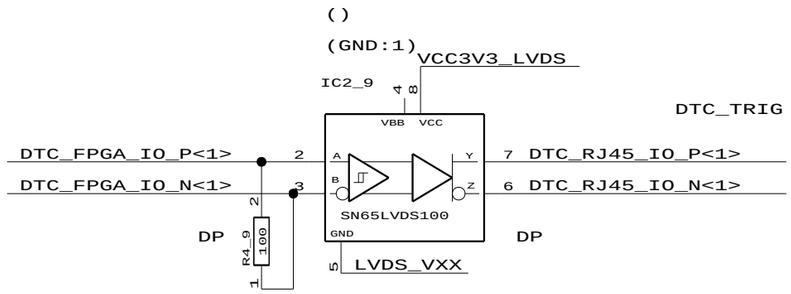
PCB by: EXT

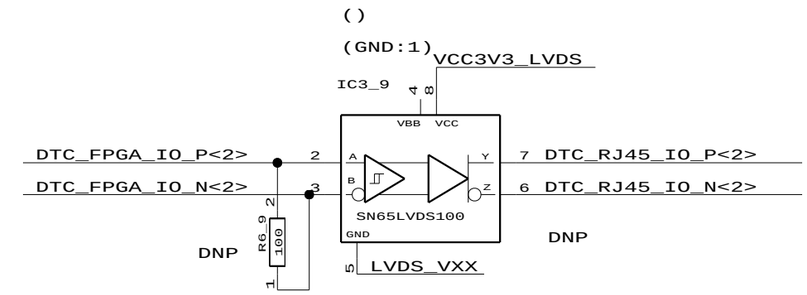
DATE: 29/07/2010

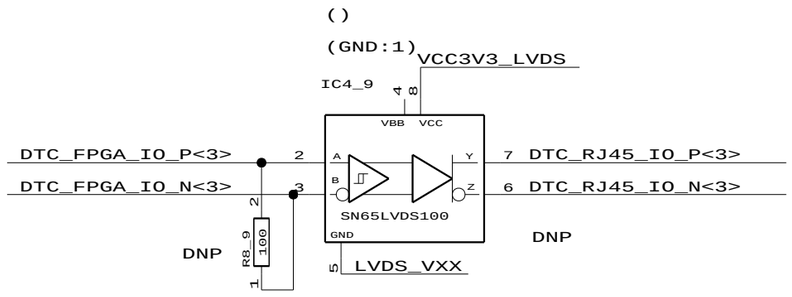
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TS/DEM

OUTPUTS

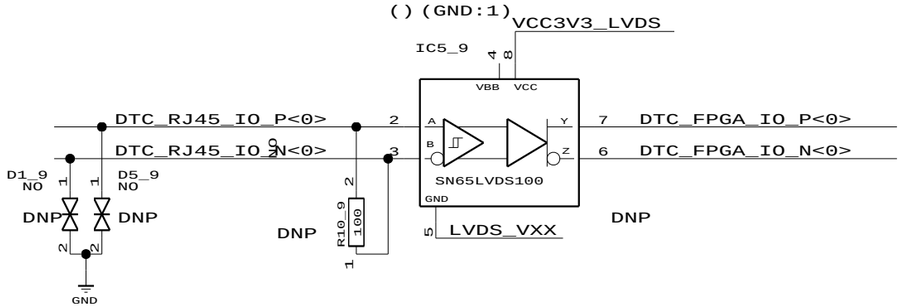


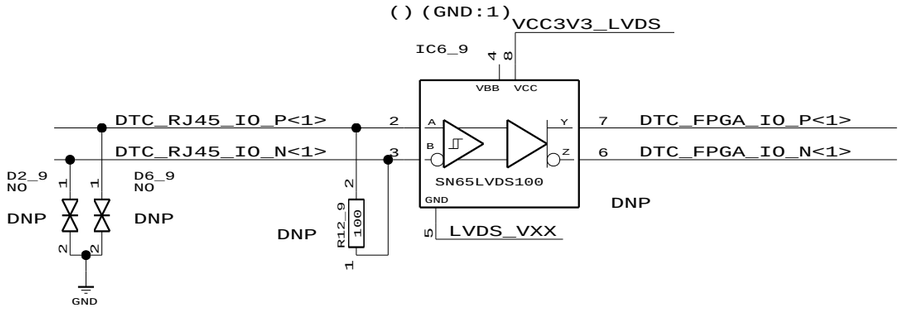


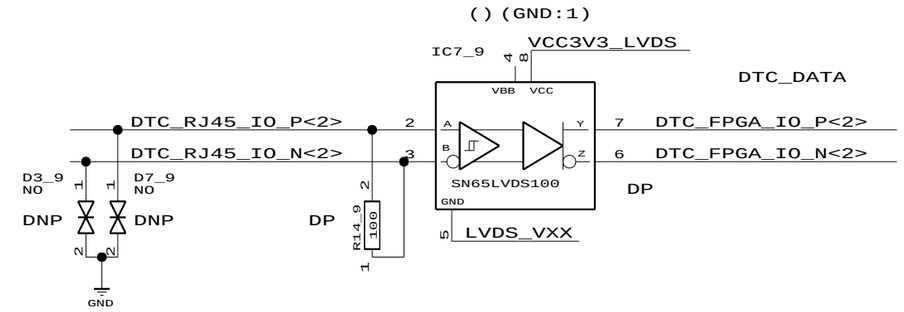


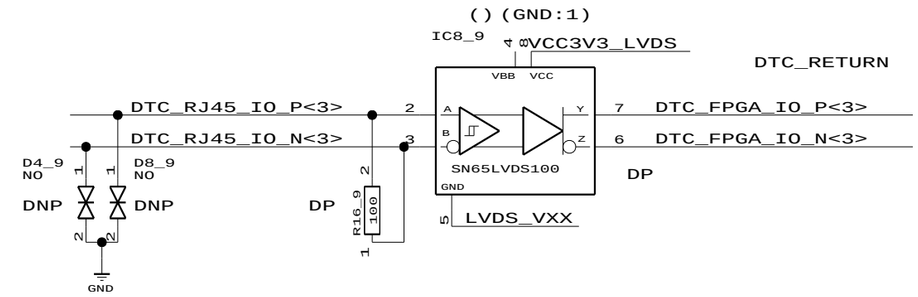


INPUTS

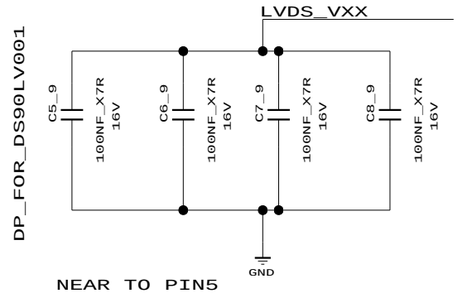


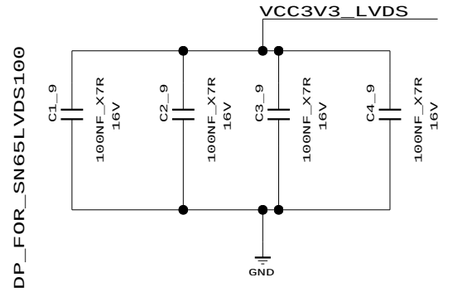






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

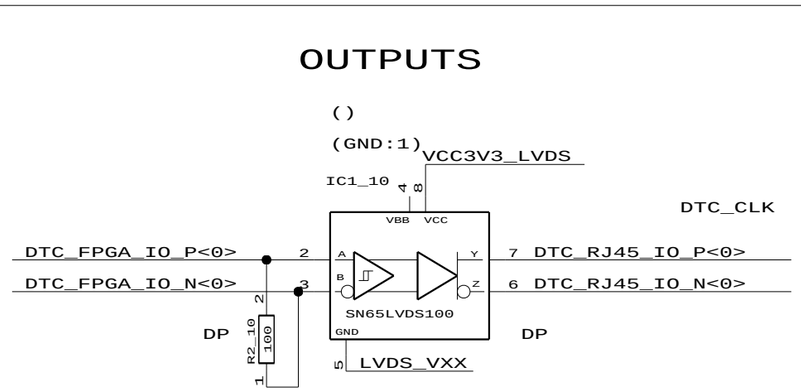
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

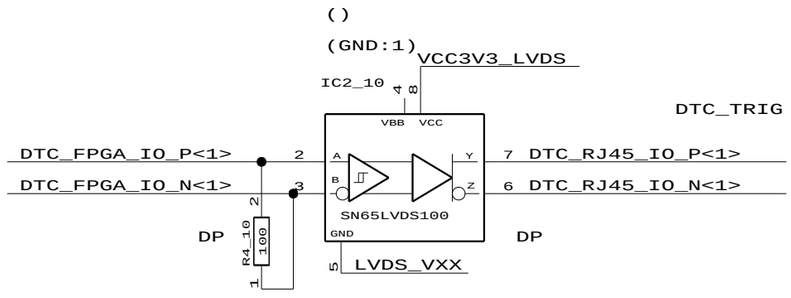
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 41/81

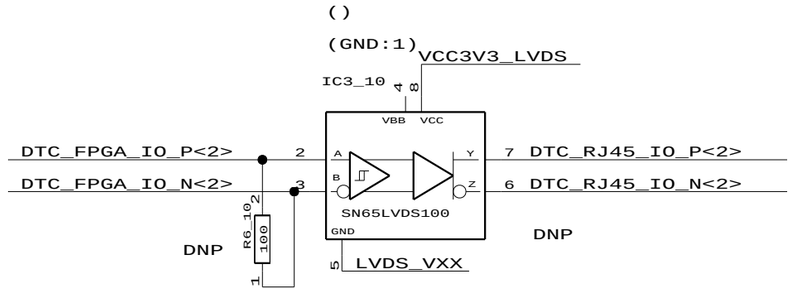
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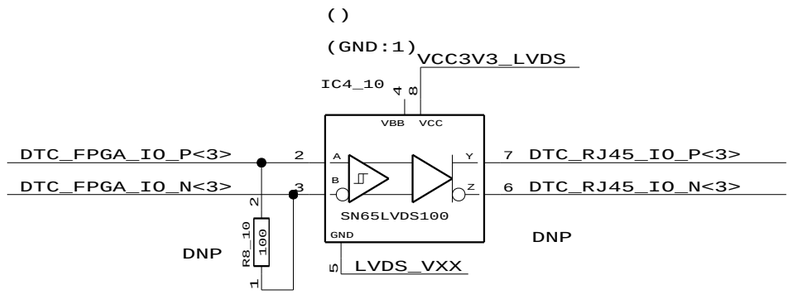
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

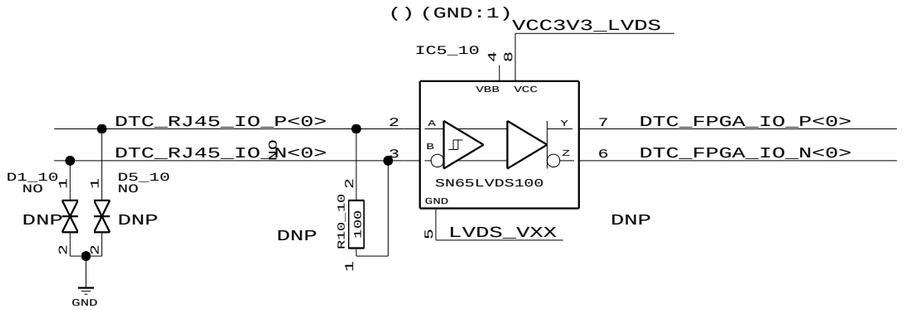


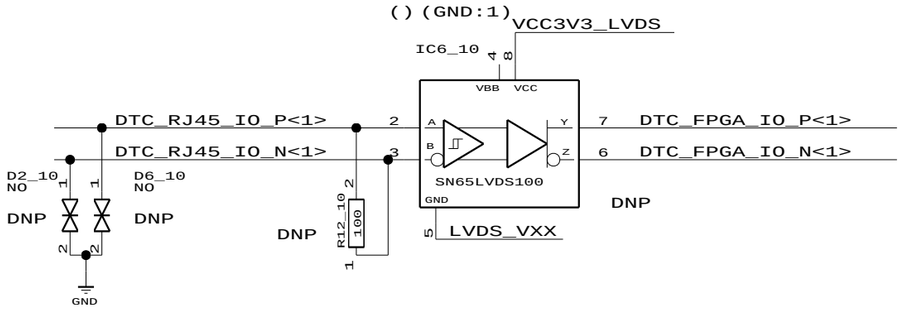


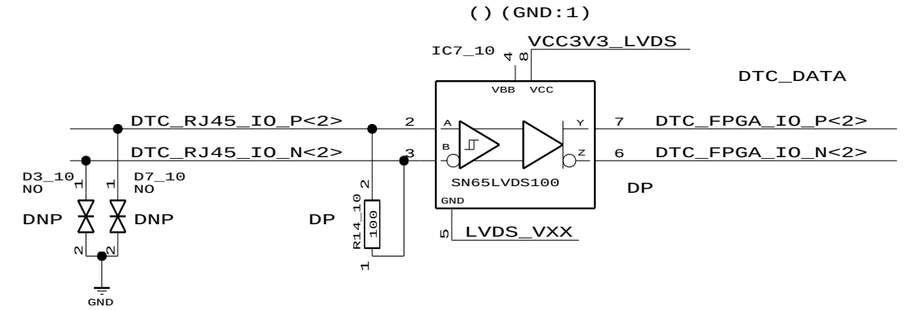


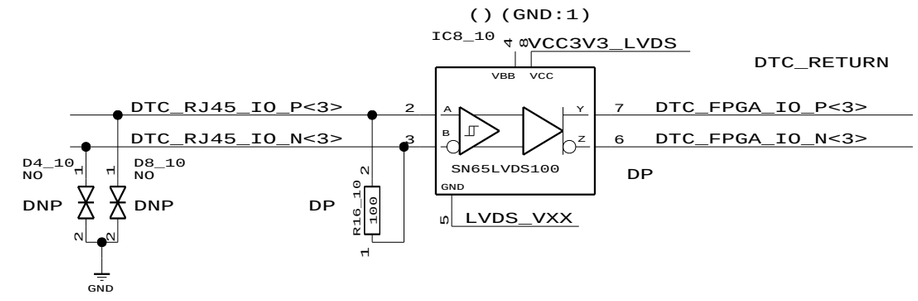


INPUTS

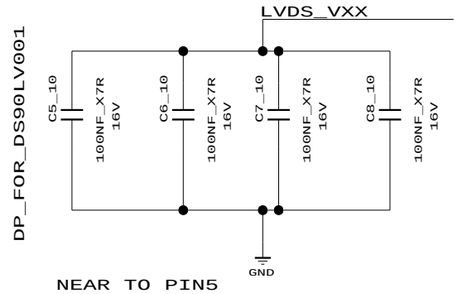


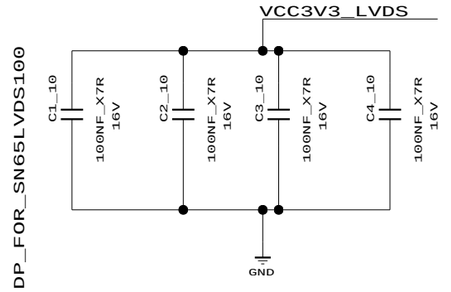






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA
- IO DTC_FPGA_IO_P<3..0>
- IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45
- IO DTC_RJ45_IO_P<3..0>
- IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

TE/MPE

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

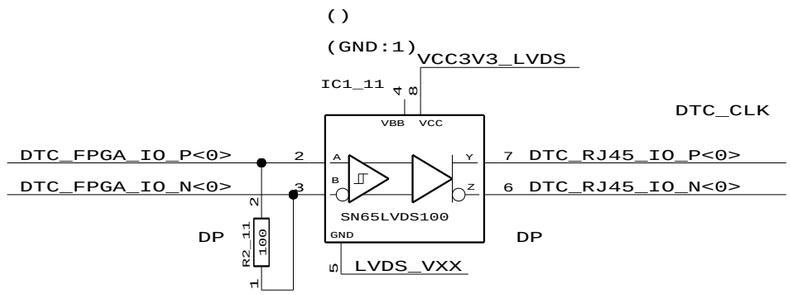
PROJECT:SRU v2.0

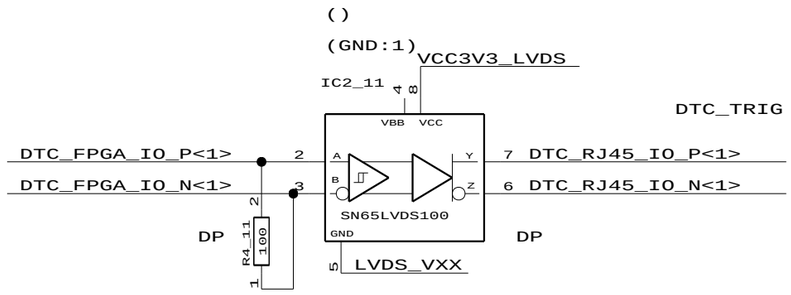
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 42/81

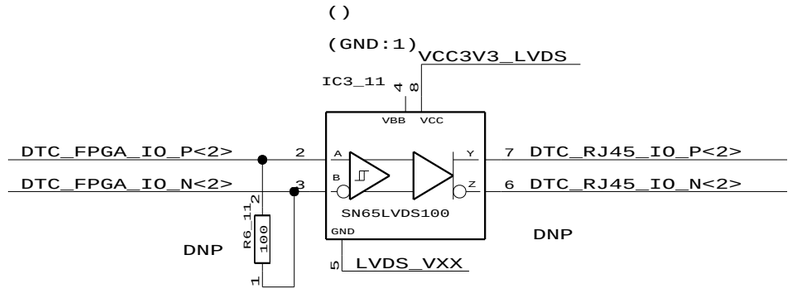
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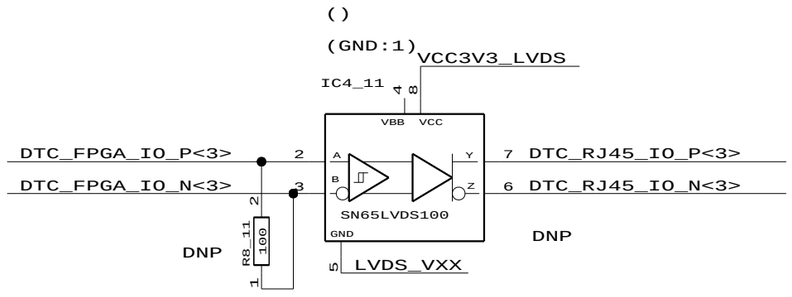
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

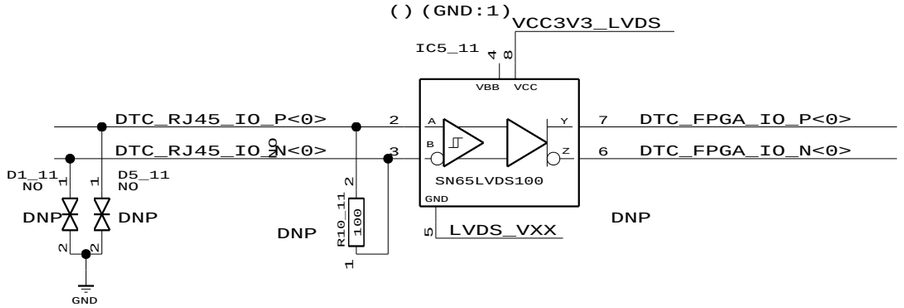


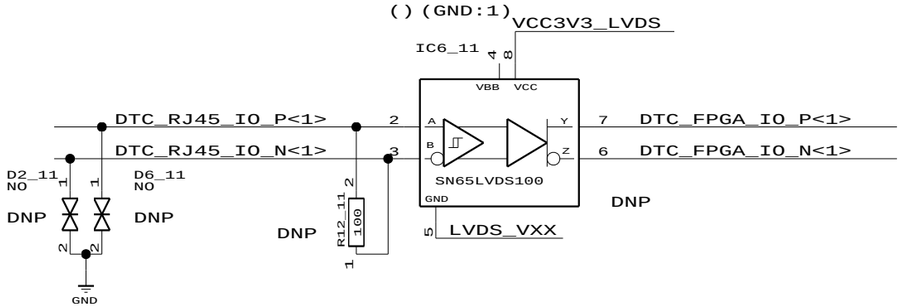


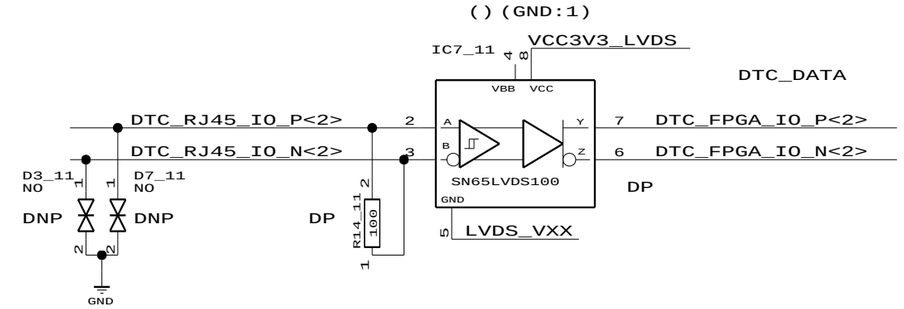


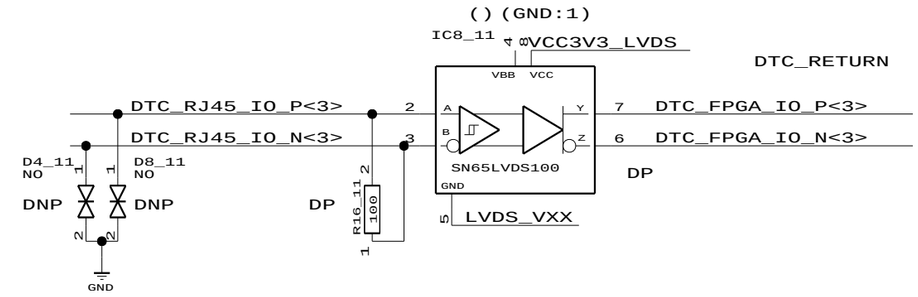


INPUTS

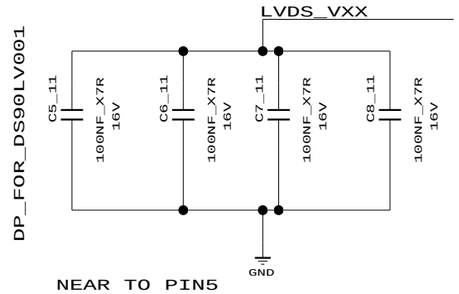


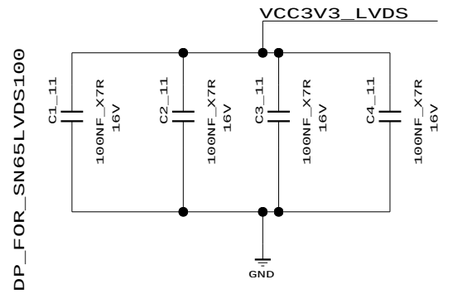






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

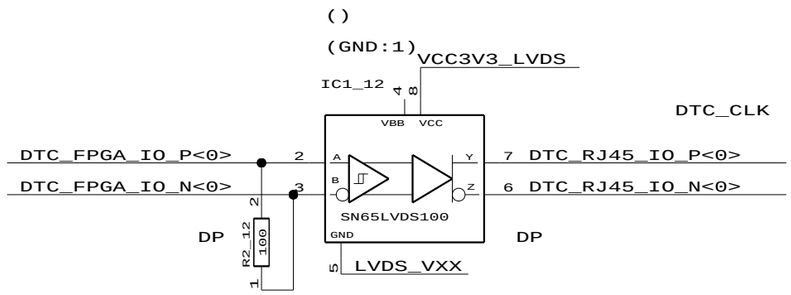
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

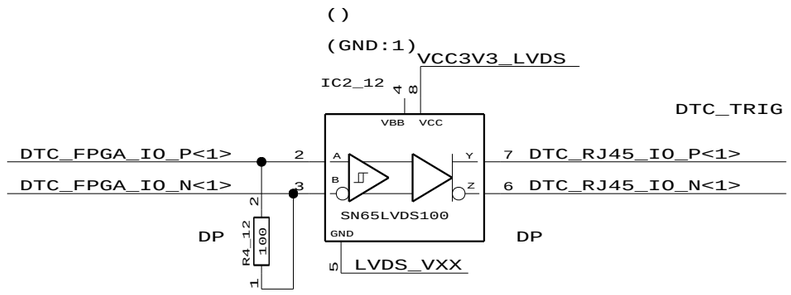
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 43/81

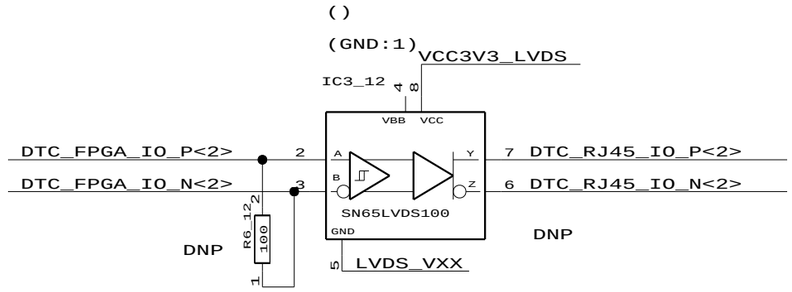
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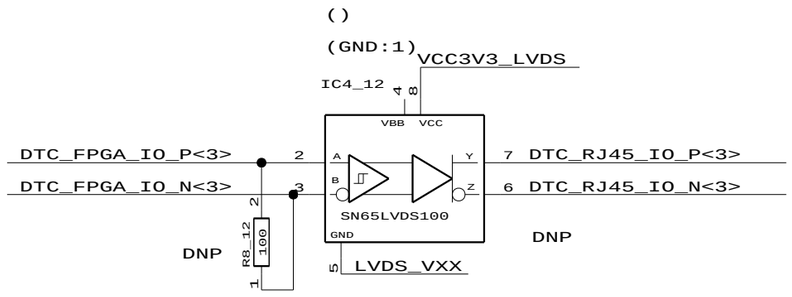
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

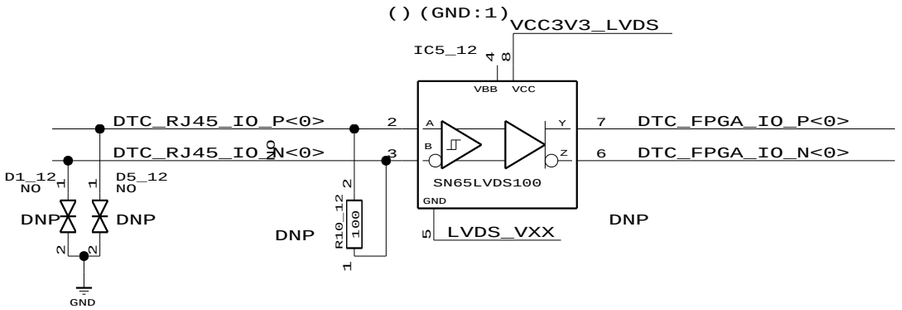


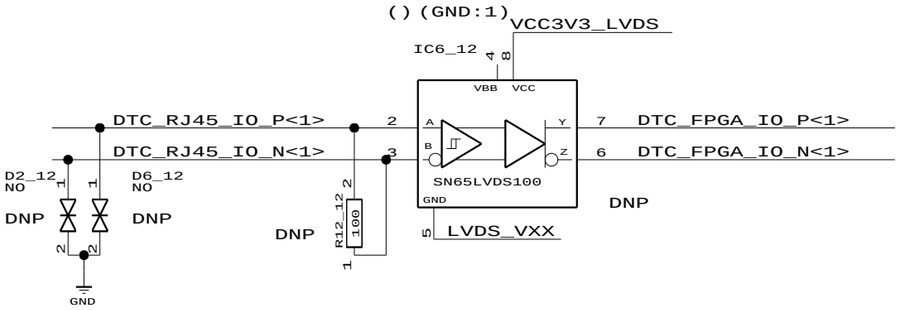


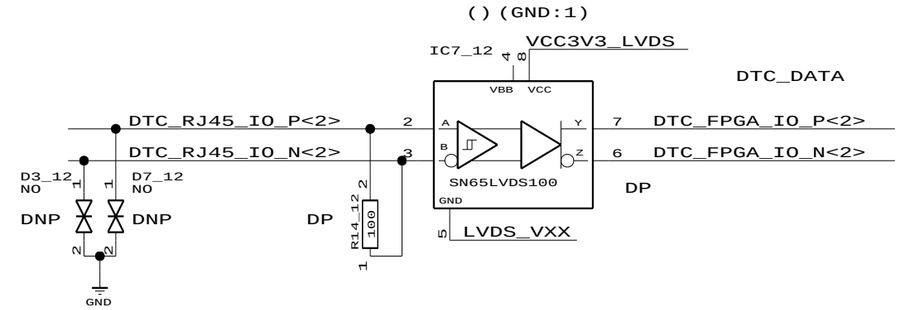


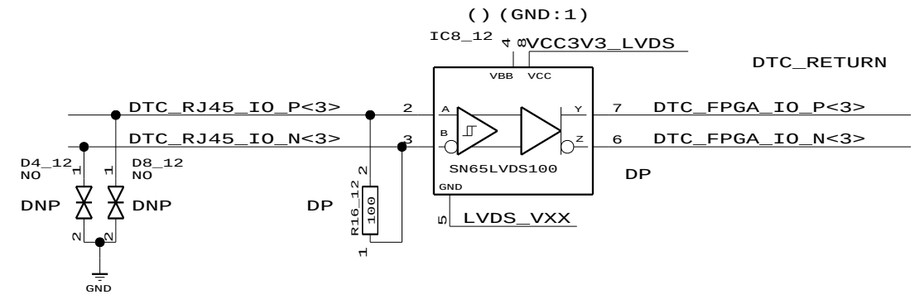


INPUTS

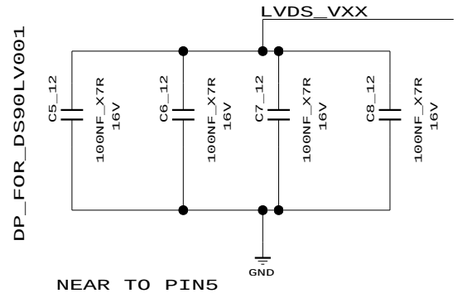


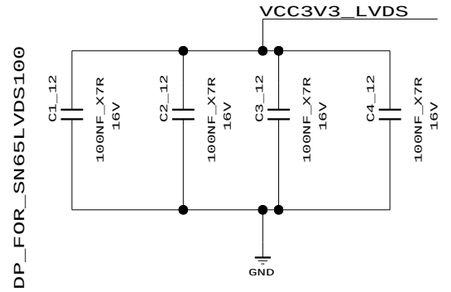






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA
- IO DTC_FPGA_IO_P<3..0>
- IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45
- IO DTC_RJ45_IO_P<3..0>
- IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

CERN TE/MPE
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND

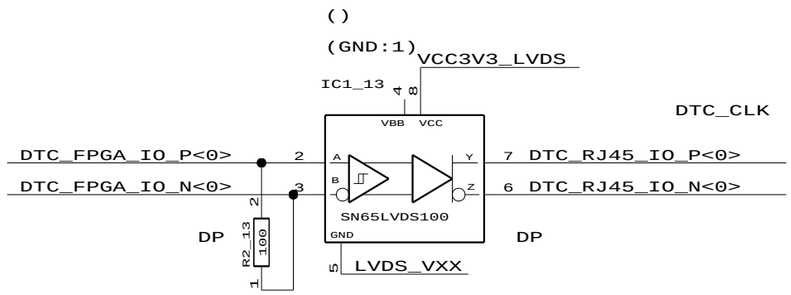
PROJECT:SRU v2.0

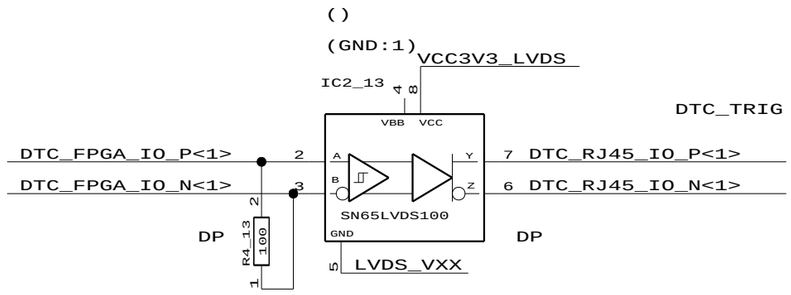
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 44/81

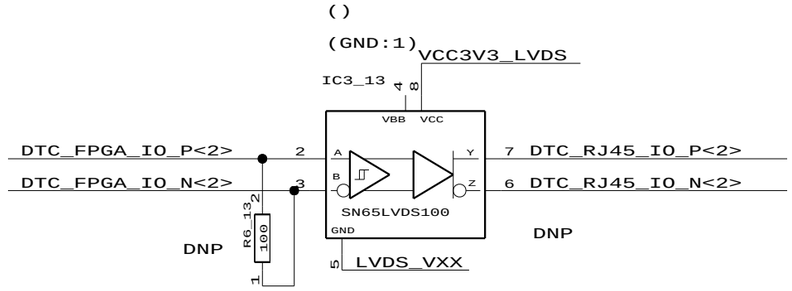
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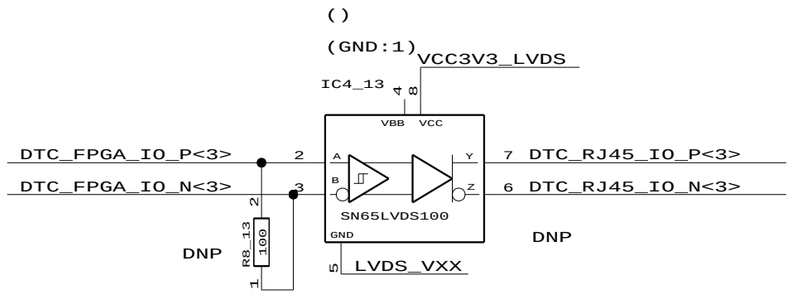
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

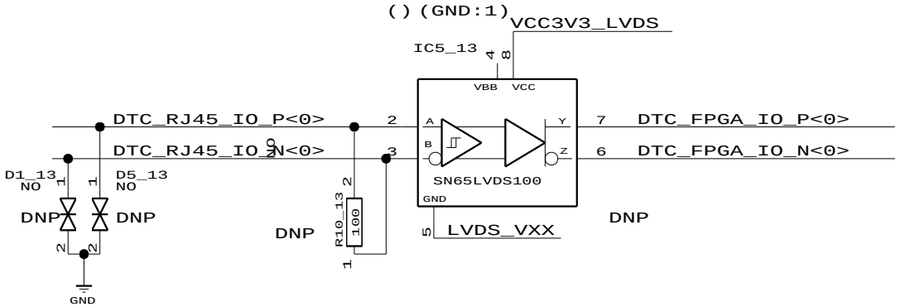


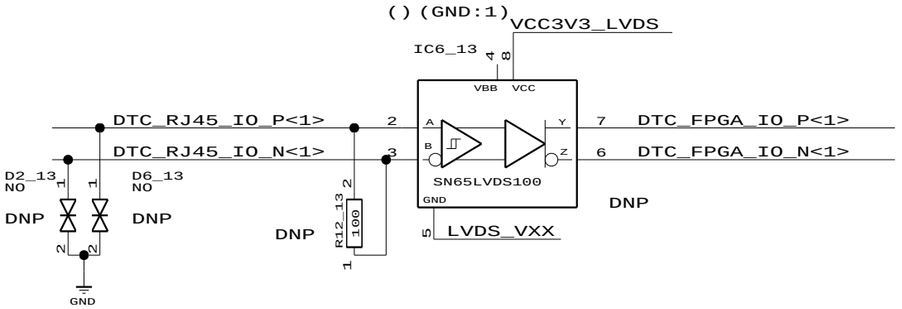


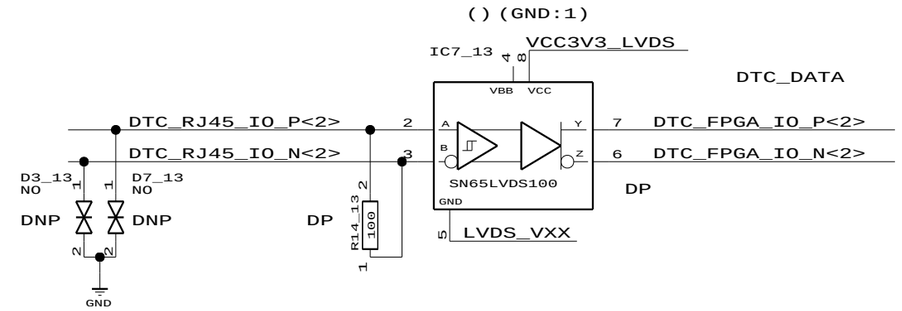


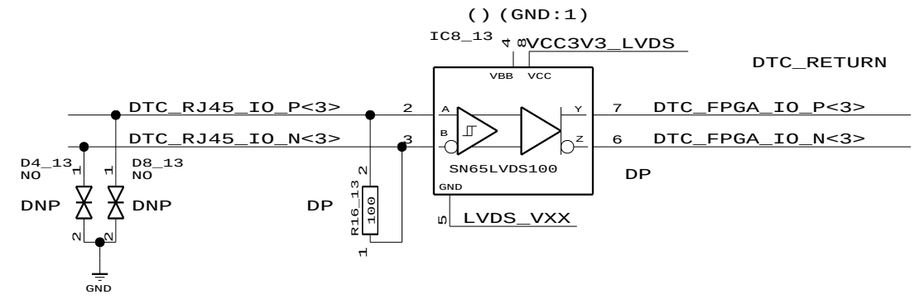


INPUTS

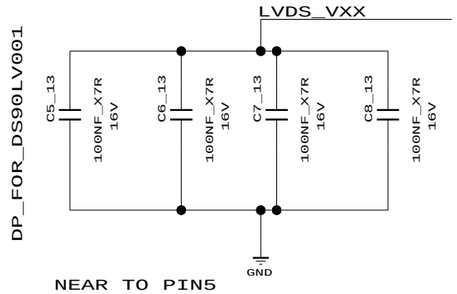


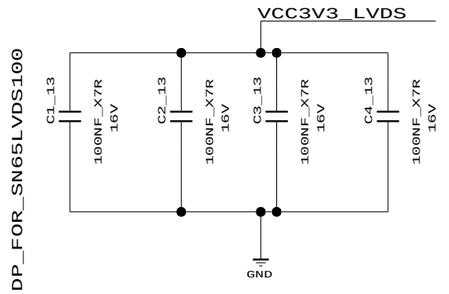






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA
- IO DTC_FPGA_IO_P<3..0>
- IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45
- IO DTC_RJ45_IO_P<3..0>
- IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

TE/MPE CERN European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND

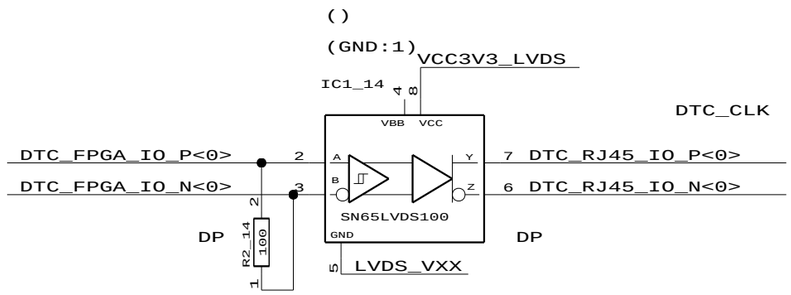
PROJECT:SRU v2.0

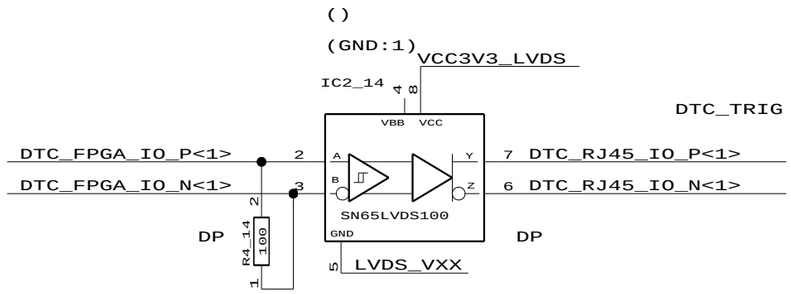
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 45/81

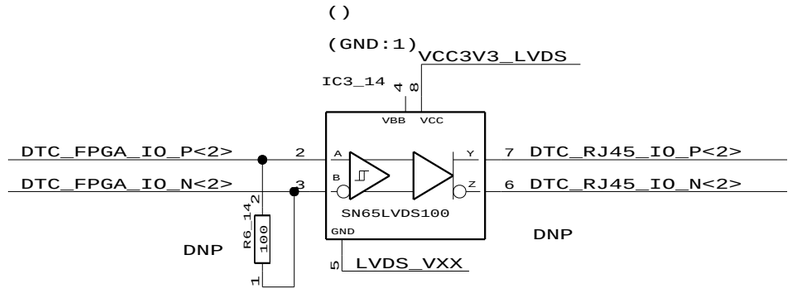
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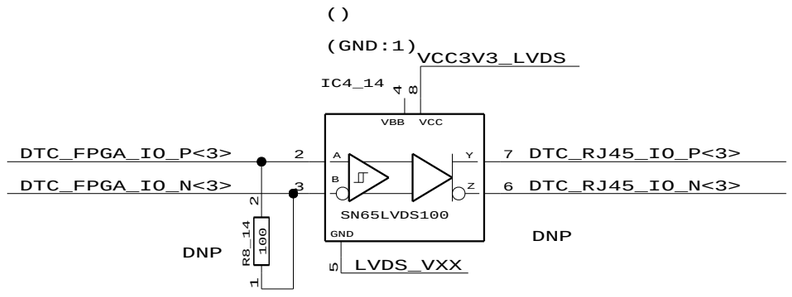
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

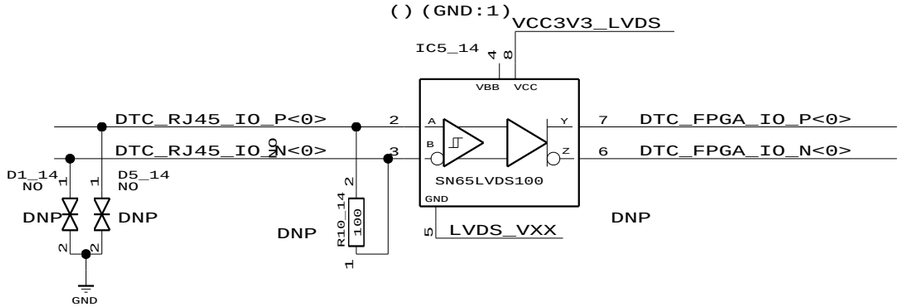


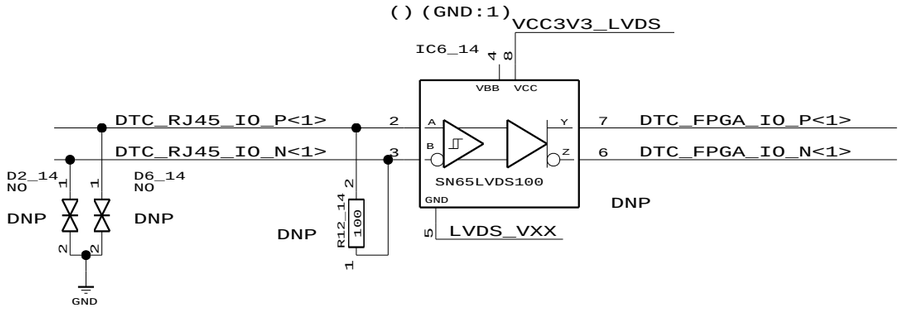


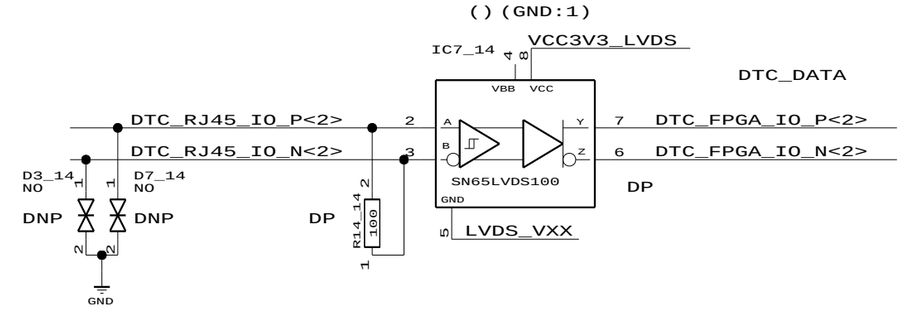


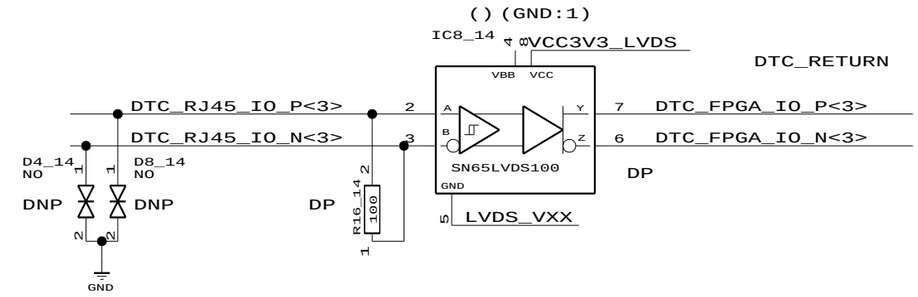


INPUTS

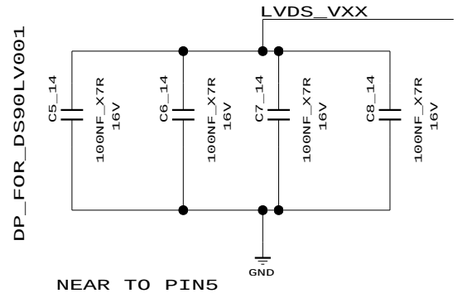


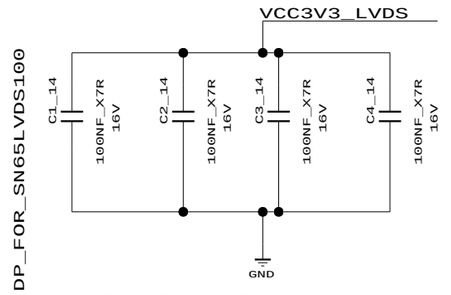






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA
- IO DTC_FPGA_IO_P<3..0>
- IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45
- IO DTC_RJ45_IO_P<3..0>
- IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

TE/MPE

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

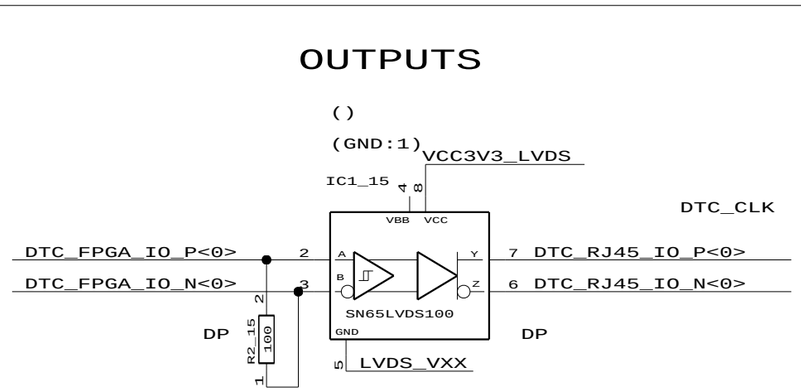
PROJECT:SRU v2.0

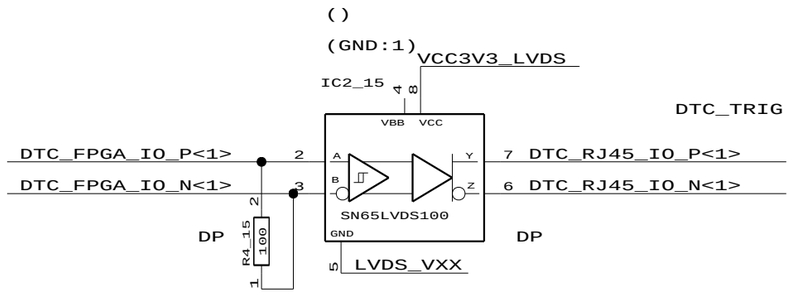
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 46/81

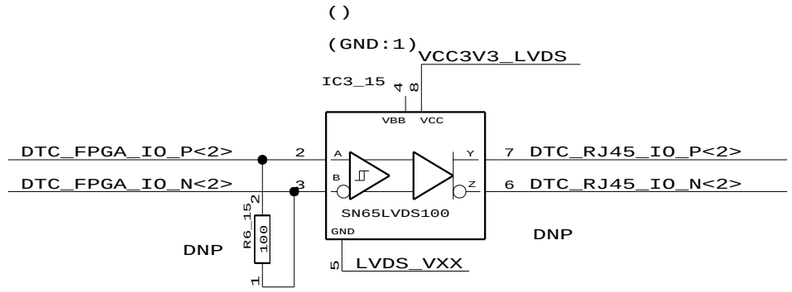
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

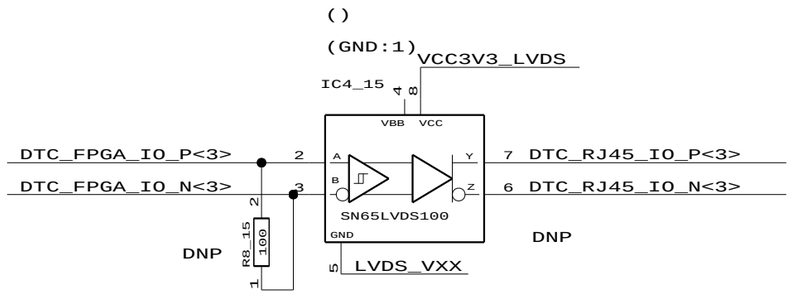
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

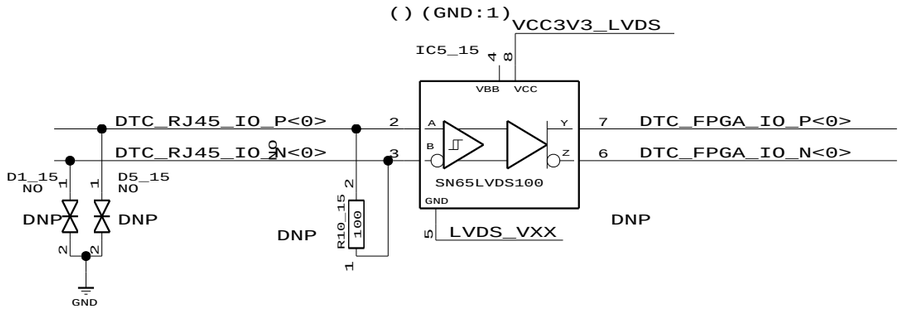


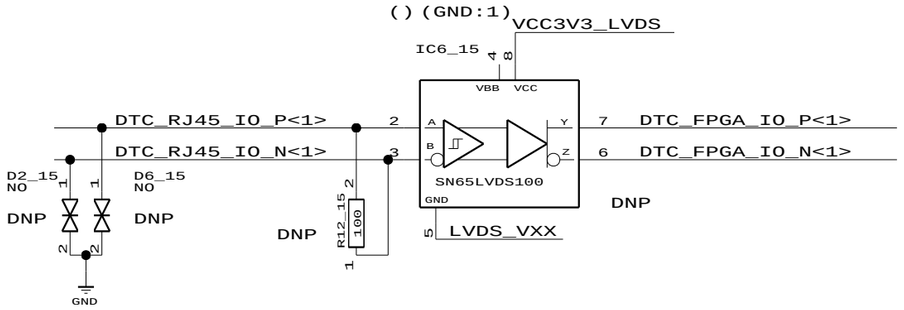


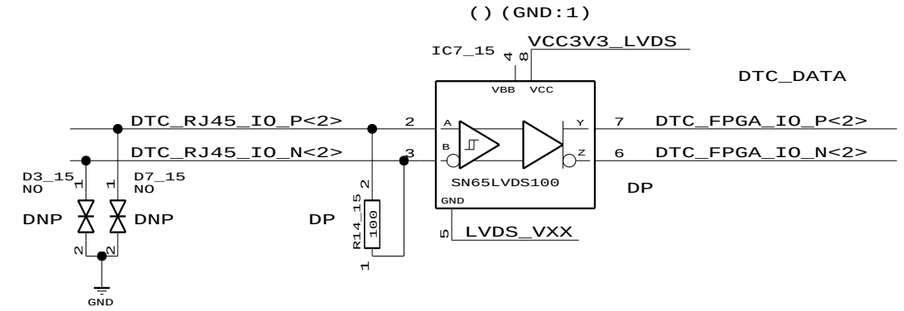


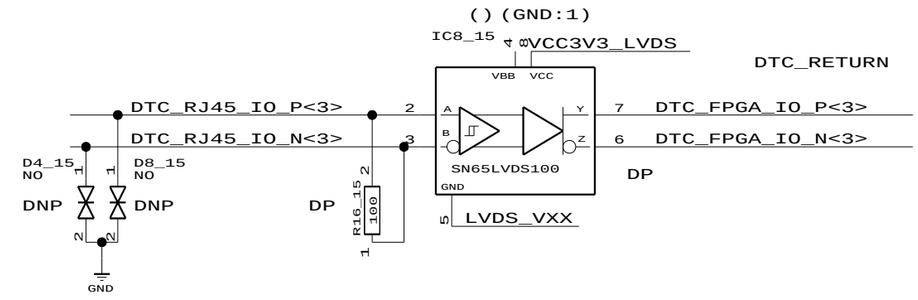


INPUTS

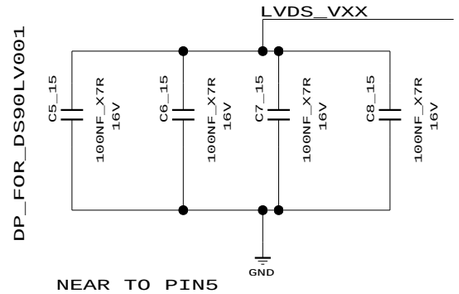


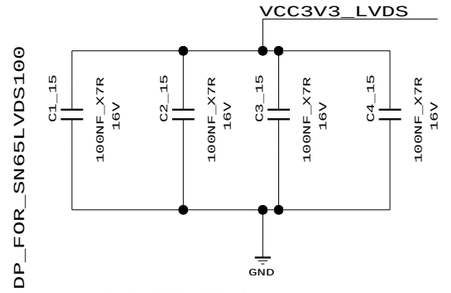






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

CERN TE/MPE European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND

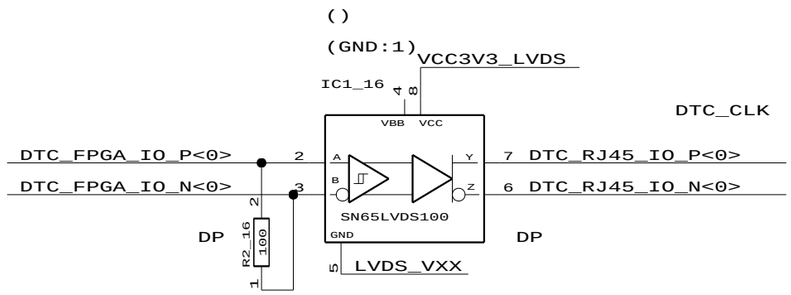
PROJECT:SRU v2.0

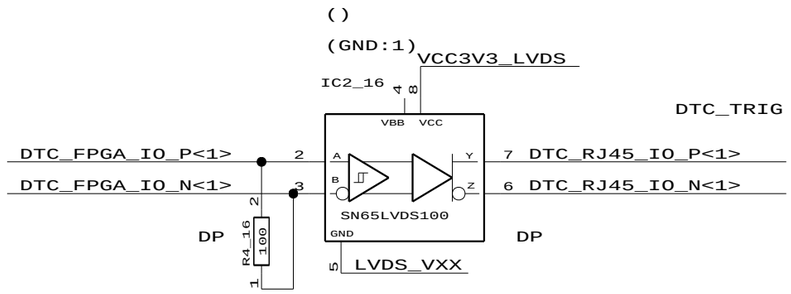
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 47/81

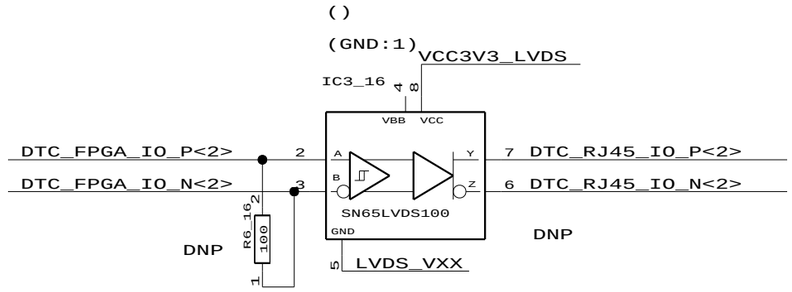
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

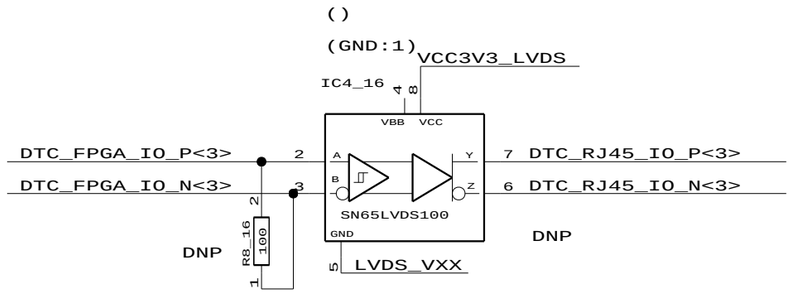
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

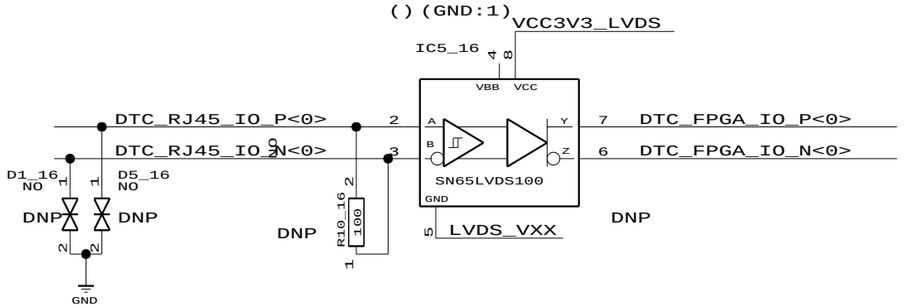


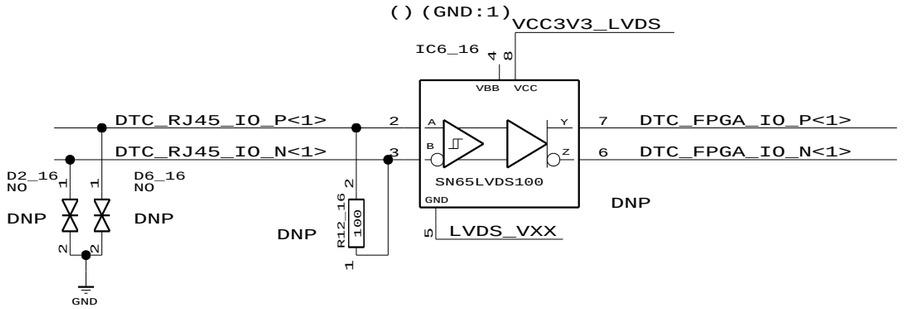


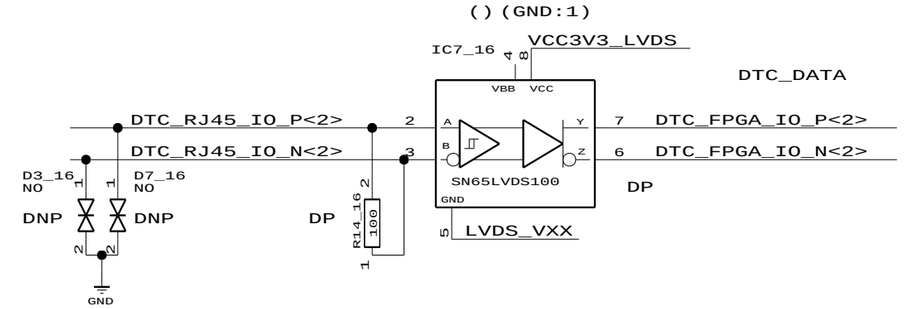


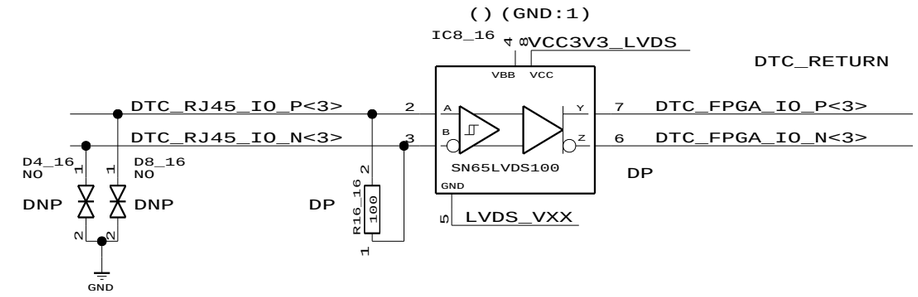


INPUTS

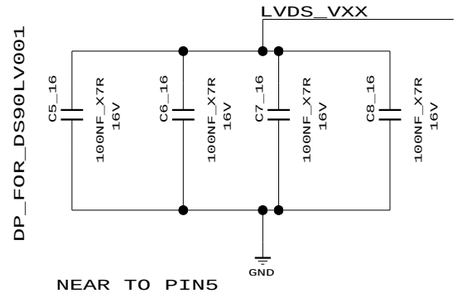


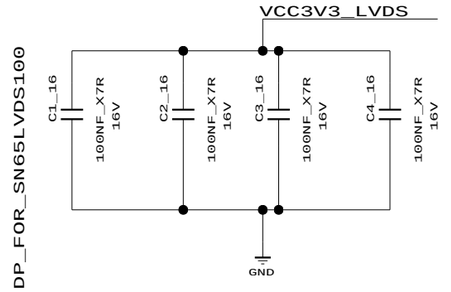






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA
- IO DTC_FPGA_IO_P<3..0>
- IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45
- IO DTC_RJ45_IO_P<3..0>
- IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

TE/MPE

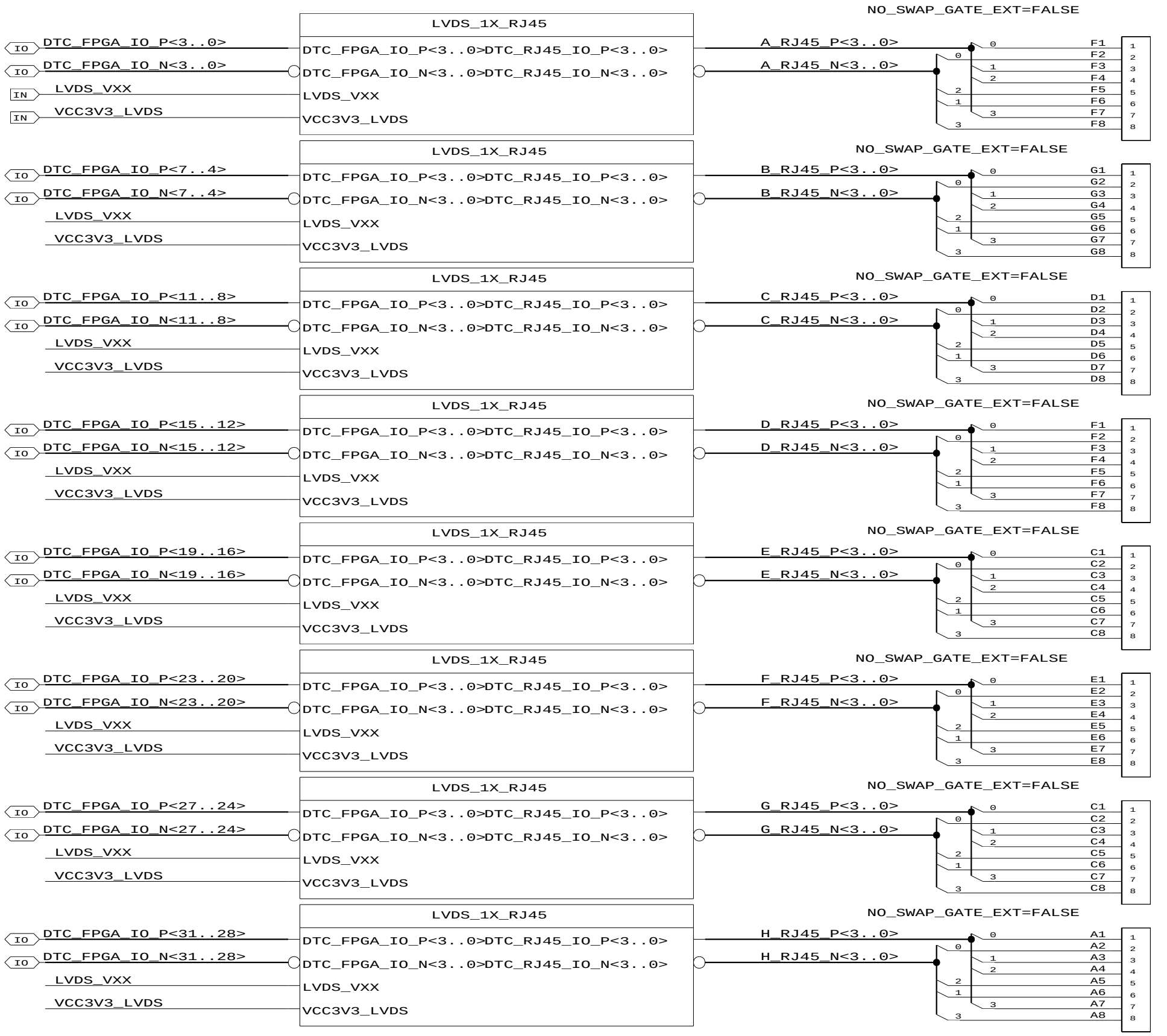
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

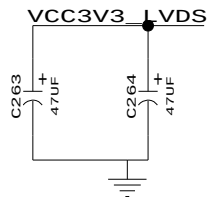
PROJECT:SRU v2.0

MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 48/81

LAST_MODIFIED=Mon Dec 12 10:53:50 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010





PLACE THIS DECOUPLING CAPACITORS
AROUND THE AROUND THE AREA
OF THIS 2*4 RJ45

Project file:sru_rev2.cpm

SYSTEM:

PROJECT:SRU v2.0

MODULE:lvds_8x_rj45

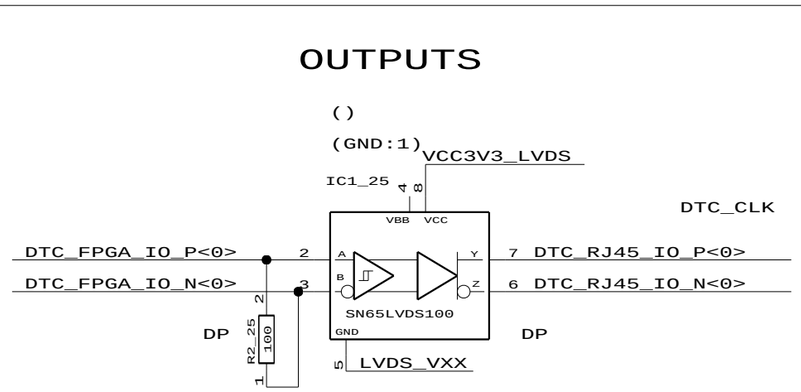
Sheet: Module: 1/1 Project: 49/81

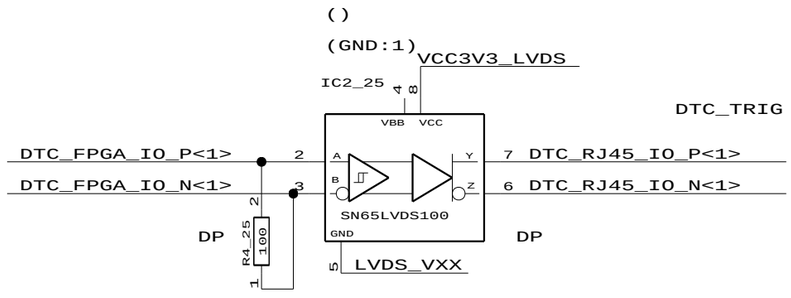
LAST_MODIFIED=Fri Dec 09 11:01:52 2011

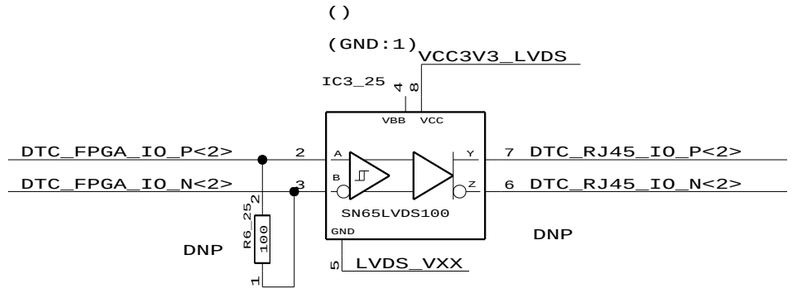
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

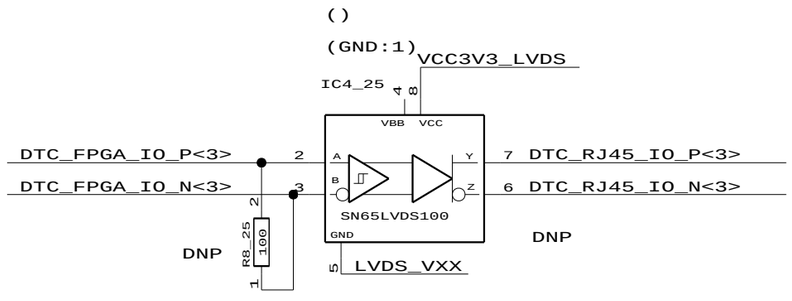
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TS/DEM

OUTPUTS

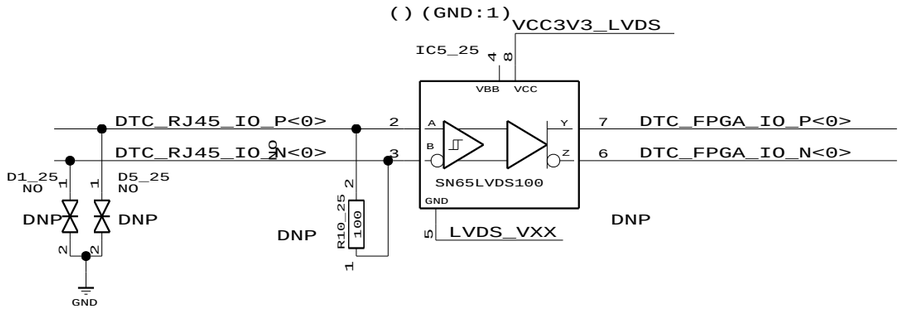


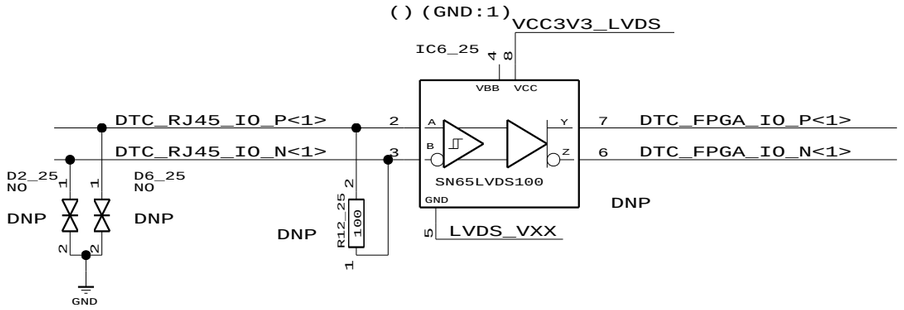


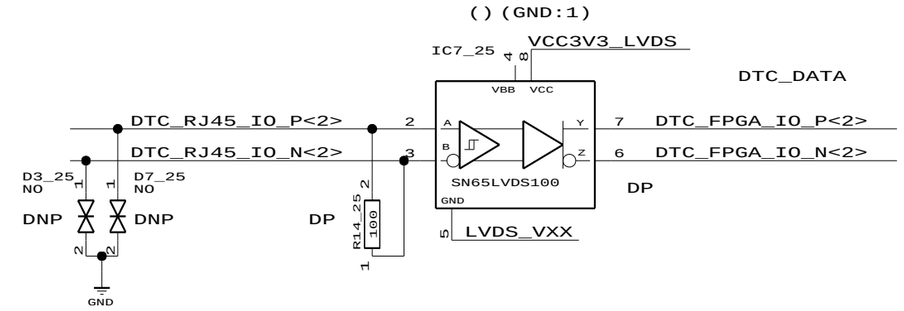


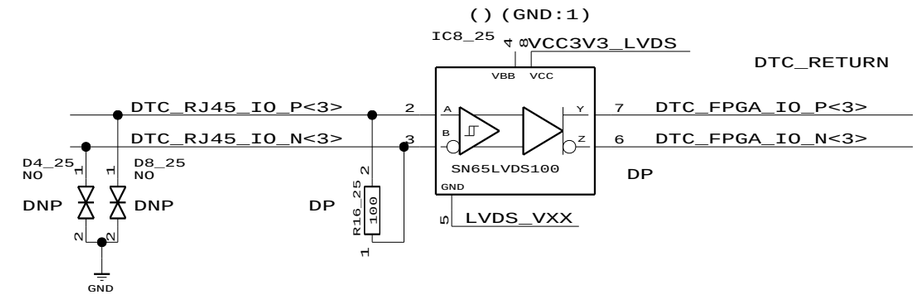


INPUTS

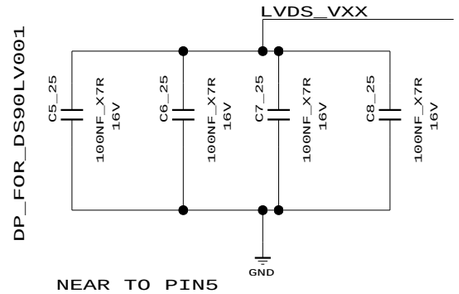




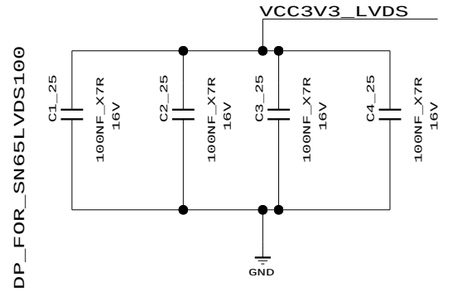




LOCAL DECOUPLING



NEAR TO PIN5



NEAR TO PIN8

IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

CERN TE/MPE European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND

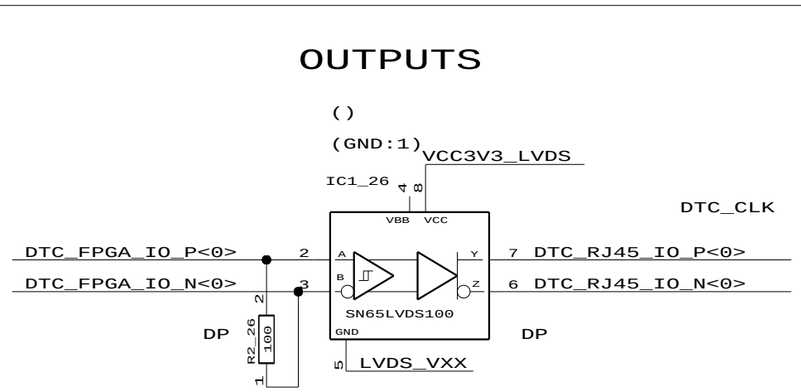
PROJECT:SRU v2.0

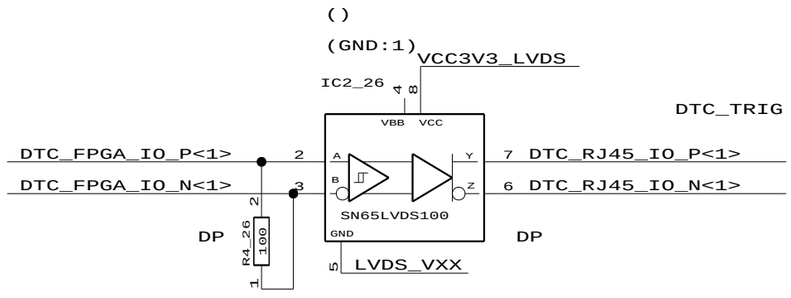
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 50/81

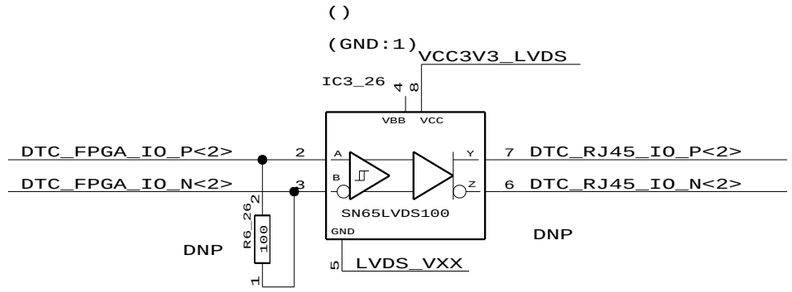
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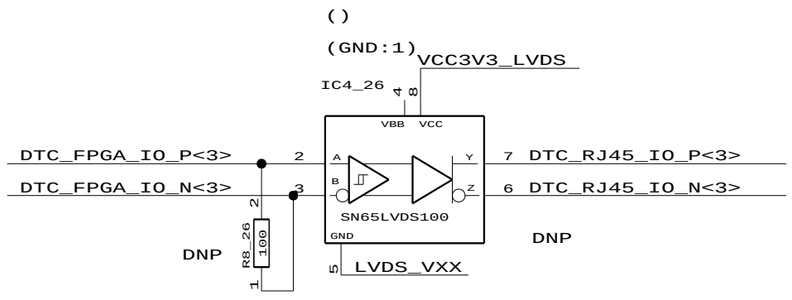
Design by: FZhang/SMartoiu PCB by: EXT DATE: 29/07/2010

OUTPUTS

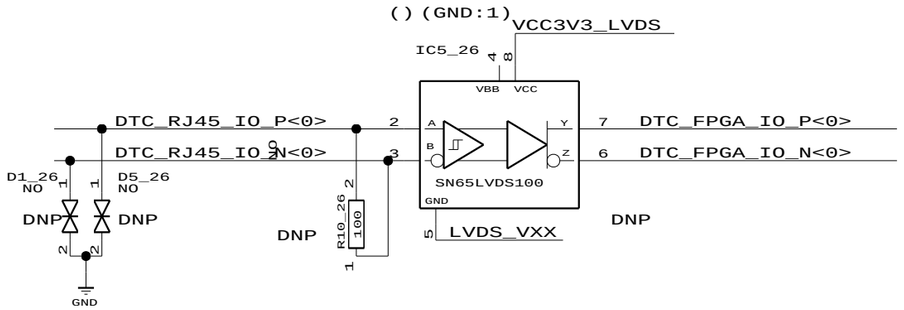


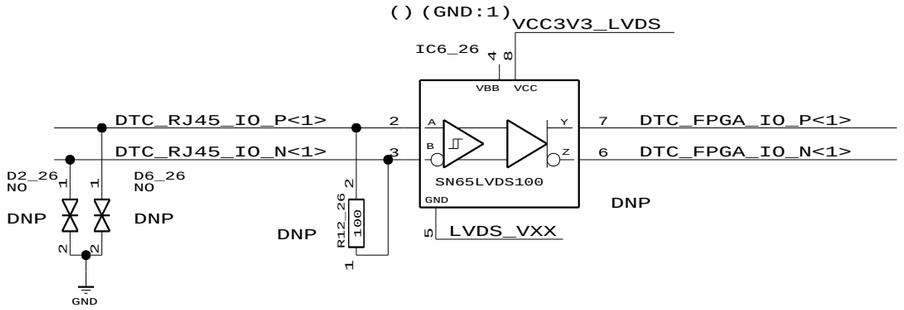


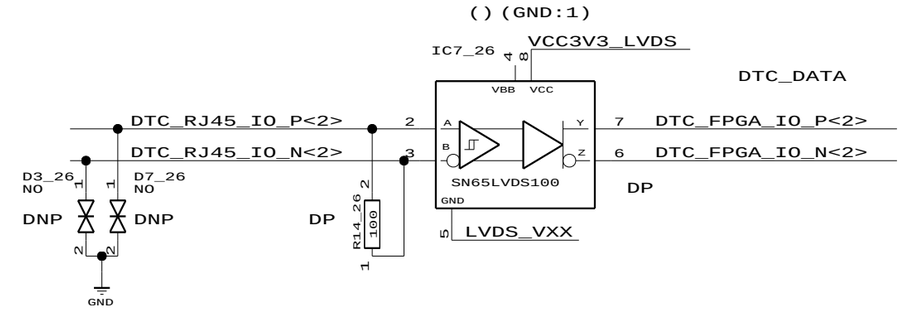


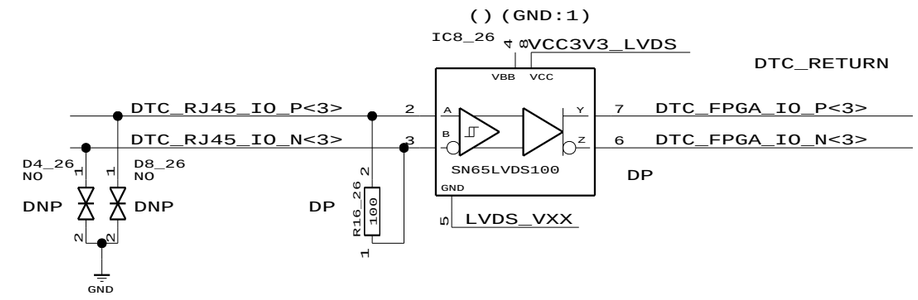


INPUTS

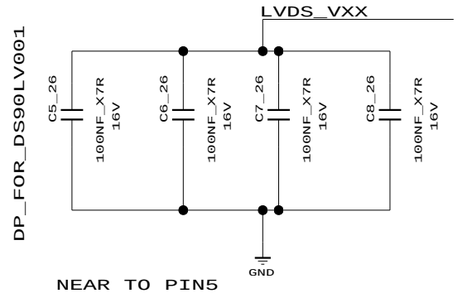


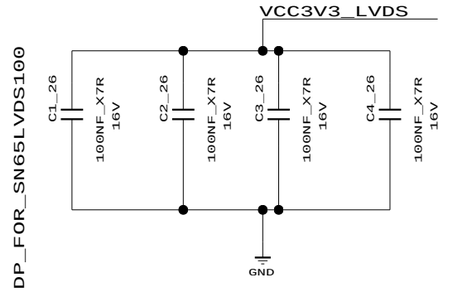






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA
- IO DTC_FPGA_IO_P<3..0>
- IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45
- IO DTC_RJ45_IO_P<3..0>
- IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

TE/MPE

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

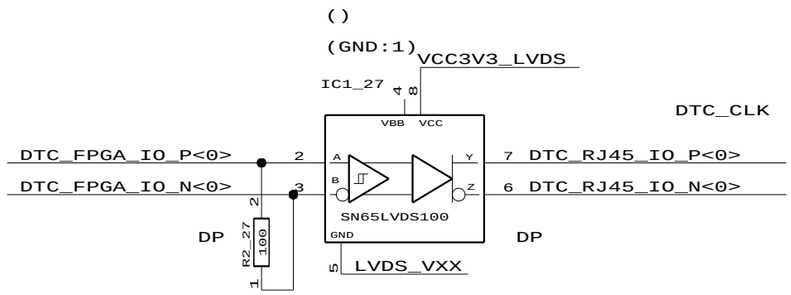
PROJECT:SRU v2.0

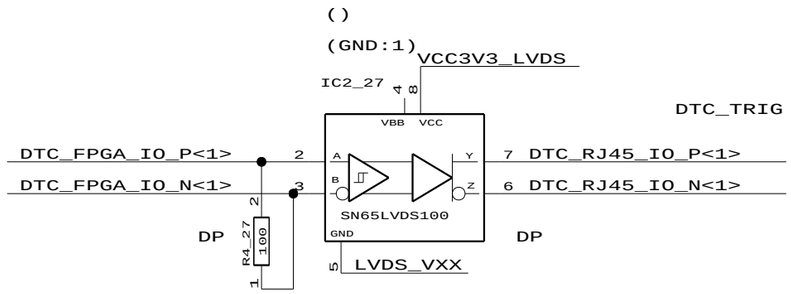
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 51/81

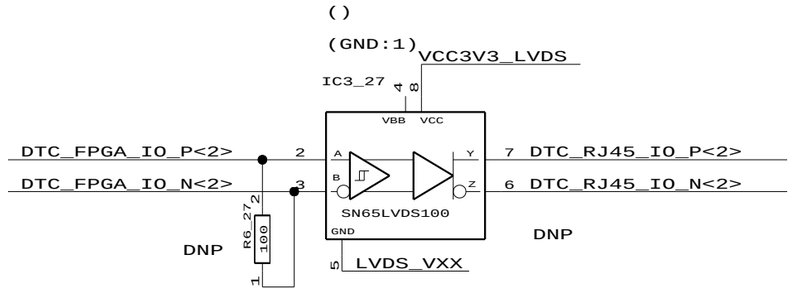
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

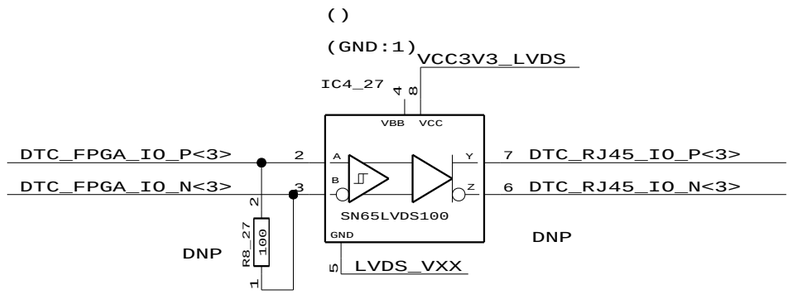
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

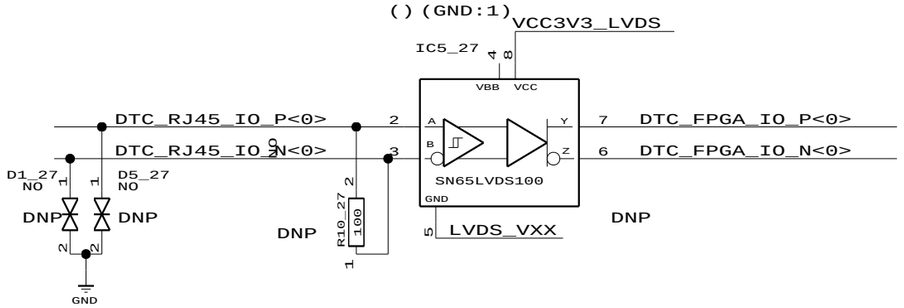


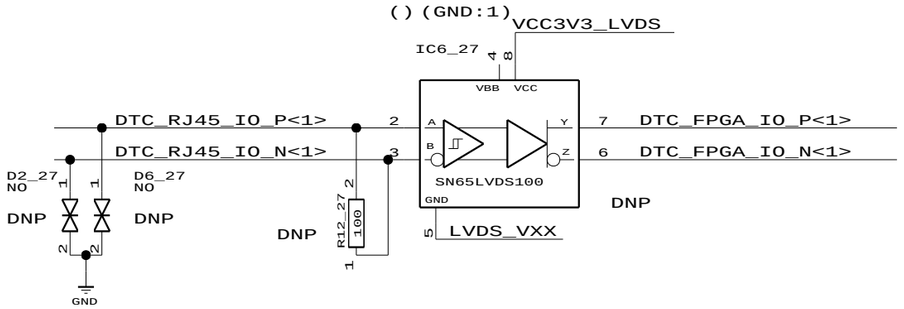


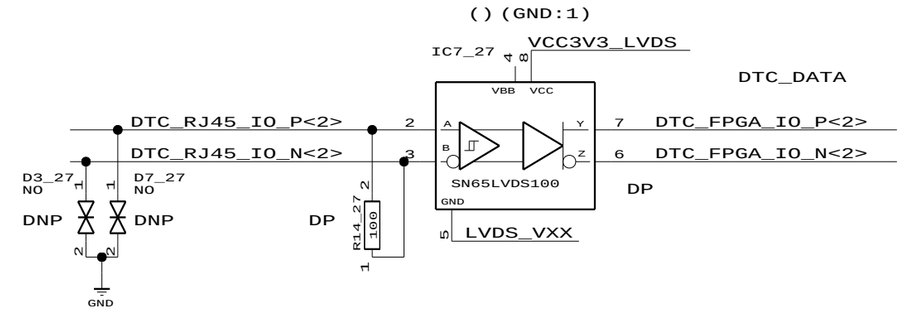


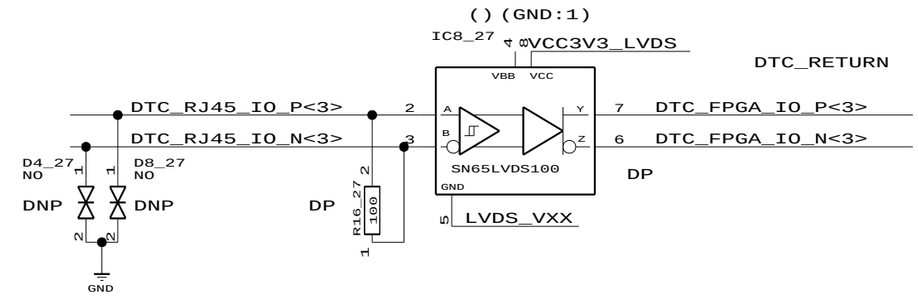


INPUTS

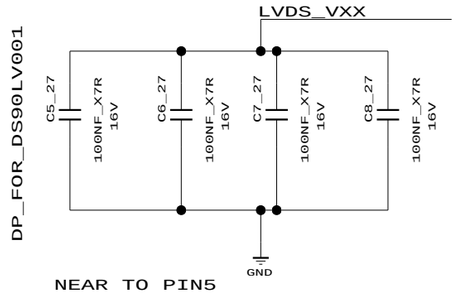


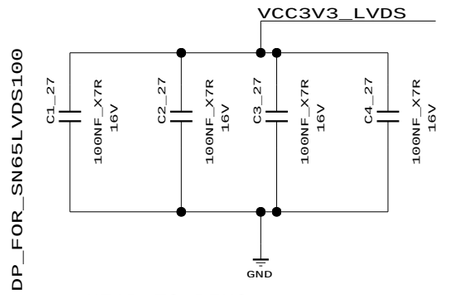






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

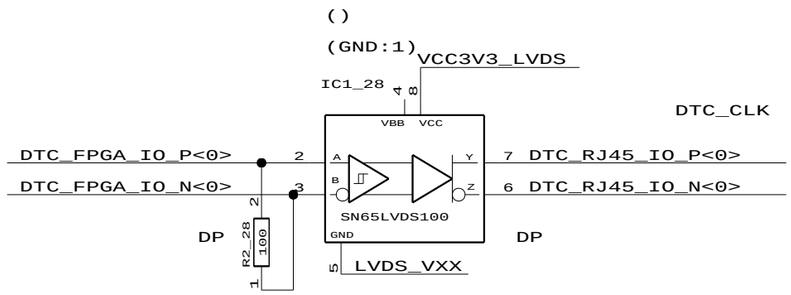
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for Nuclear Research
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SWITZERLAND
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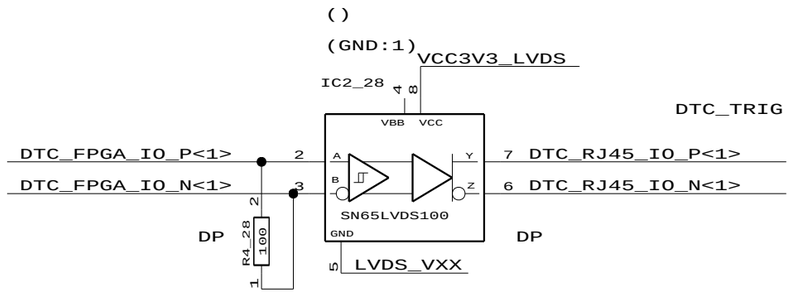
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 52/81

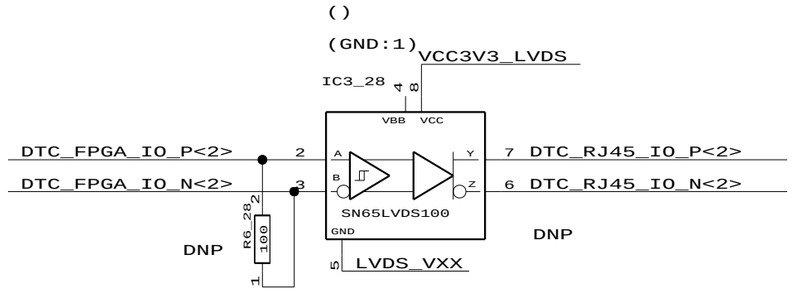
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

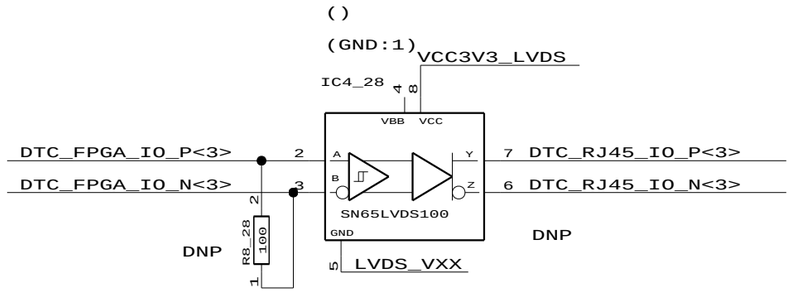
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

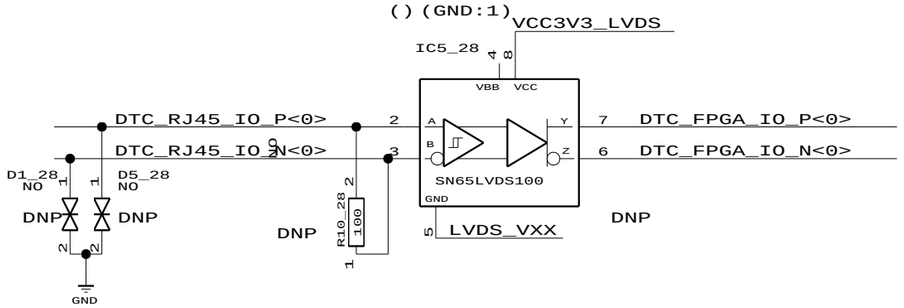


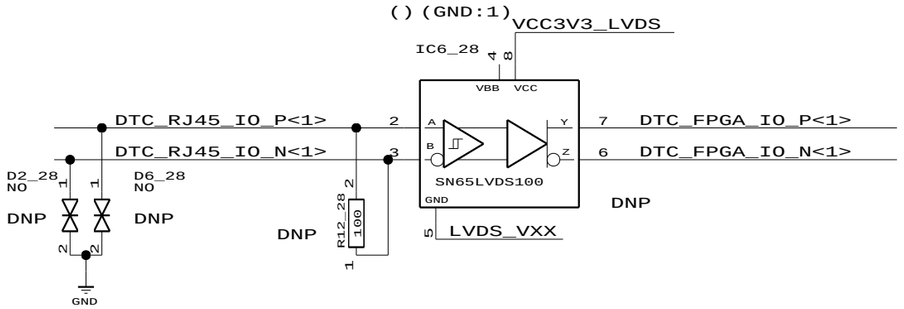


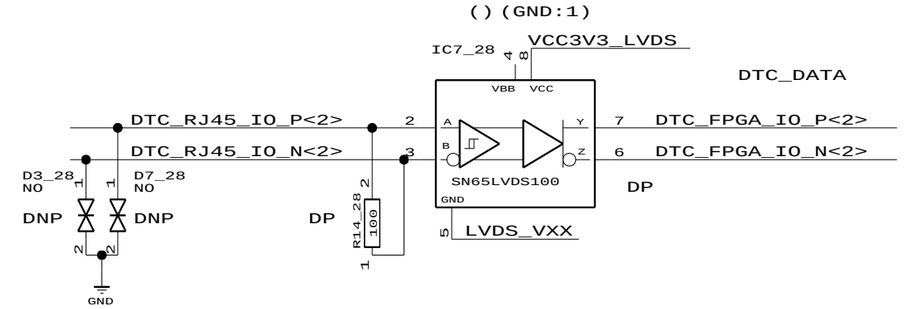


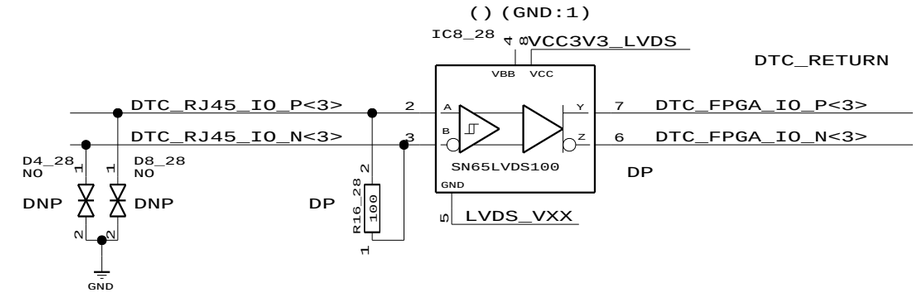


INPUTS

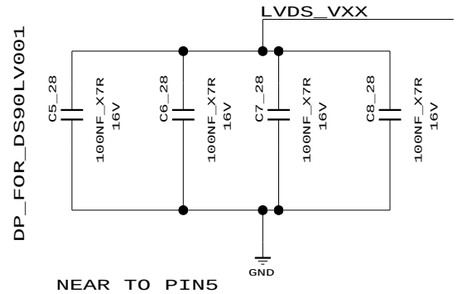


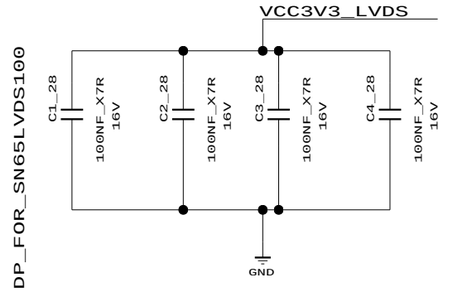






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

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MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 53/81

LAST_MODIFIED=Mon Dec 12 10:53:50 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

()
(GND:1)
VCC3V3_LVDS
IC1_29
DTC_CLK
DTC_FPGA_IO_P<0>
DTC_FPGA_IO_N<0>
DTC_RJ45_IO_P<0>
DTC_RJ45_IO_N<0>
SN65LVDS100
DP
DP
R2_29
100
LVDS_VXX

()
(GND:1)
VCC3V3_LVDS
IC2_29
DTC_TRIG
DTC_FPGA_IO_P<1>
DTC_FPGA_IO_N<1>
DTC_RJ45_IO_P<1>
DTC_RJ45_IO_N<1>
SN65LVDS100
DP
DP
R4_29
100
LVDS_VXX

()
(GND:1)
VCC3V3_LVDS
IC3_29
DTC_FPGA_IO_P<2>
DTC_FPGA_IO_N<2>
DTC_RJ45_IO_P<2>
DTC_RJ45_IO_N<2>
SN65LVDS100
DNP
DNP
R6_29
100
LVDS_VXX

()
(GND:1)
VCC3V3_LVDS
IC4_29
DTC_FPGA_IO_P<3>
DTC_FPGA_IO_N<3>
DTC_RJ45_IO_P<3>
DTC_RJ45_IO_N<3>
SN65LVDS100
DNP
DNP
R8_29
100
LVDS_VXX

INPUTS

()(GND:1)
VCC3V3_LVDS
IC5_29
DTC_RJ45_IO_P<0>
DTC_RJ45_IO_N<0>
DTC_FPGA_IO_P<0>
DTC_FPGA_IO_N<0>
SN65LVDS100
D1_29
NO
D5_29
NO
DNP
DNP
DNP
DNP
R10_29
100
LVDS_VXX
GND

()(GND:1)
VCC3V3_LVDS
IC6_29
DTC_RJ45_IO_P<1>
DTC_RJ45_IO_N<1>
DTC_FPGA_IO_P<1>
DTC_FPGA_IO_N<1>
SN65LVDS100
D2_29
NO
D6_29
NO
DNP
DNP
DNP
DNP
R12_29
100
LVDS_VXX
GND

()(GND:1)
VCC3V3_LVDS
IC7_29
DTC_DATA
DTC_RJ45_IO_P<2>
DTC_RJ45_IO_N<2>
DTC_FPGA_IO_P<2>
DTC_FPGA_IO_N<2>
SN65LVDS100
D3_29
NO
D7_29
NO
DNP
DNP
DP
DP
R14_29
100
LVDS_VXX
GND

()(GND:1)
VCC3V3_LVDS
IC8_29
DTC_RETURN
DTC_RJ45_IO_P<3>
DTC_RJ45_IO_N<3>
DTC_FPGA_IO_P<3>
DTC_FPGA_IO_N<3>
SN65LVDS100
D4_29
NO
D8_29
NO
DNP
DNP
DP
DP
R16_29
100
LVDS_VXX
GND

LOCAL DECOUPLING

DP_FOR_DS90LV001
LVDS_VXX
C5_29 100NF_X7R 16V
C6_29 100NF_X7R 16V
C7_29 100NF_X7R 16V
C8_29 100NF_X7R 16V
GND
NEAR TO PIN5

DP_FOR_SN65LVDS100
VCC3V3_LVDS
C1_29 100NF_X7R 16V
C2_29 100NF_X7R 16V
C3_29 100NF_X7R 16V
C4_29 100NF_X7R 16V
GND
NEAR TO PIN8

IN LVDS_VXX
IN VCC3V3_LVDS

TO THE FPGA
IO DTC_FPGA_IO_P<3..0>
IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45
IO DTC_RJ45_IO_P<3..0>
IO DTC_RJ45_IO_N<3..0>

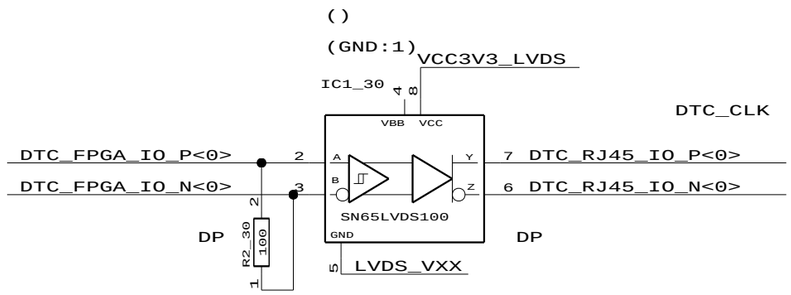
Project file:sru_rev2.cpm
SYSTEM:

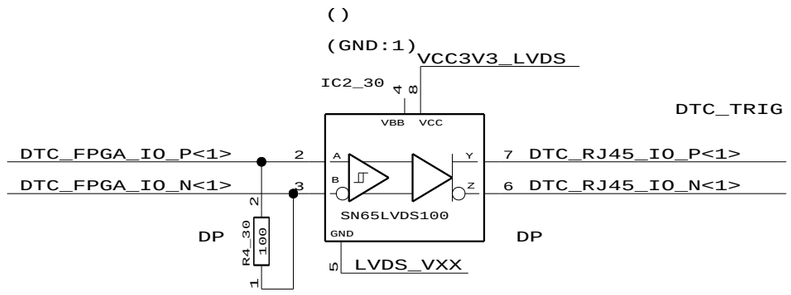
PROJECT:SRU v2.0

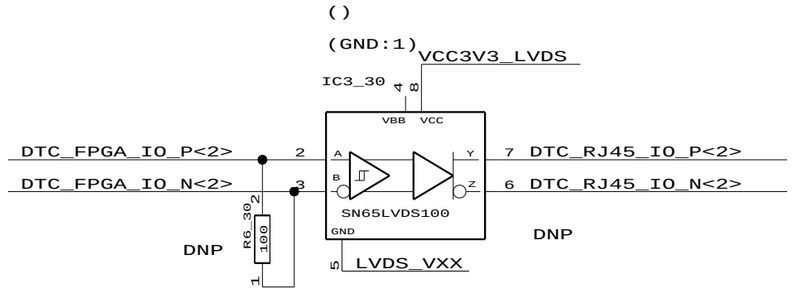
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for Nuclear Research
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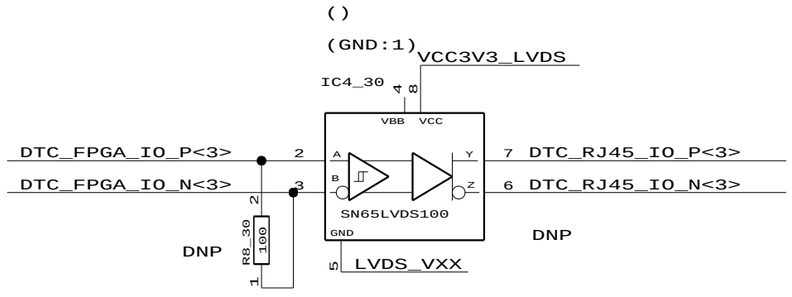
MODULE:lvds_1x_rj45
Sheet: 1/1
Module: 1/1
Project: 54/81
LAST_MODIFIED=Mon Dec 12 10:53:50 2011
Design by: FZhang/SMartoiu
PCB by: EXT
DATE: 29/07/2010

OUTPUTS

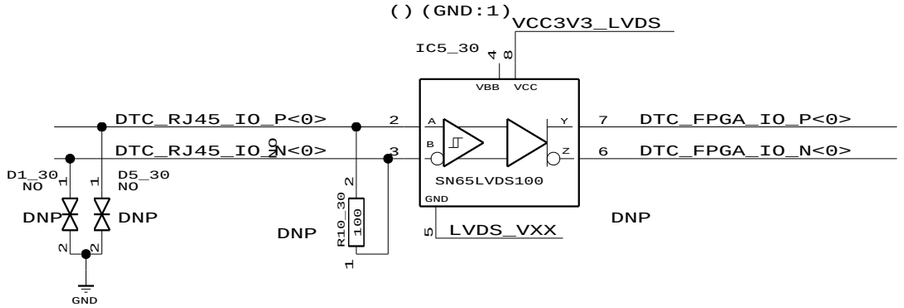


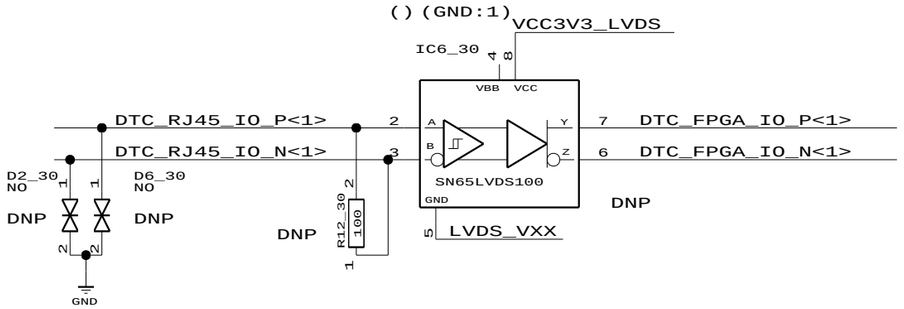


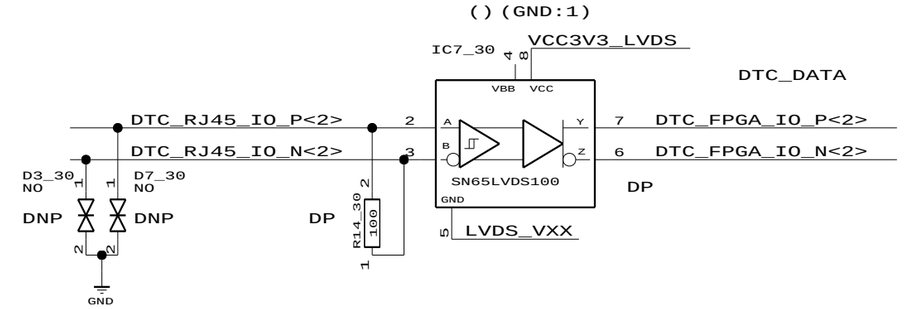


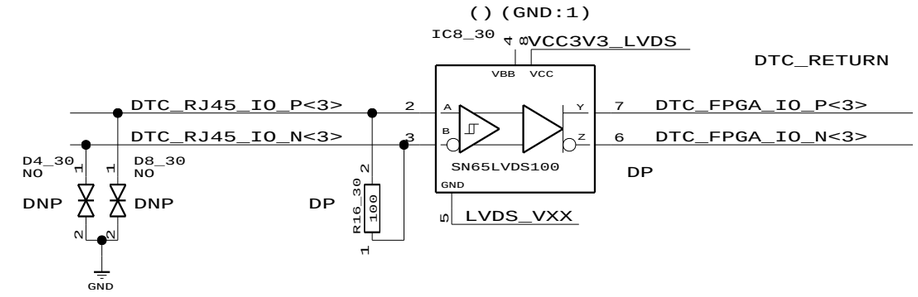


INPUTS

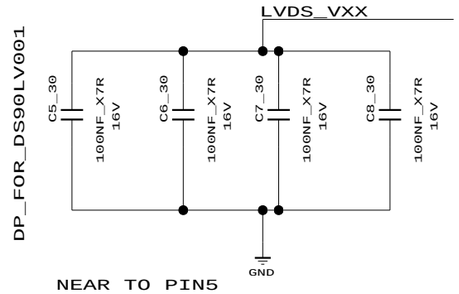


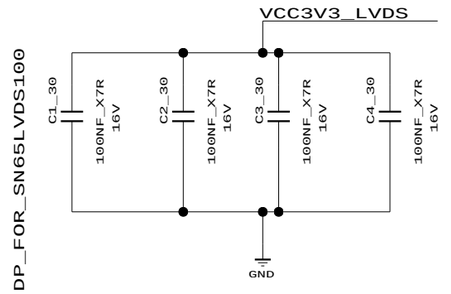






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

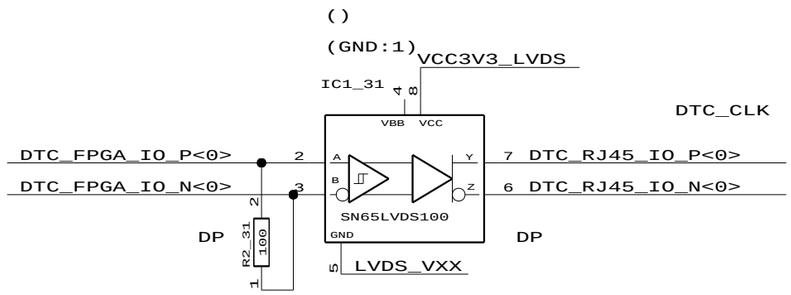
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for Nuclear Research
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TE/MPE

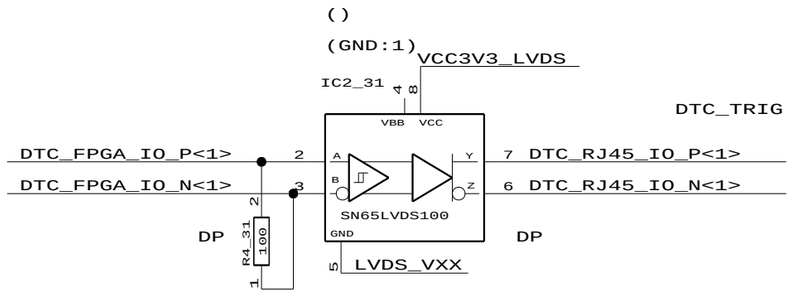
MODULE:lvds_1x_rj45 Sheet: Module: 1/1 Project: 55/81

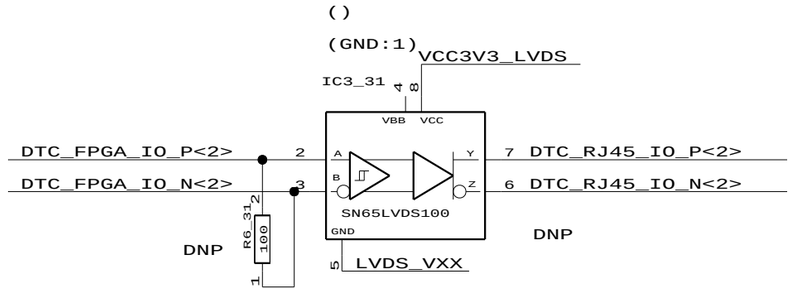
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

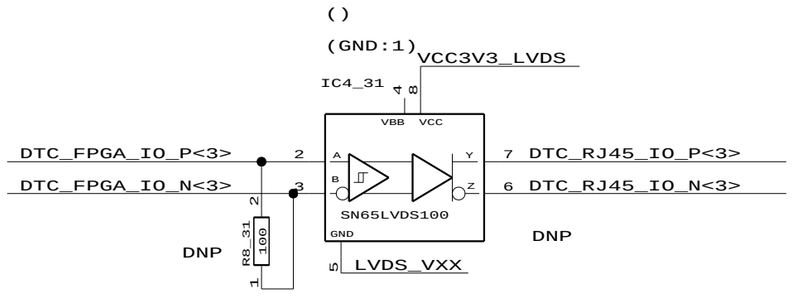
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

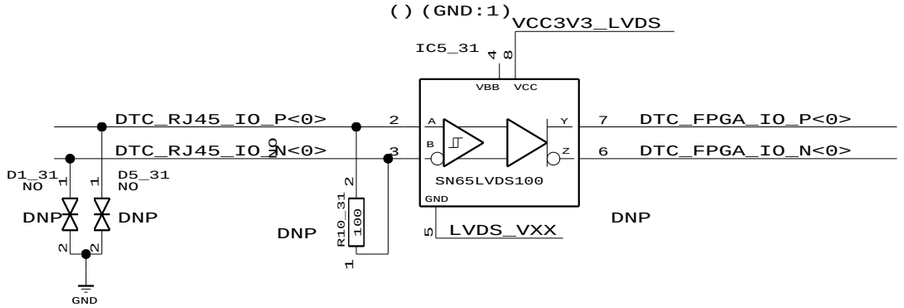


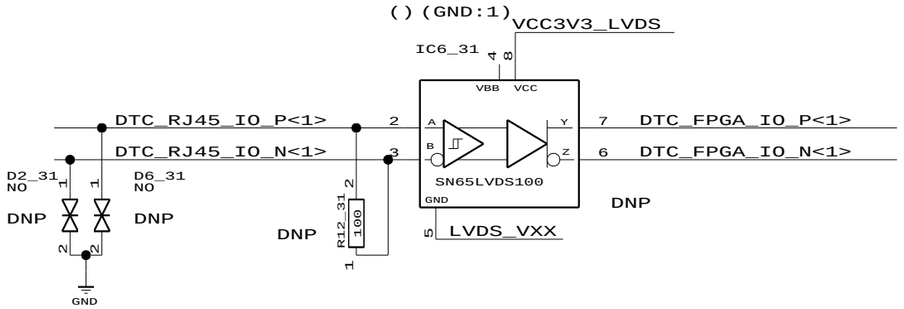


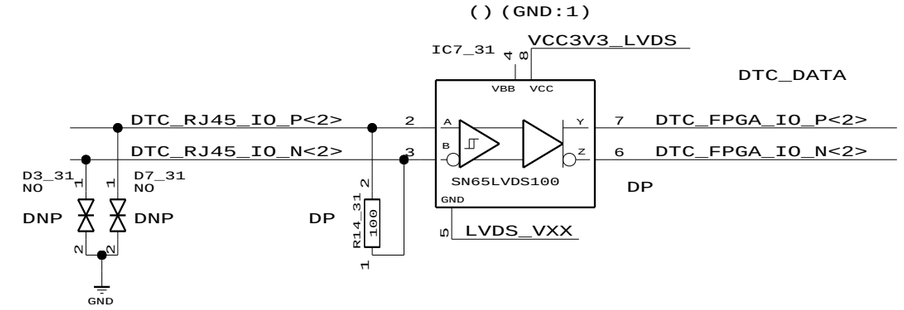


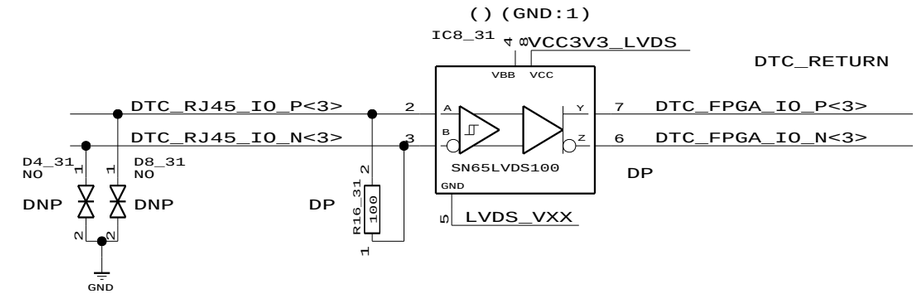


INPUTS

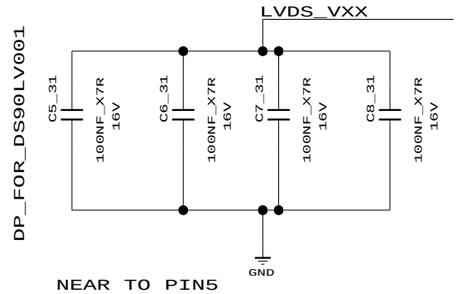


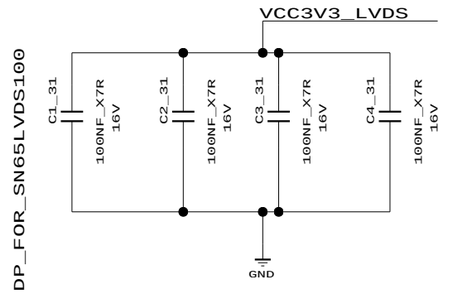






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

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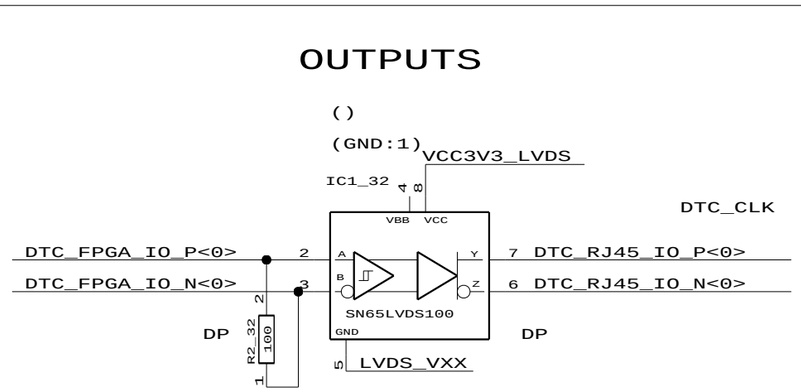
PROJECT:SRU v2.0

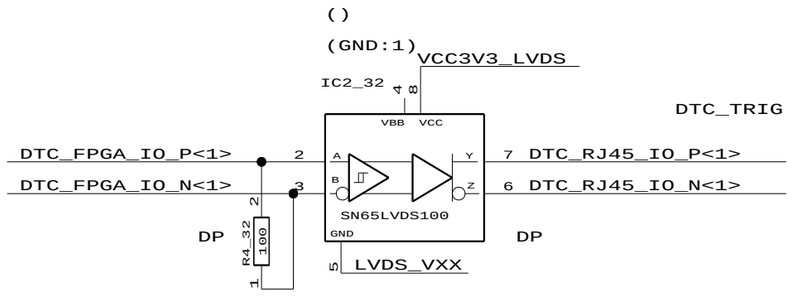
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 56/81

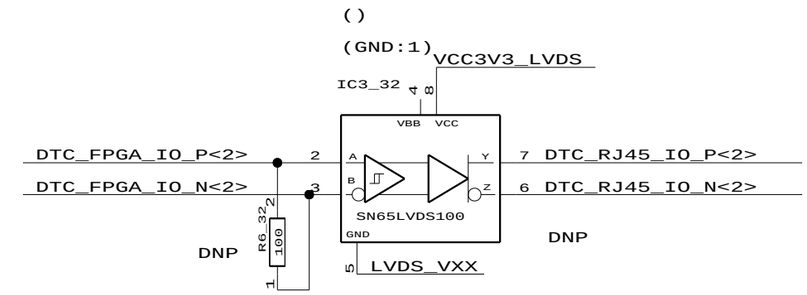
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

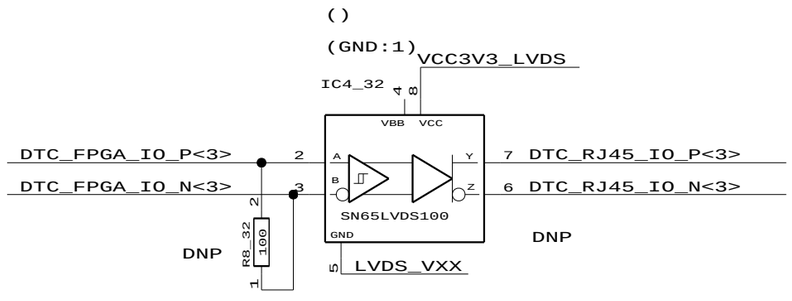
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

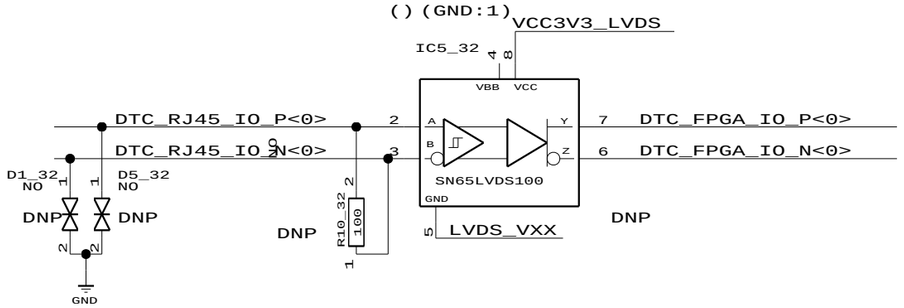


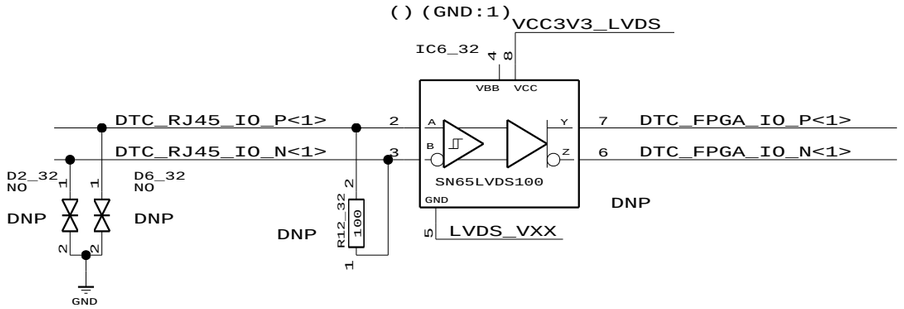


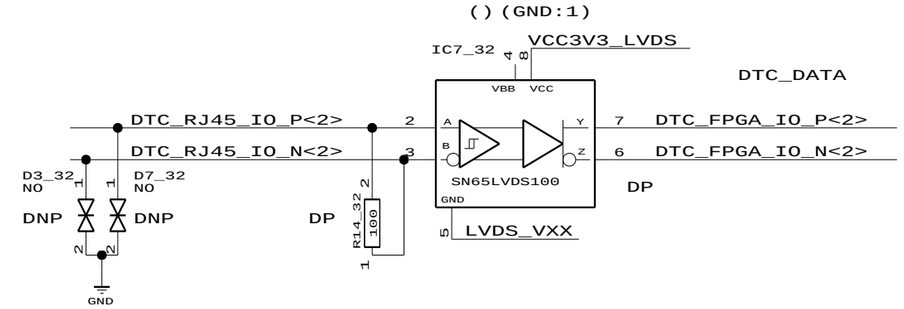


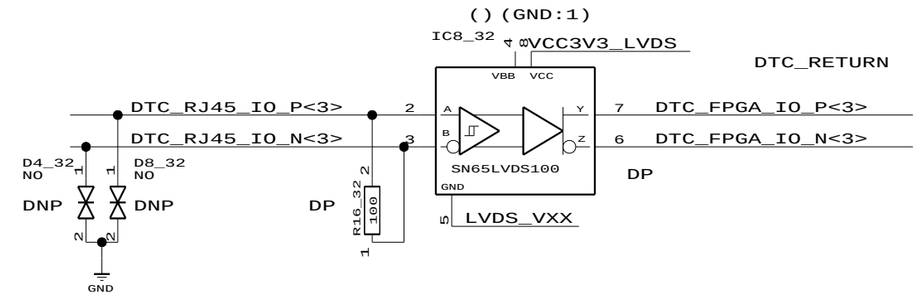


INPUTS

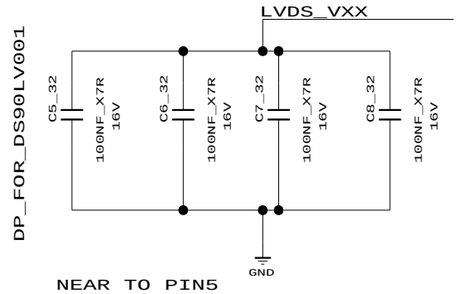


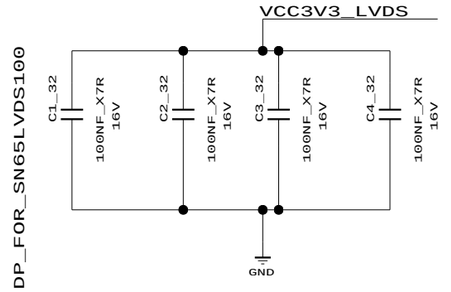






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

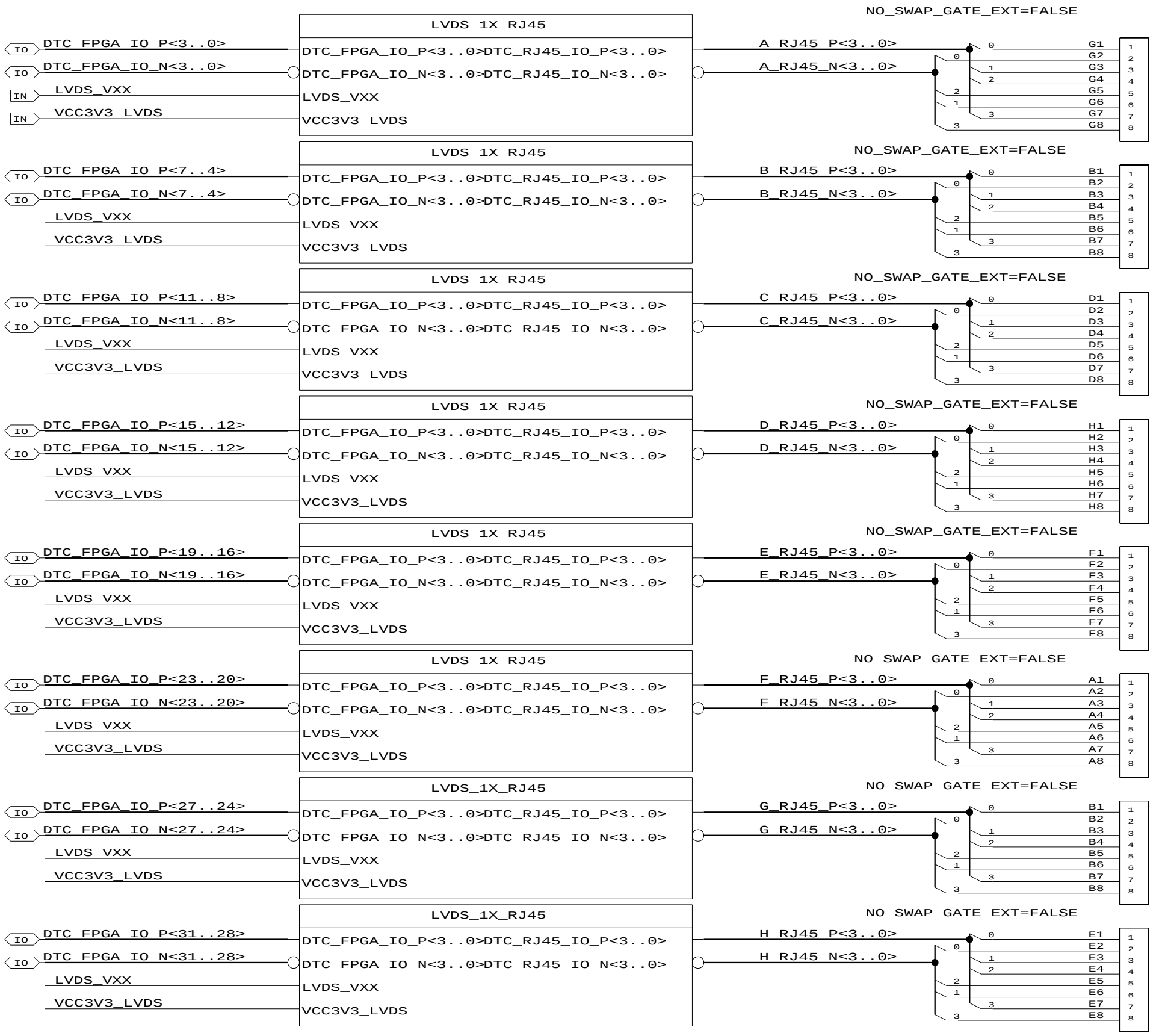
PROJECT:SRU v2.0

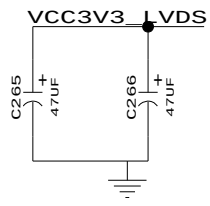
European Organization for Nuclear Research
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SWITZERLAND
TE/MPE

MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 57/81

LAST_MODIFIED=Mon Dec 12 10:53:50 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010





PLACE THIS DECOUPLING CAPACITORS
AROUND THE AROUND THE AREA
OF THIS 2*4 RJ45

Project file:sru_rev2.cpm

SYSTEM:

PROJECT:SRU v2.0

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

TS/DEM

MODULE:lvds_8x_rj45

Sheet: Module: 1/1 Project: 58/81

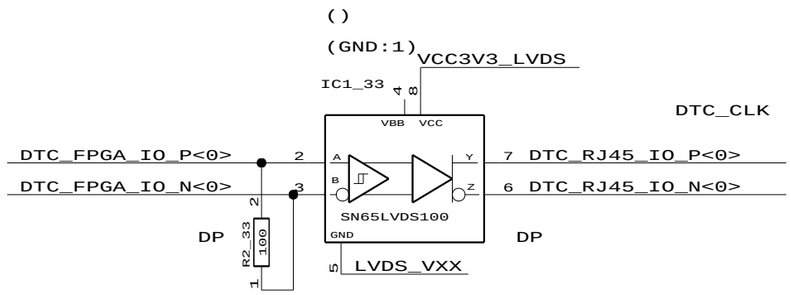
LAST_MODIFIED=Fri Dec 09 11:01:52 2011

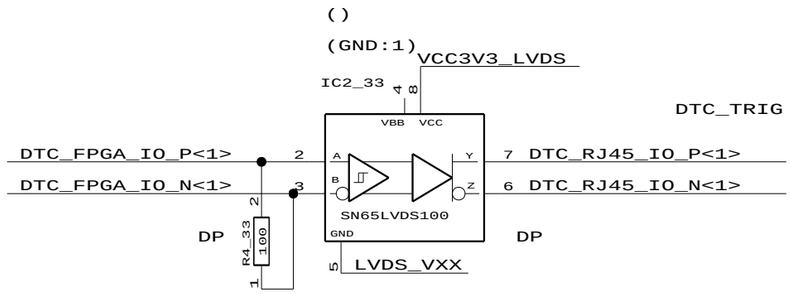
Design by: FZhang/SMartoiu

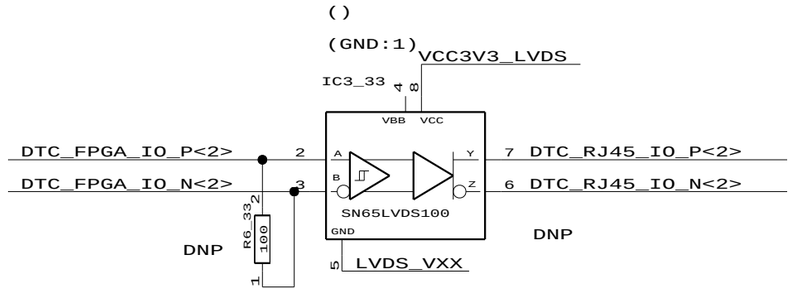
PCB by: EXT

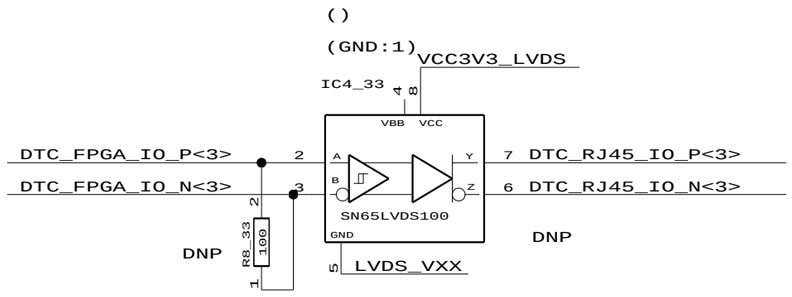
DATE: 29/07/2010

OUTPUTS

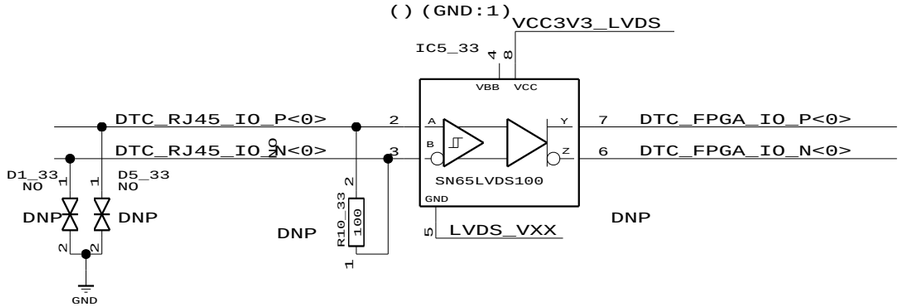


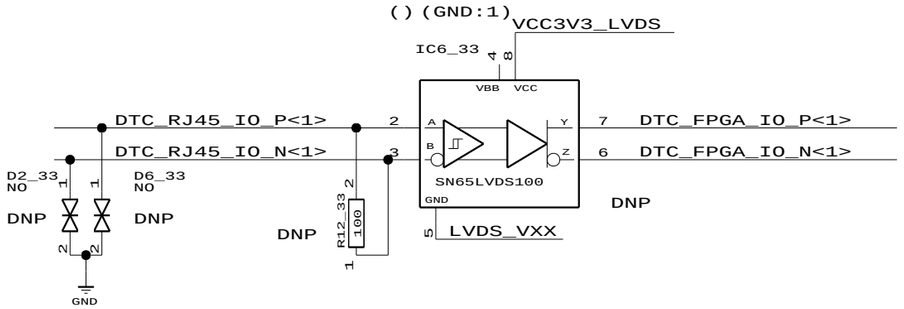


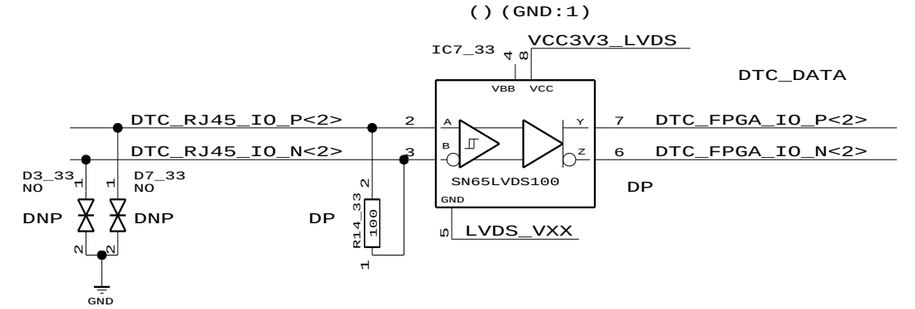


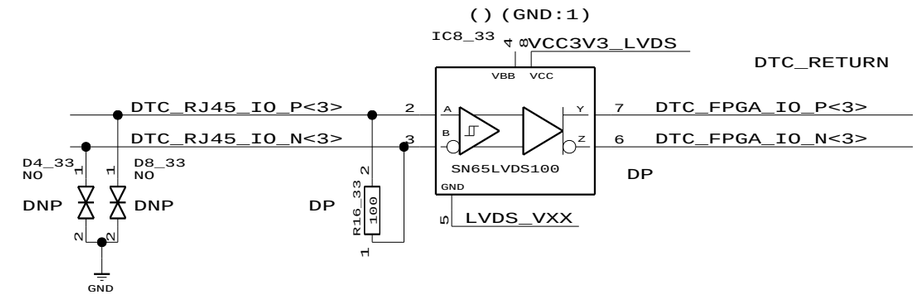


INPUTS

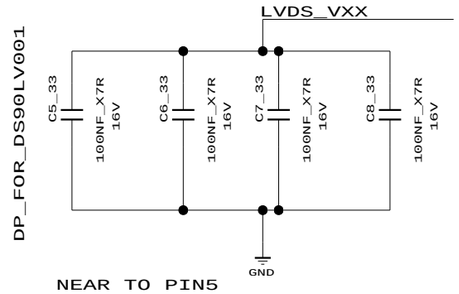


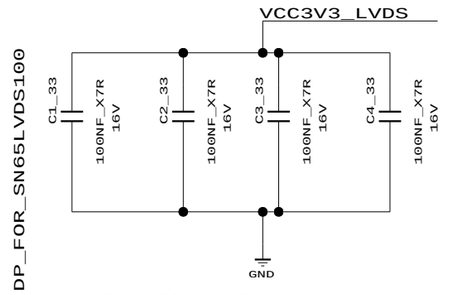






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA
- IO DTC_FPGA_IO_P<3..0>
- IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45
- IO DTC_RJ45_IO_P<3..0>
- IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

TE/MPE

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

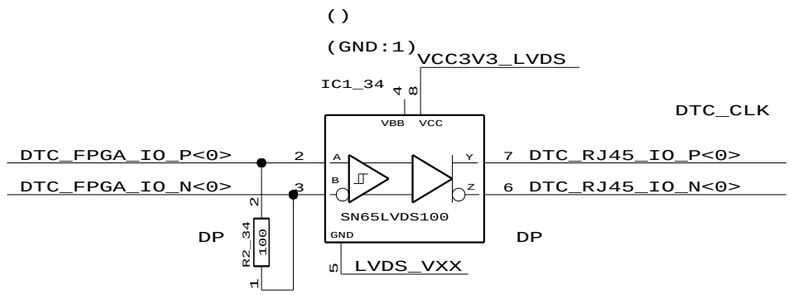
PROJECT:SRU v2.0

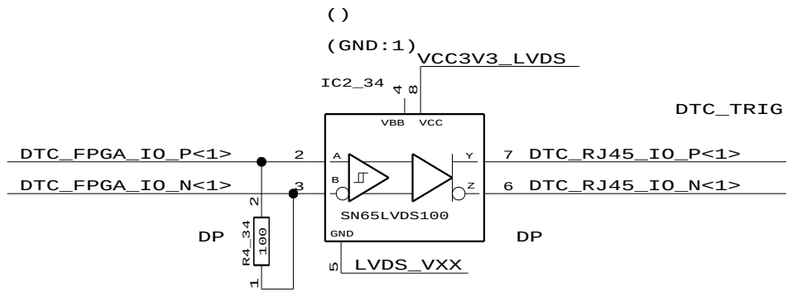
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 59/81

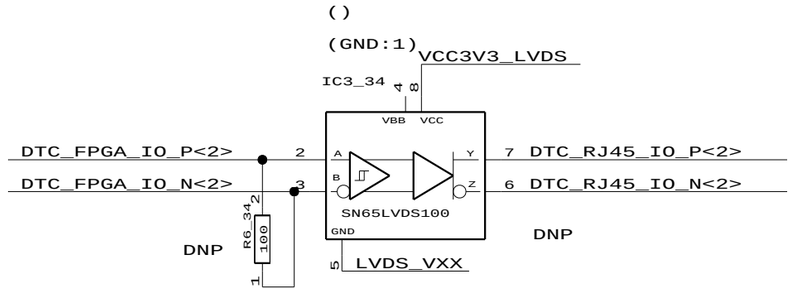
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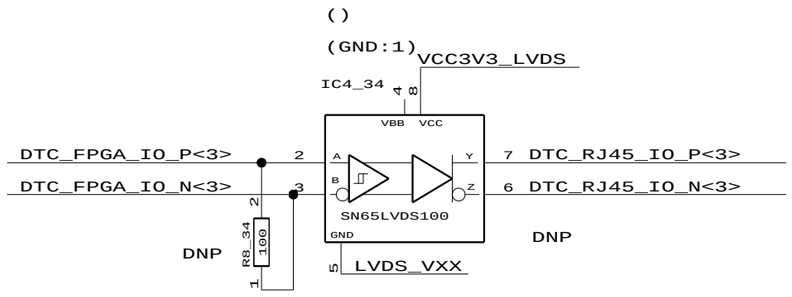
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

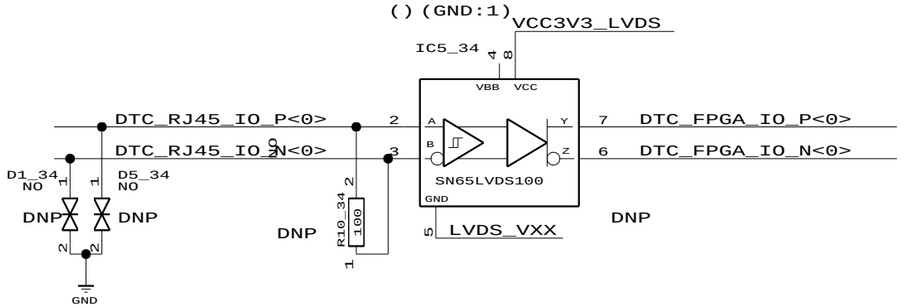


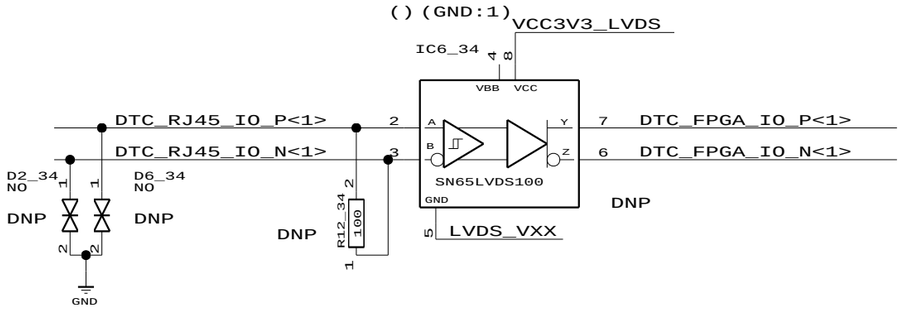


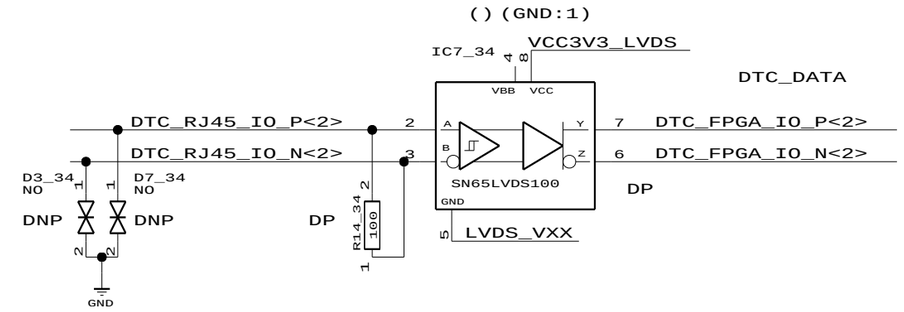


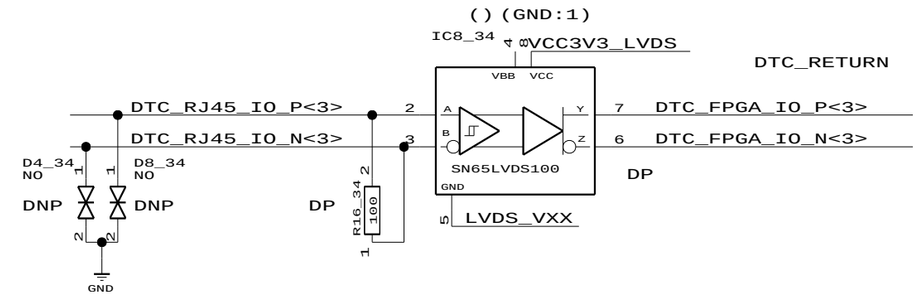


INPUTS

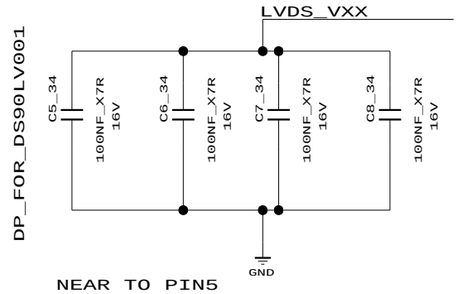


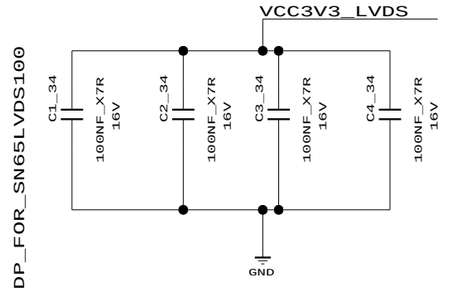






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

TE/MPE

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

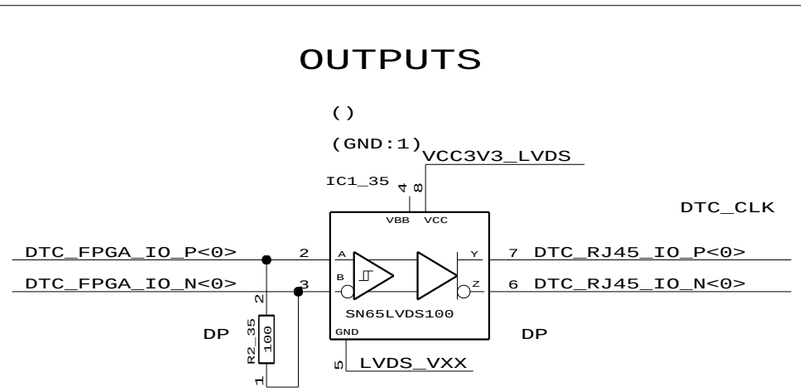
PROJECT:SRU v2.0

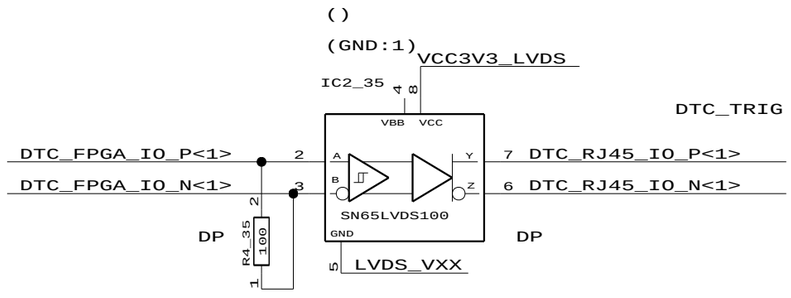
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 60/81

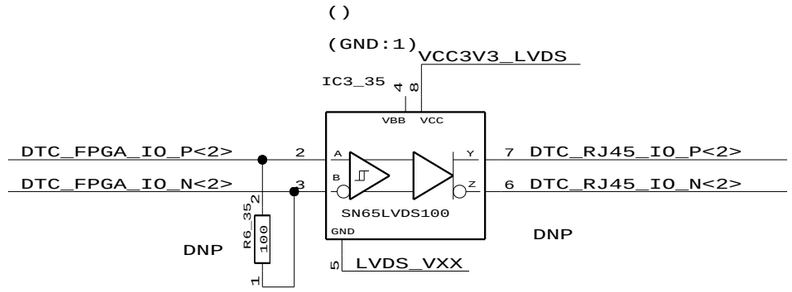
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

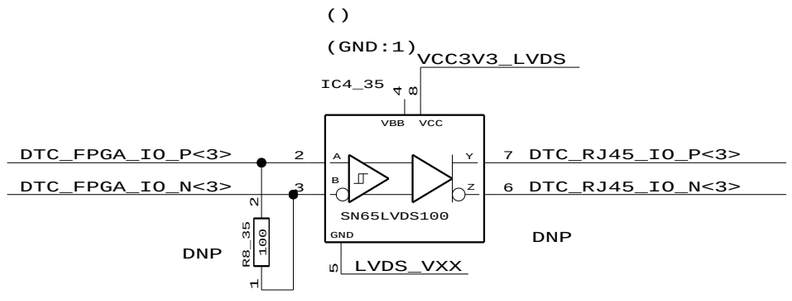
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

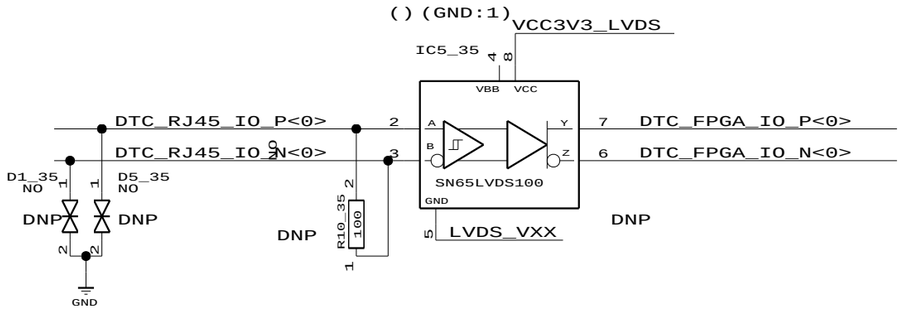


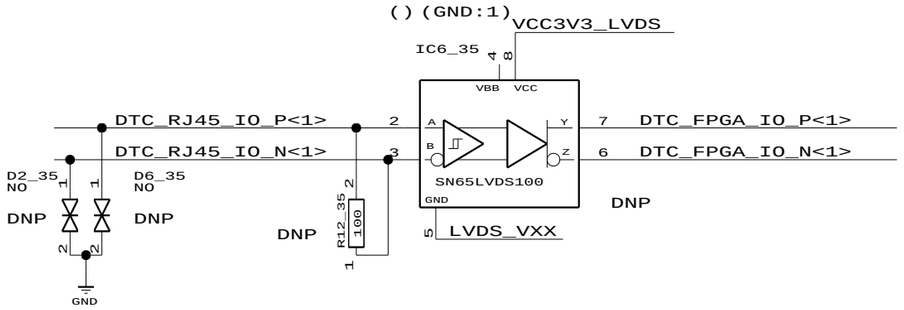


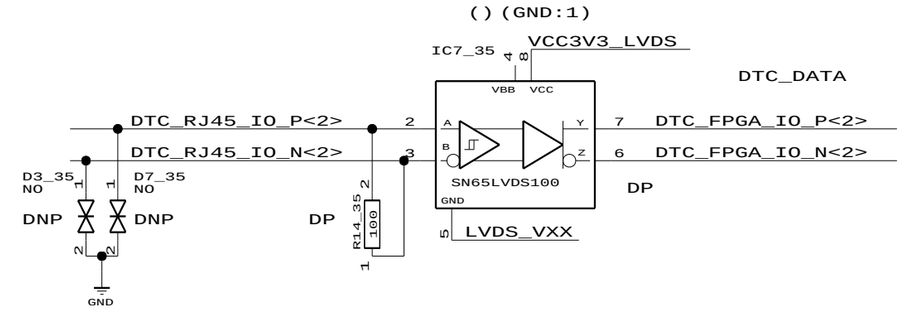


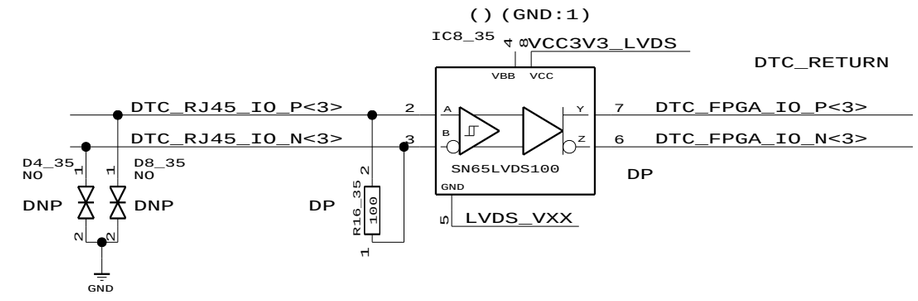


INPUTS

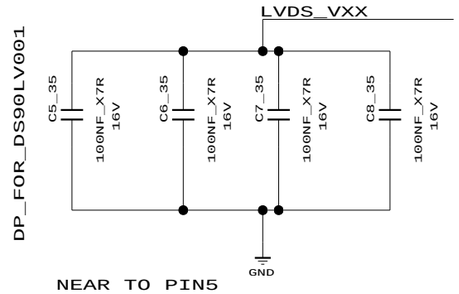


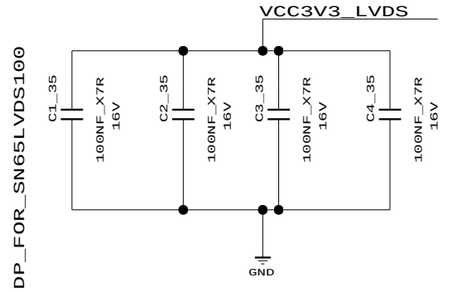






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

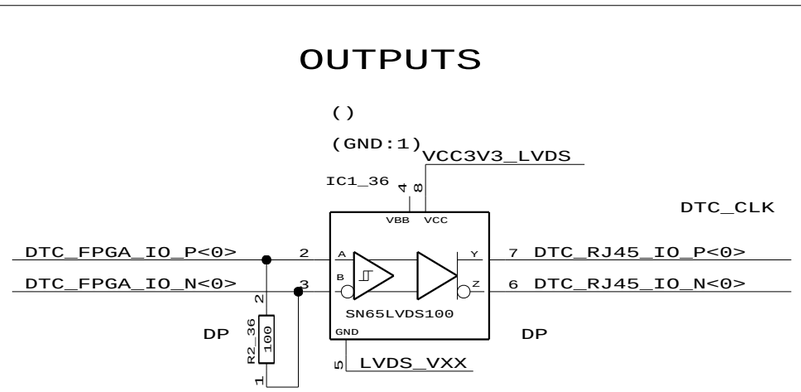
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

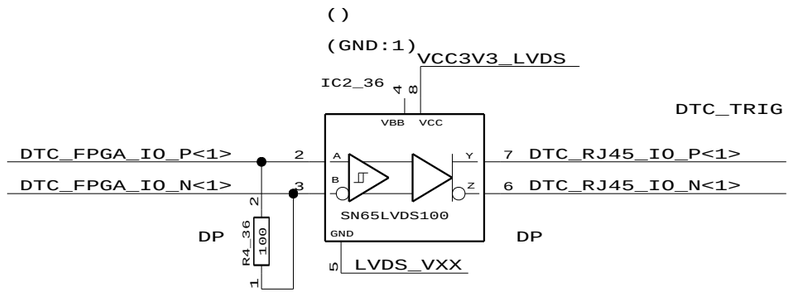
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 61/81

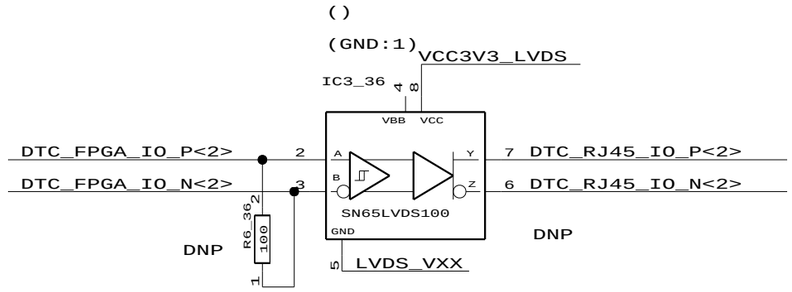
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

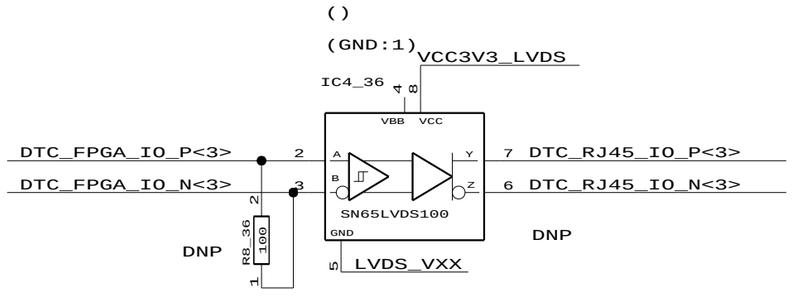
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

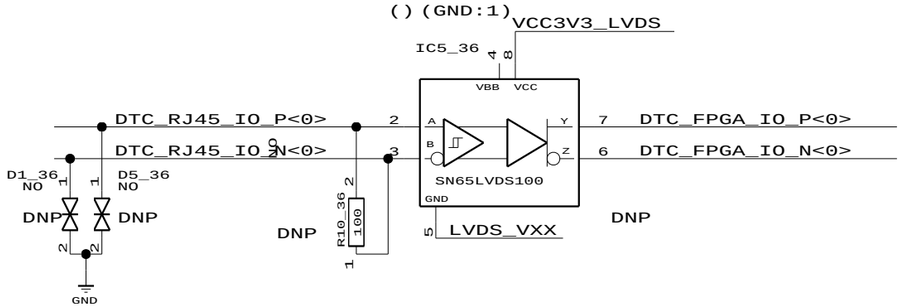


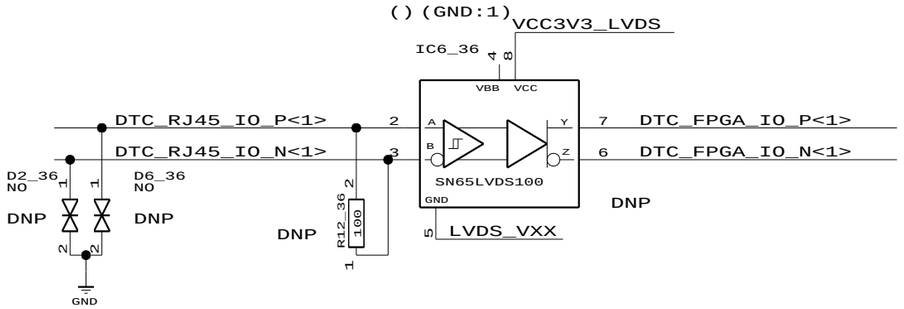


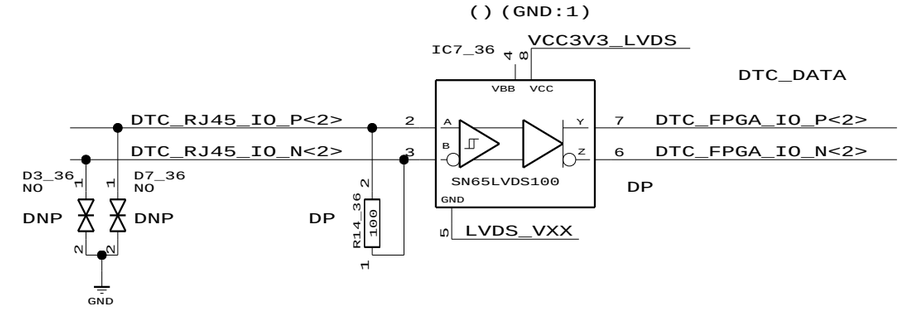


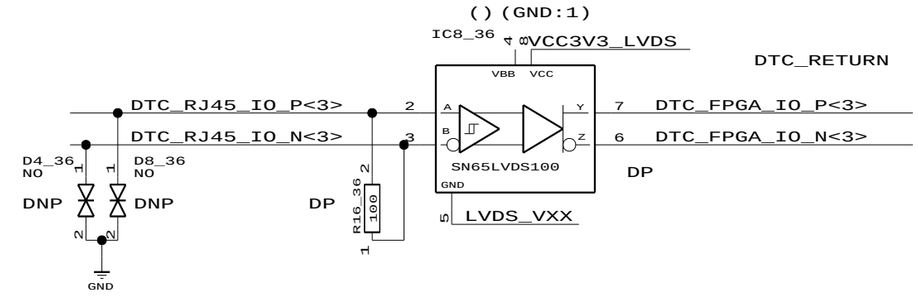


INPUTS

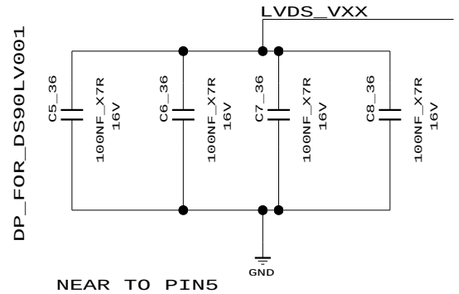


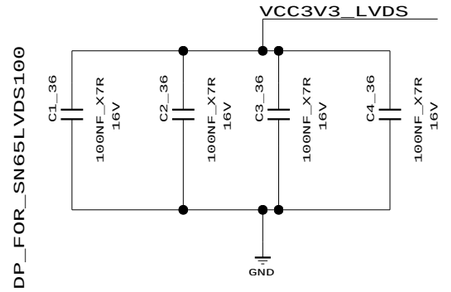






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

CERN TE/MPE European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND

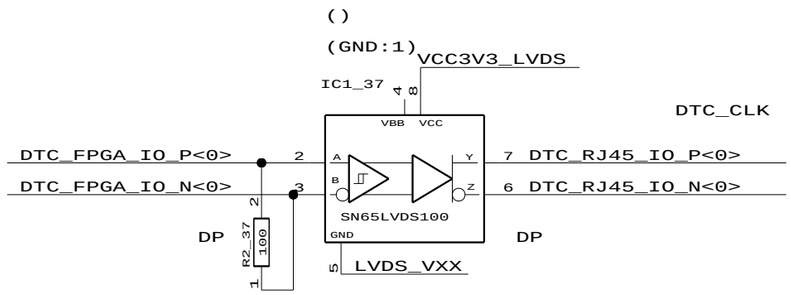
PROJECT:SRU v2.0

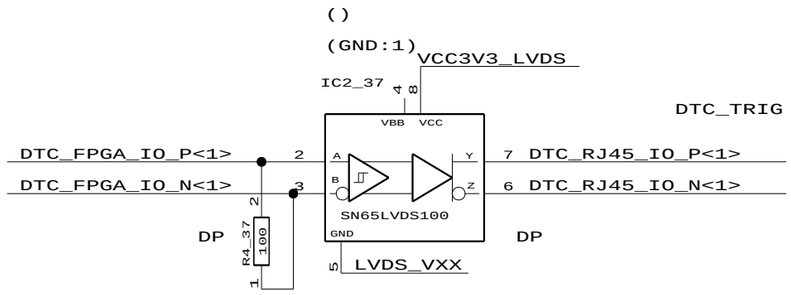
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 62/81

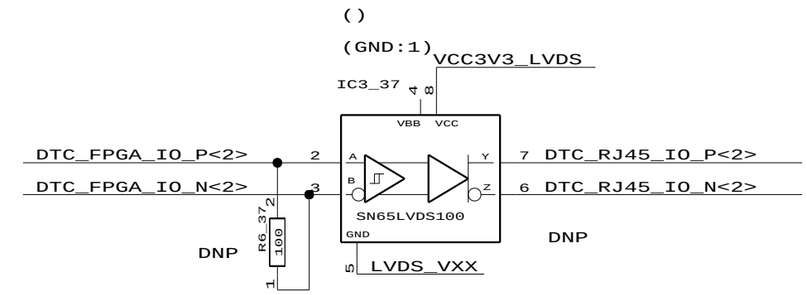
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

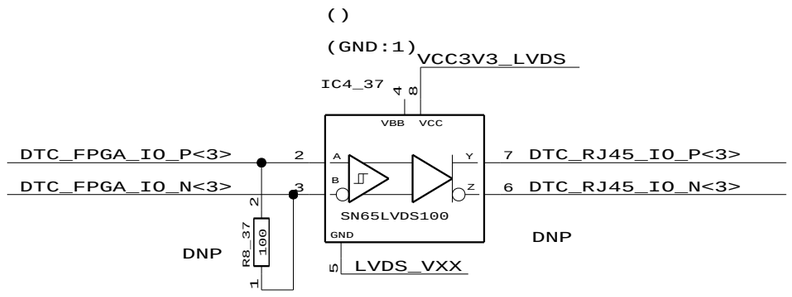
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

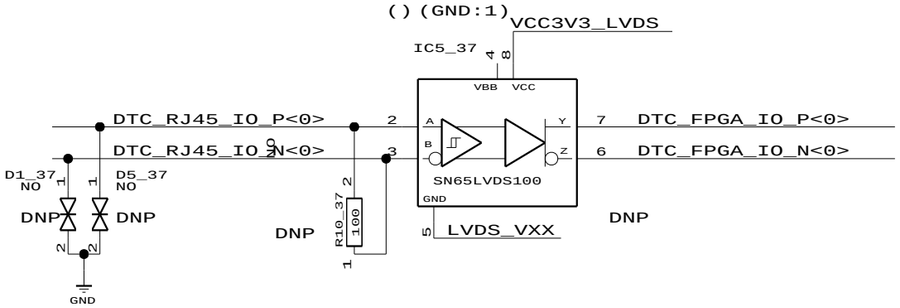


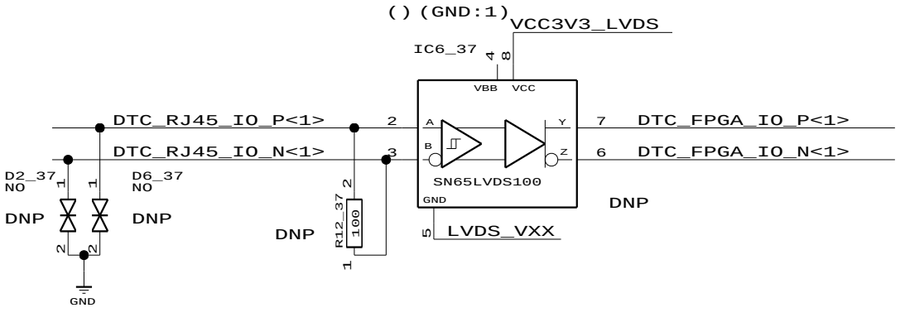


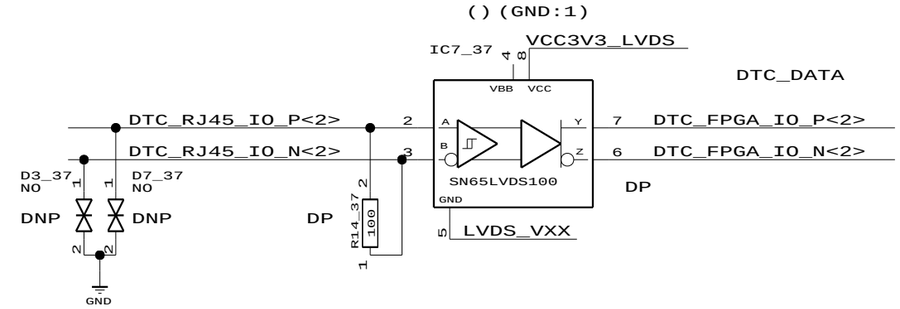


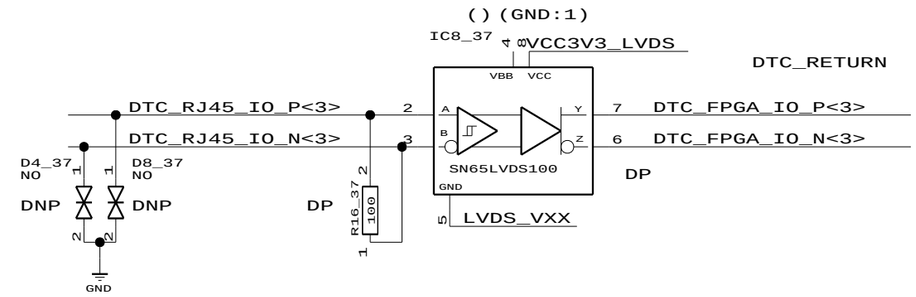


INPUTS

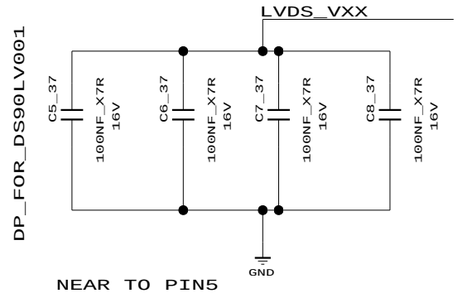


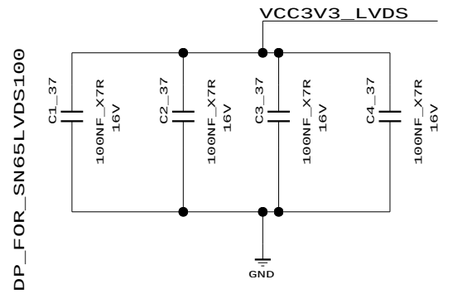






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

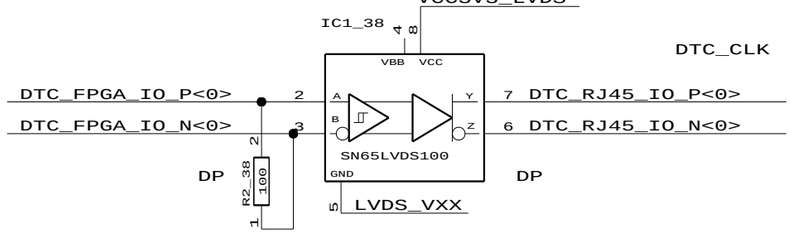
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 63/81

LAST_MODIFIED=Mon Dec 12 10:53:50 2011

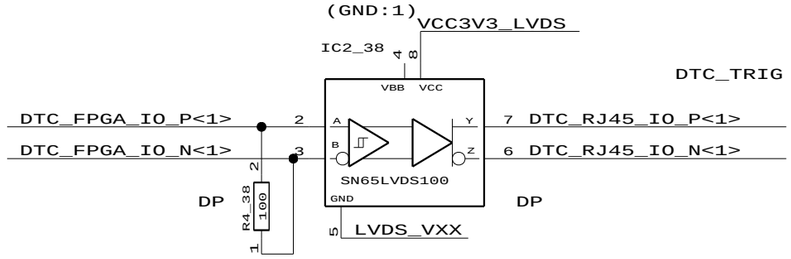
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

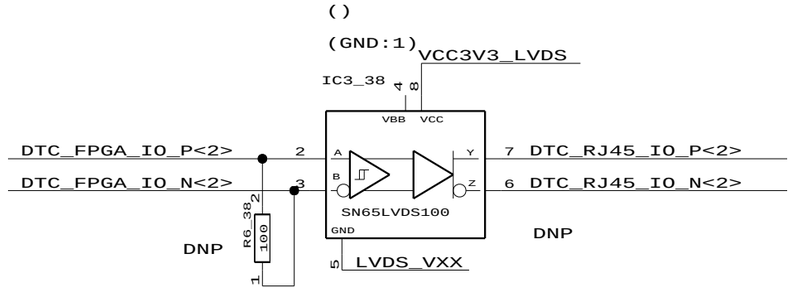
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(GND:1)
VCC3V3_LVDS



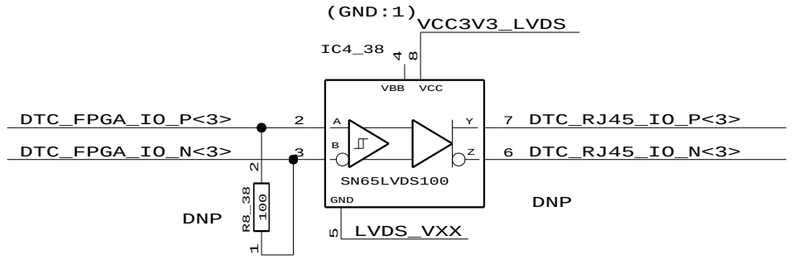
()
(GND:1)
VCC3V3_LVDS



()
(GND:1)
VCC3V3_LVDS

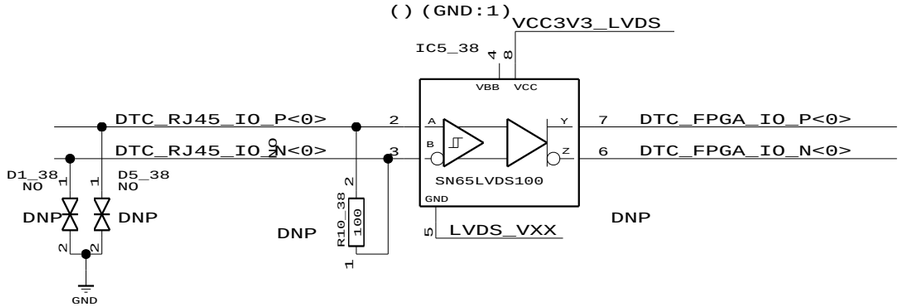


()
(GND:1)
VCC3V3_LVDS

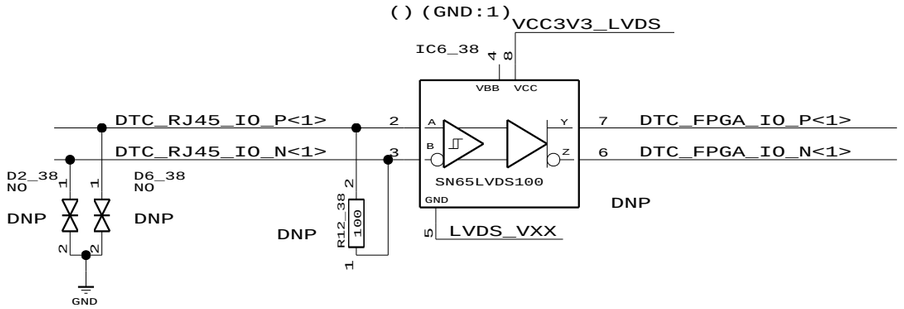


INPUTS

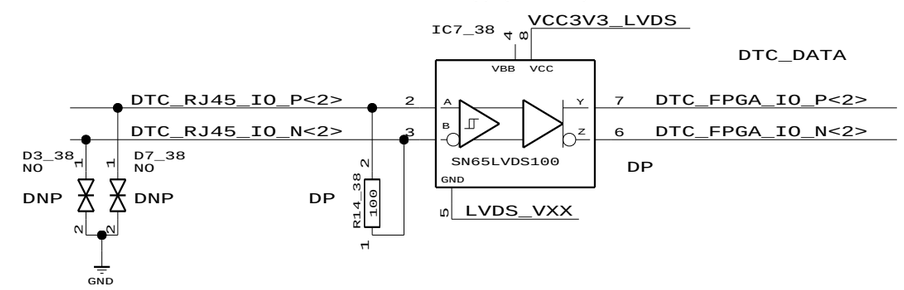
()(GND:1)
VCC3V3_LVDS



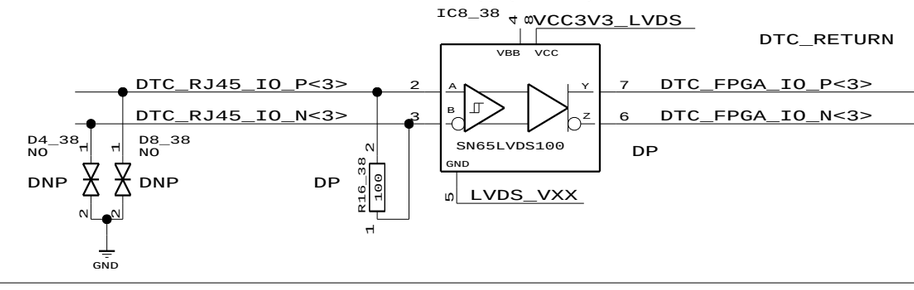
()(GND:1)
VCC3V3_LVDS



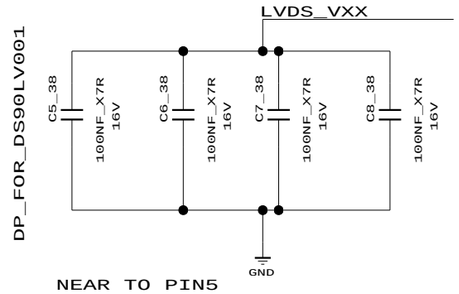
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VCC3V3_LVDS
DTC_DATA

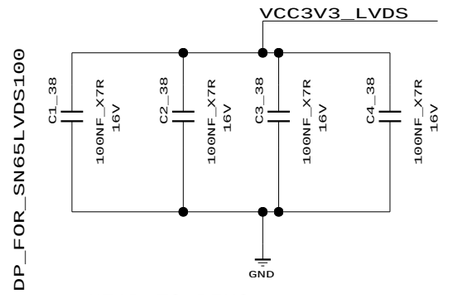


()(GND:1)
VCC3V3_LVDS
DTC_RETURN



LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA
IO DTC_FPGA_IO_P<3..0>
IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45
IO DTC_RJ45_IO_P<3..0>
IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

TE/MPE
CERN
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

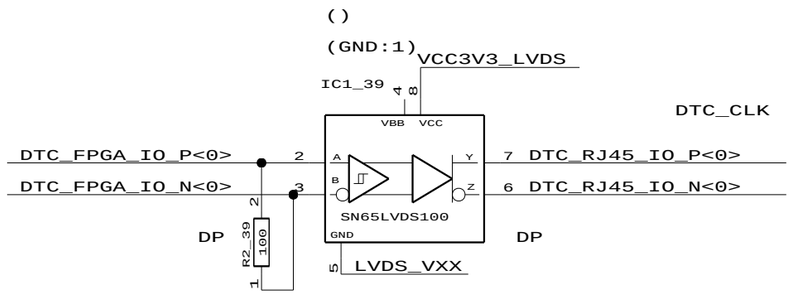
PROJECT:SRU v2.0

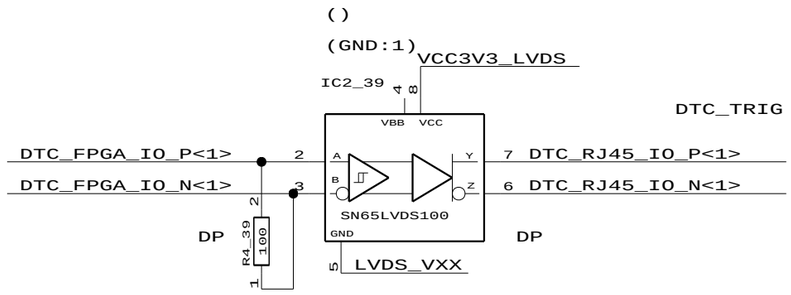
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 64/81

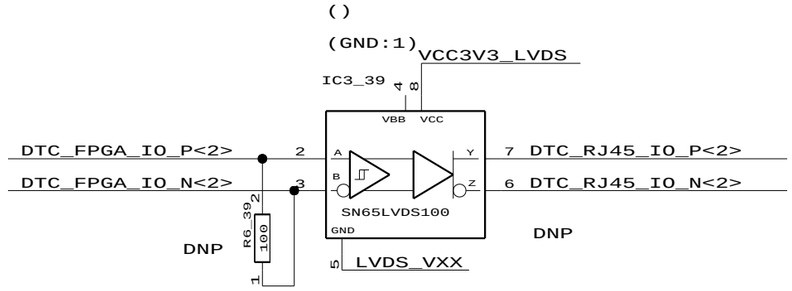
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

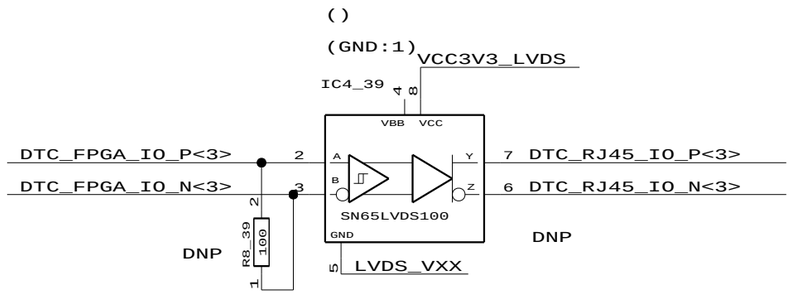
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

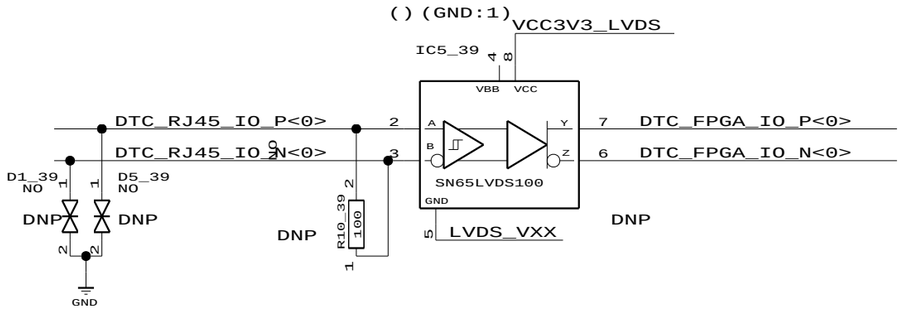


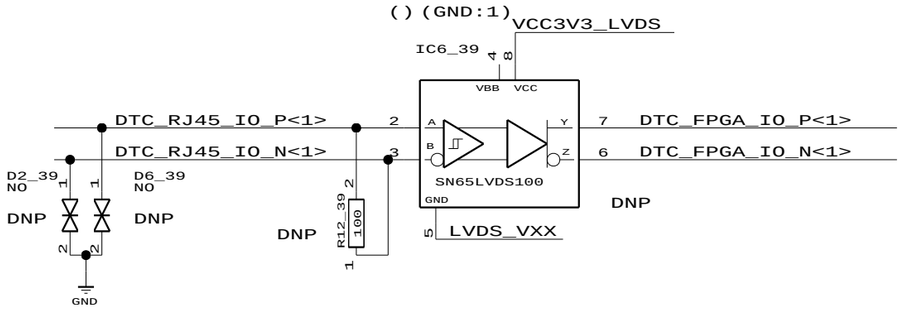


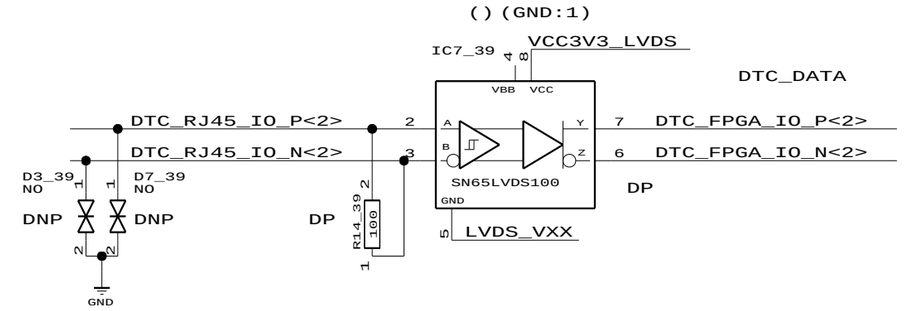


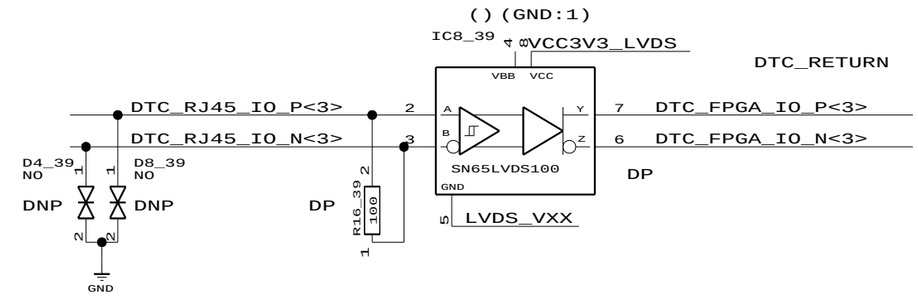


INPUTS

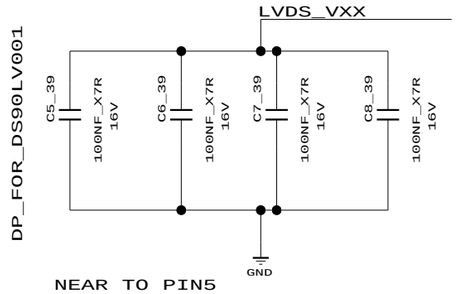


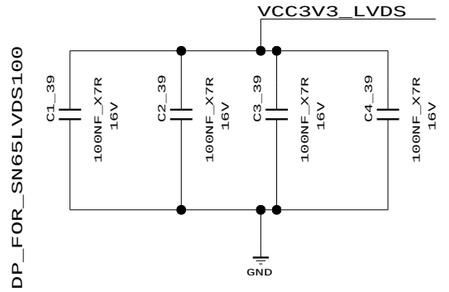






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

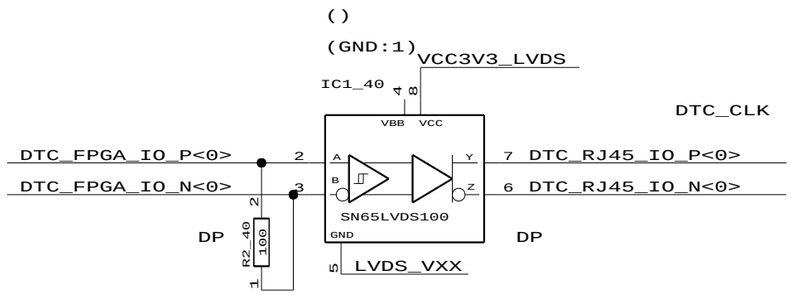
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

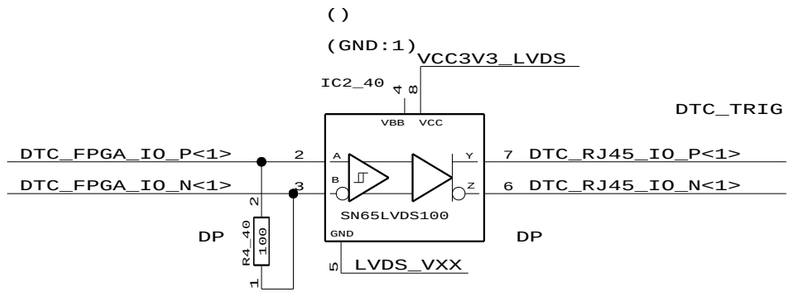
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 65/81

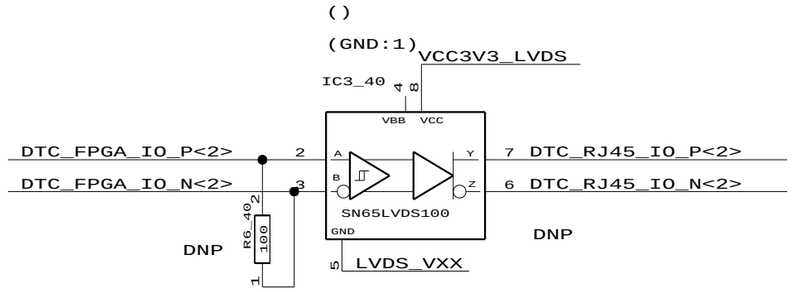
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

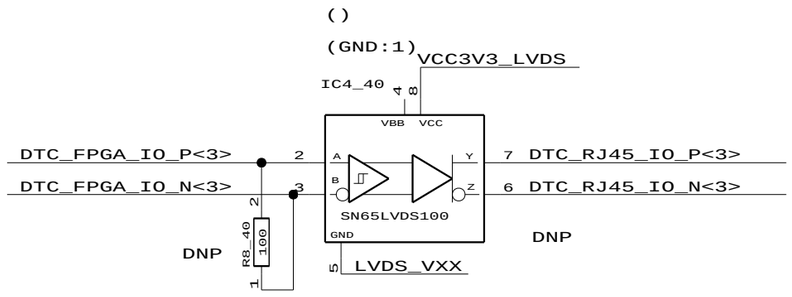
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

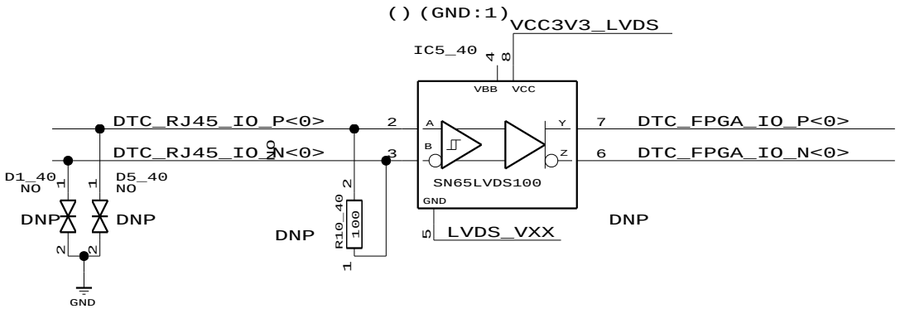


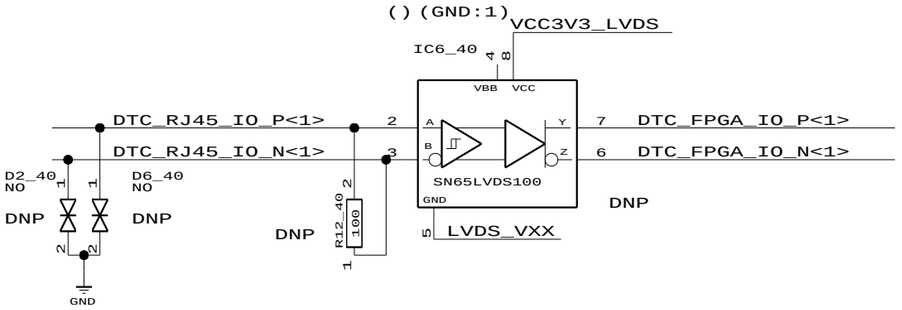


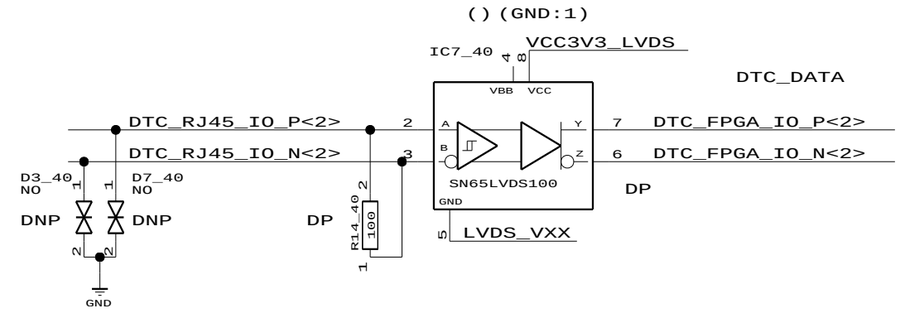


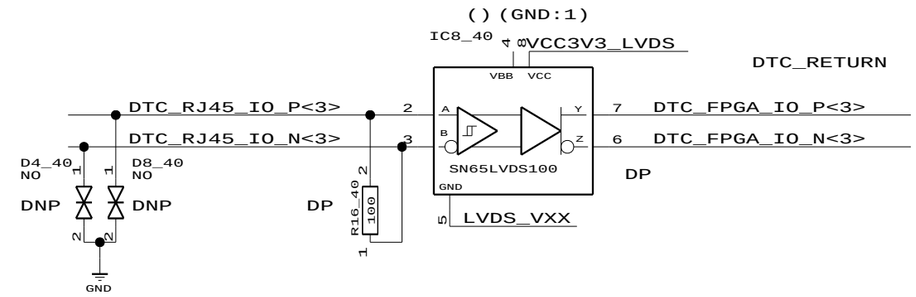


INPUTS

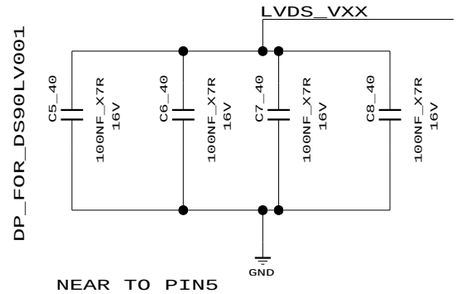


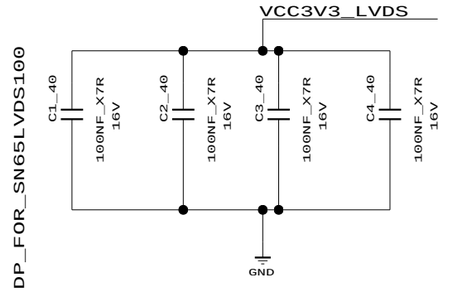






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

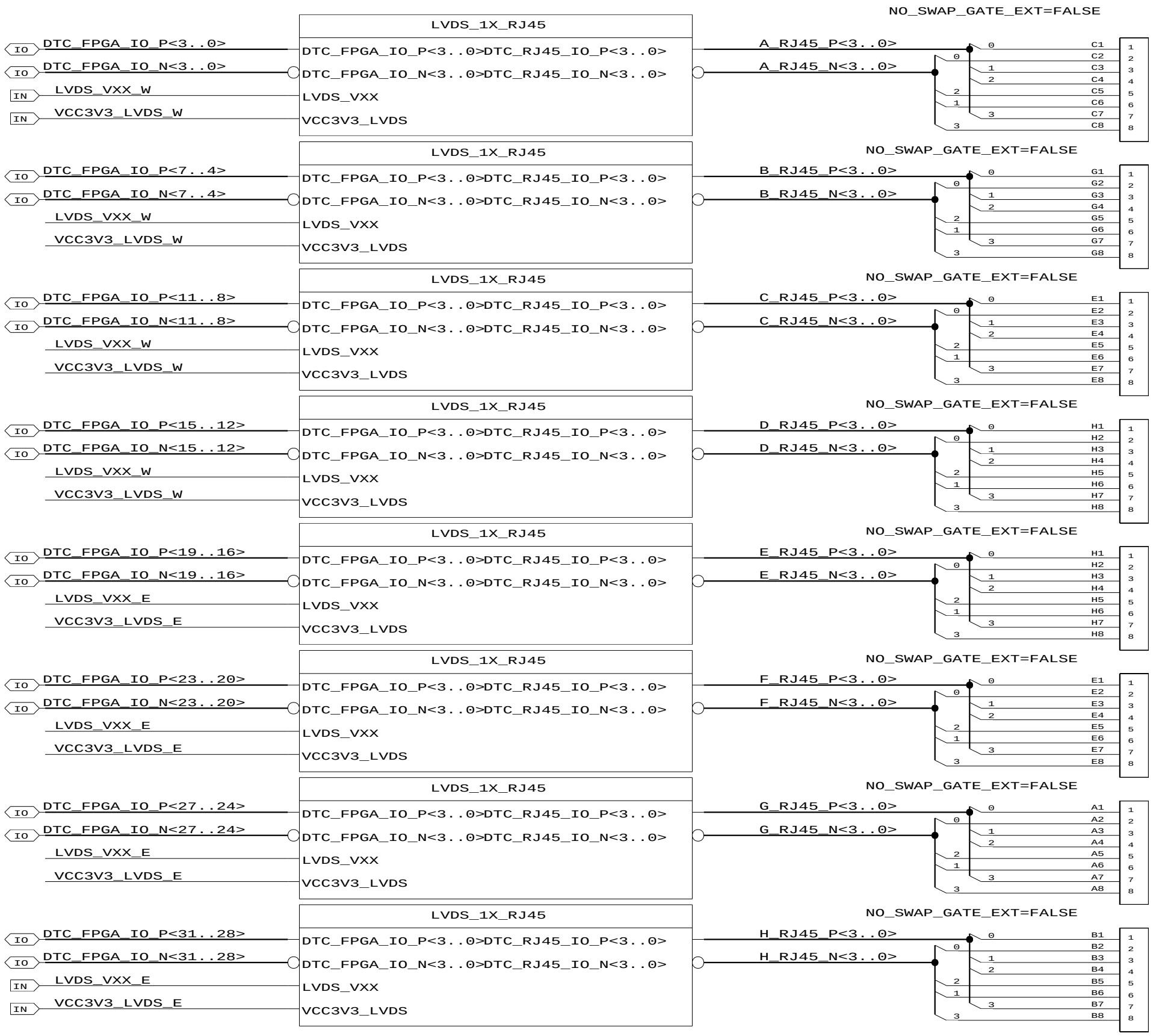
PROJECT:SRU v2.0

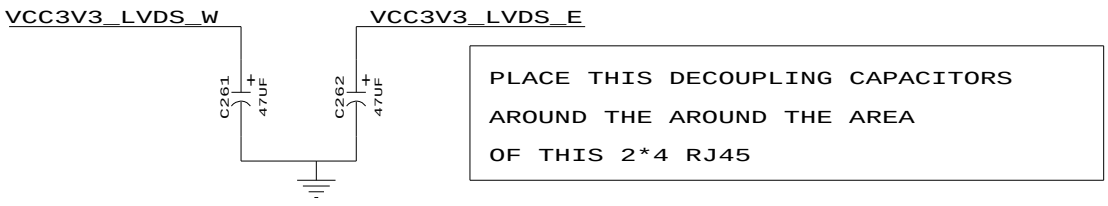
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 66/81

LAST_MODIFIED=Mon Dec 12 10:53:50 2011

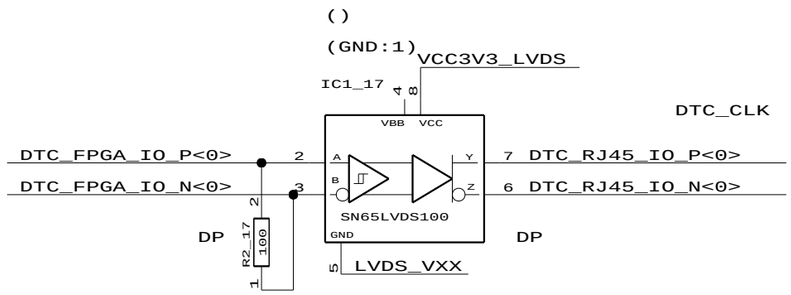
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

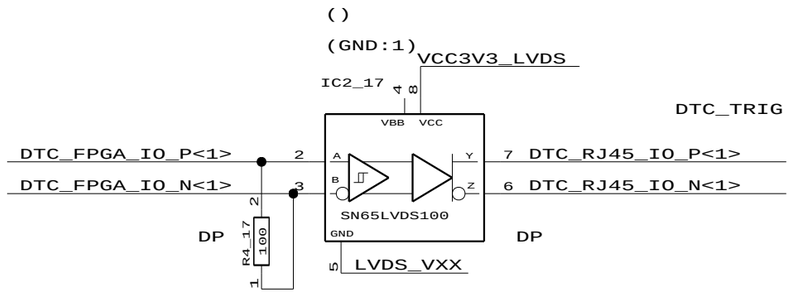


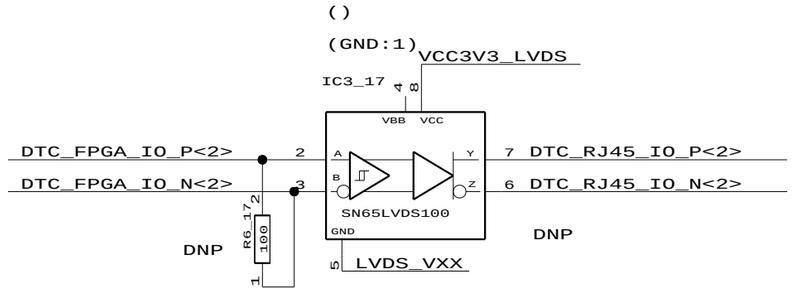


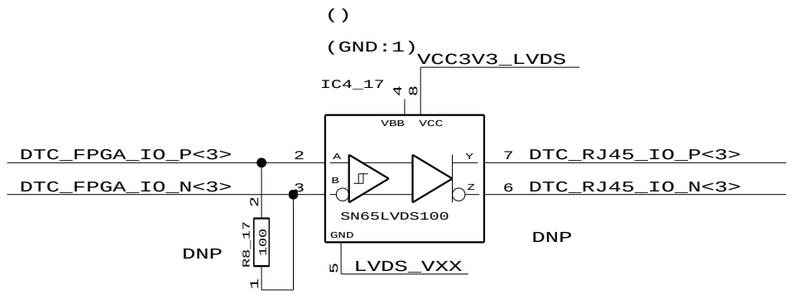
Project file:sru_rev2.cpm			SYSTEM:
European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND (TS/DEM)	PROJECT:SRU v2.0		
	MODULE:lvds_8x_rj45_mix	Sheet: Module: 1/1 Project: 67/81	
	LAST_MODIFIED=Fri Dec 09 11:01:54 2011		
	Design by: FZhang/SMartoiu	PCB by: EXT	DATE: 29/07/2010

OUTPUTS

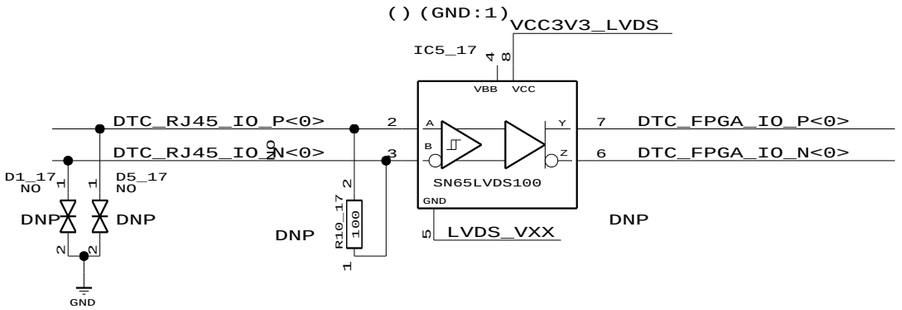


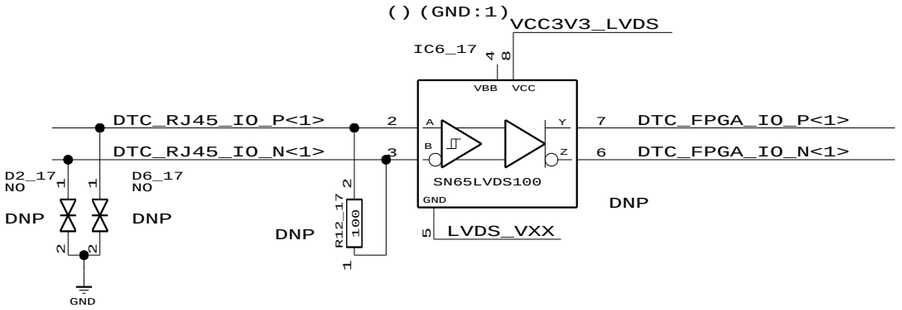


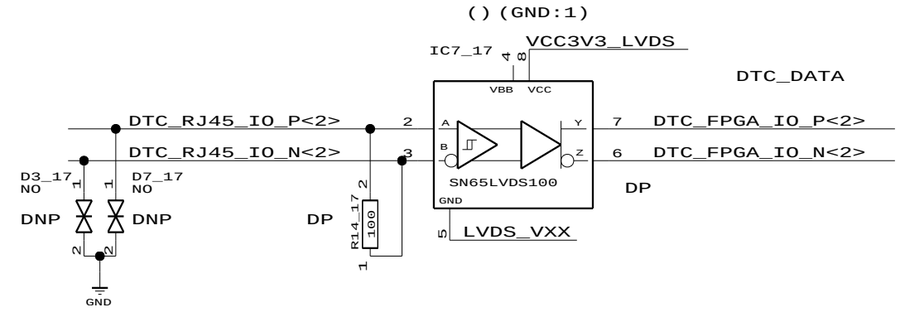


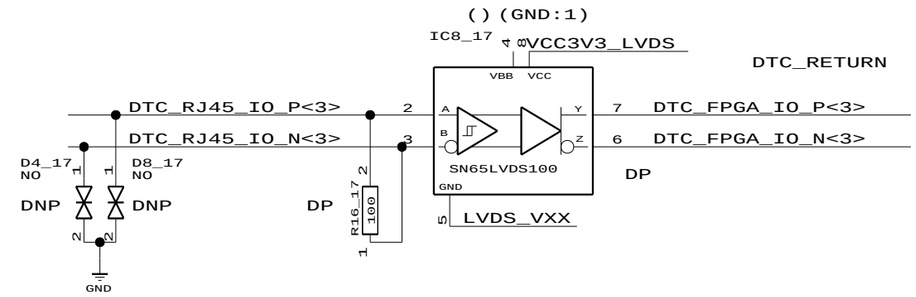


INPUTS

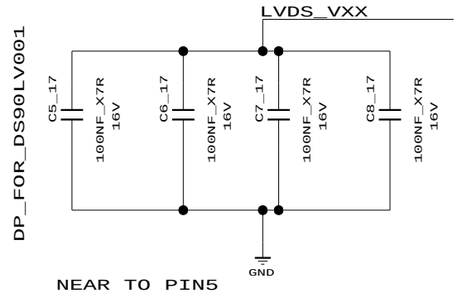


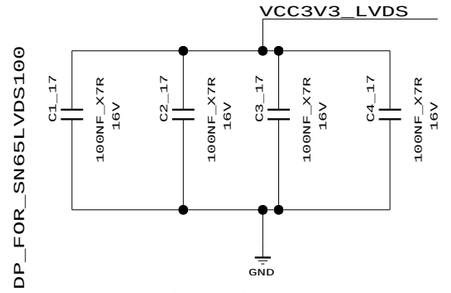






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

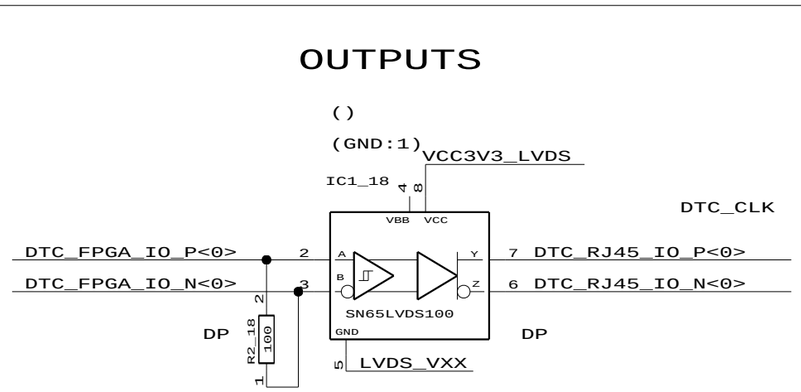
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

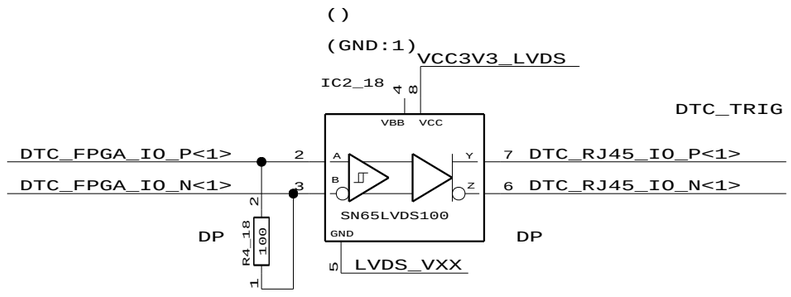
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 68/81

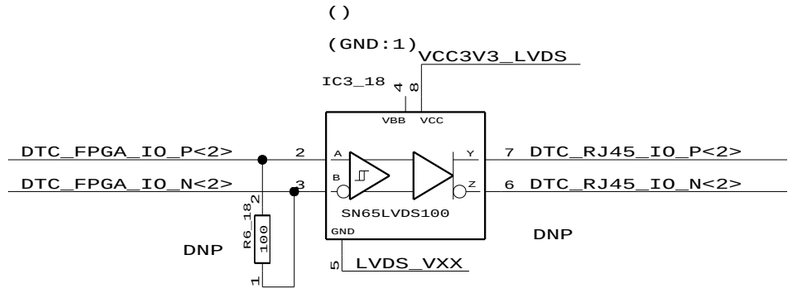
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

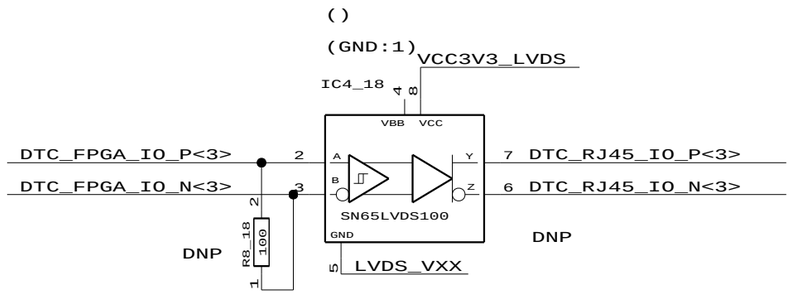
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

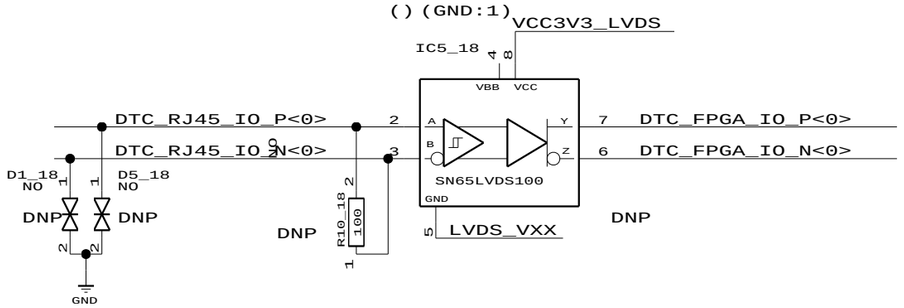


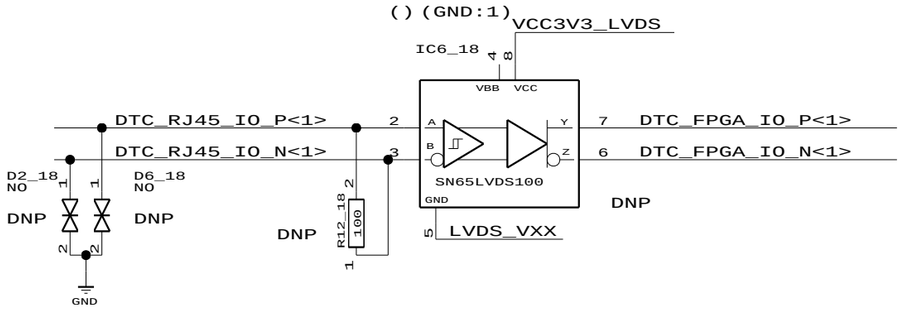


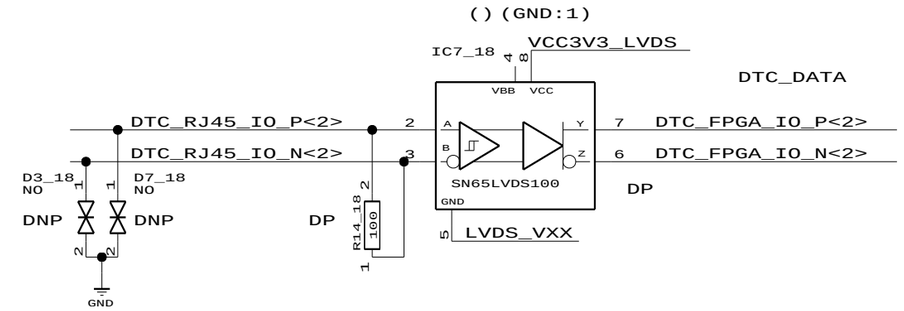


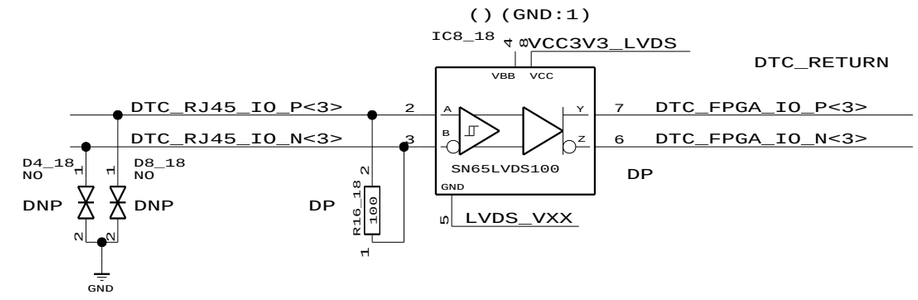


INPUTS

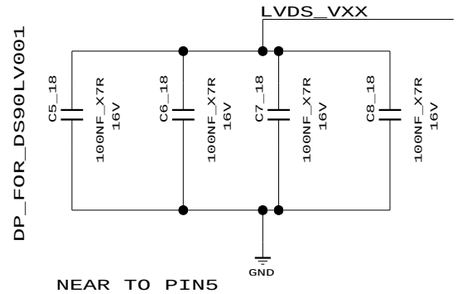


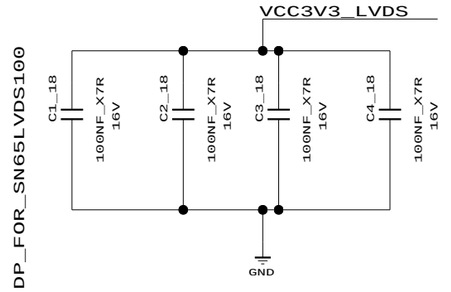






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

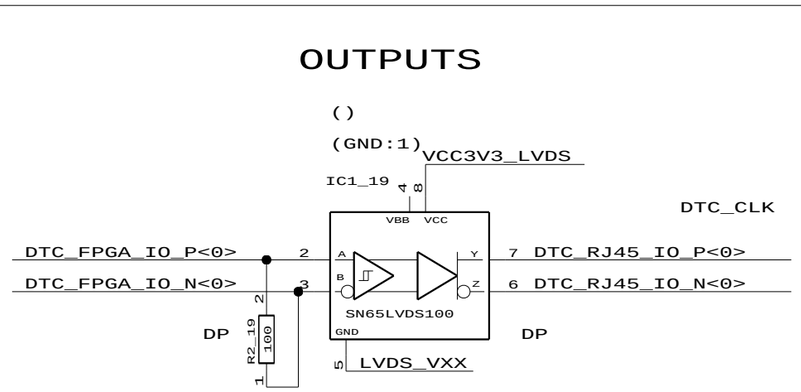
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

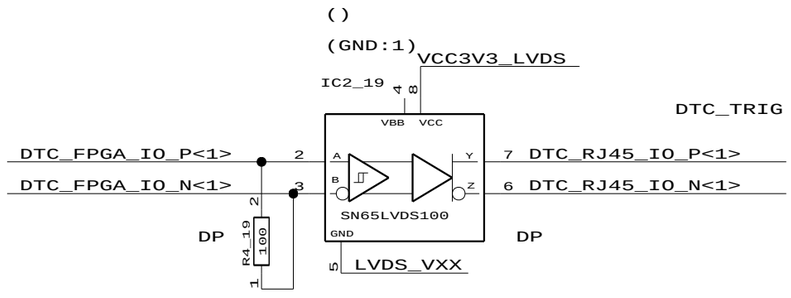
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 69/81

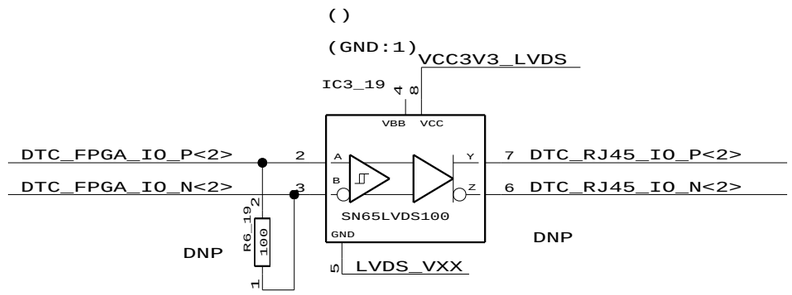
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

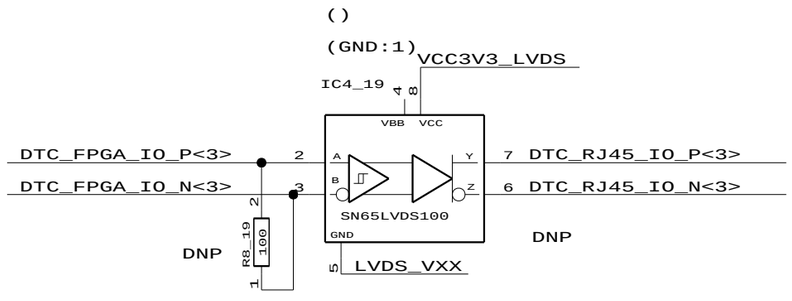
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

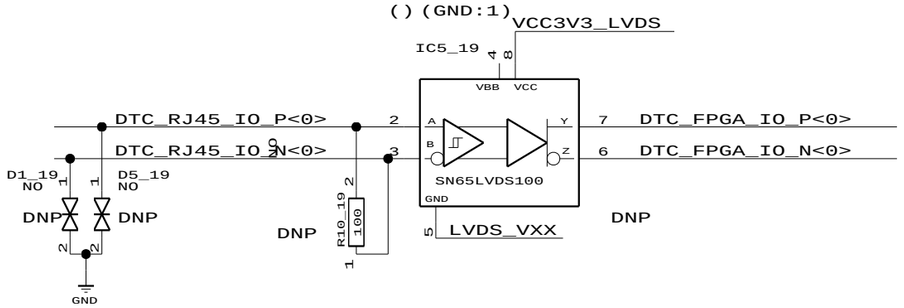


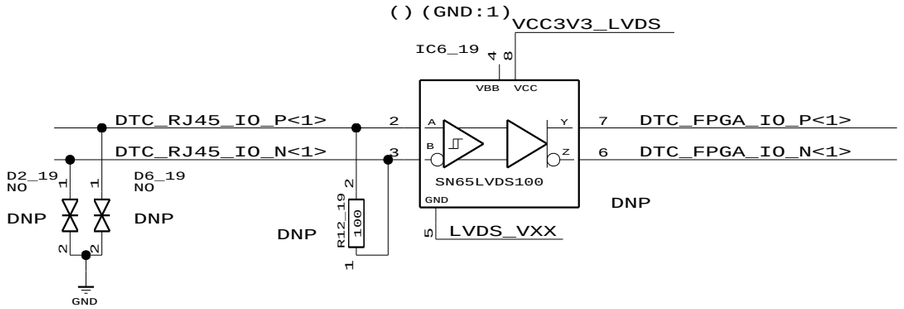


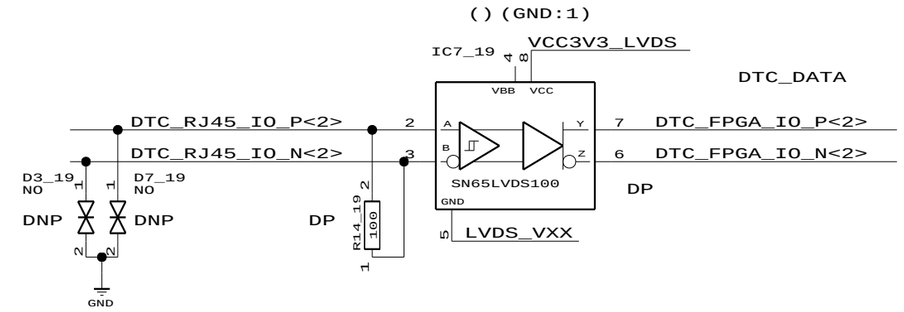


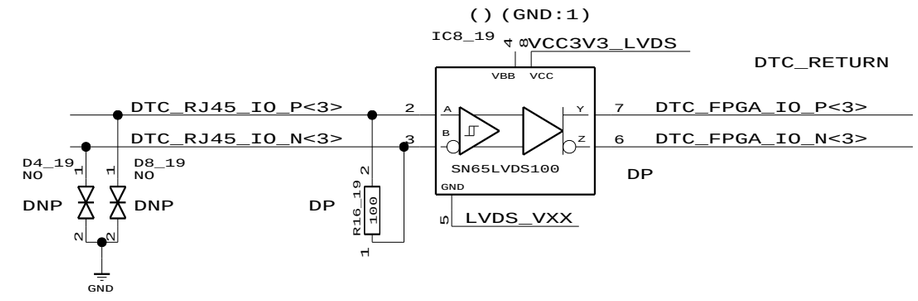


INPUTS

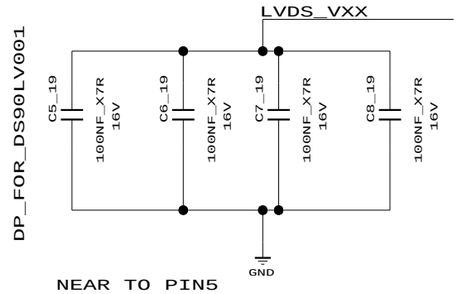


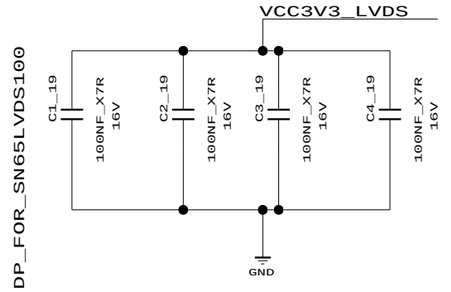






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

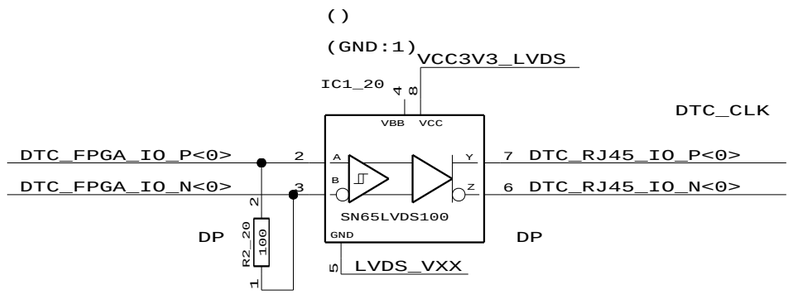
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

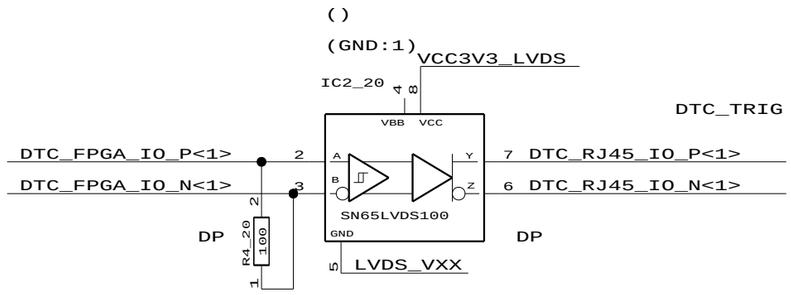
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 70/81

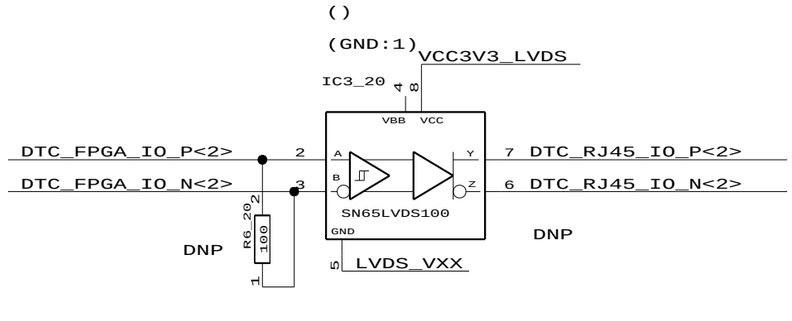
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

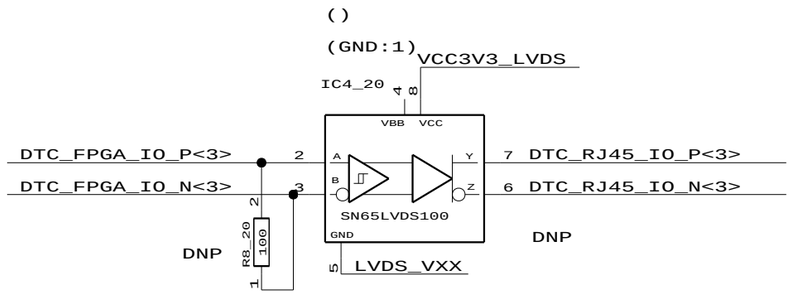
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

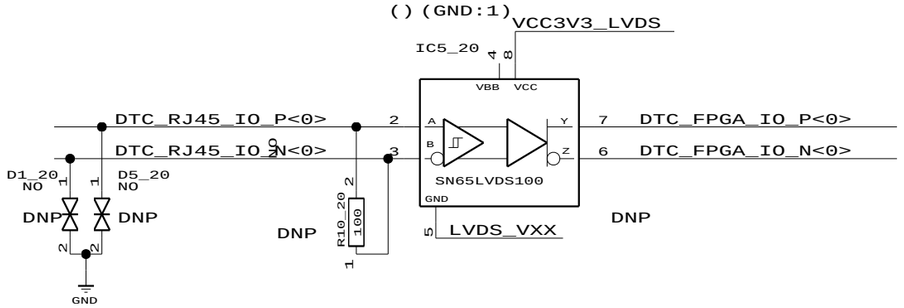


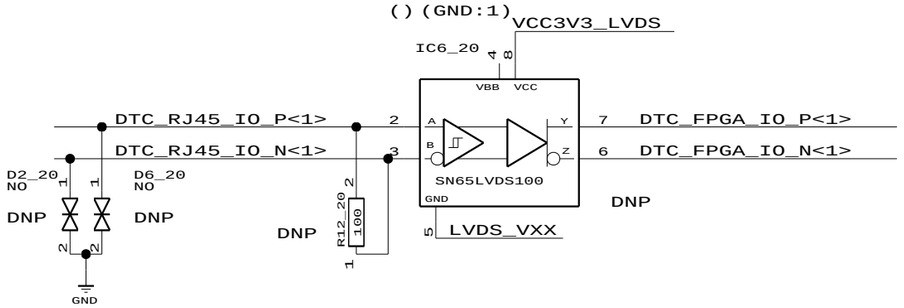


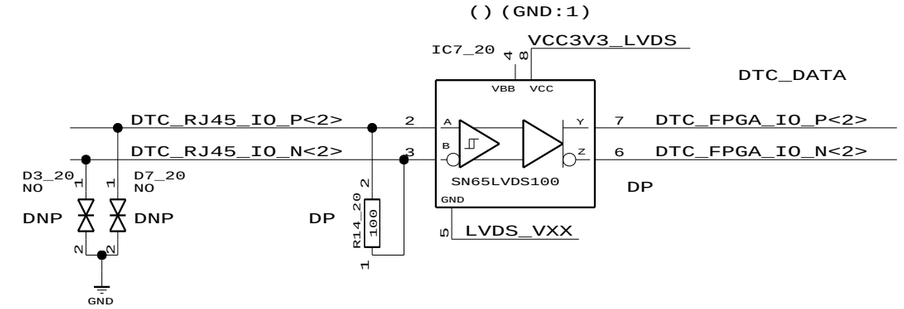


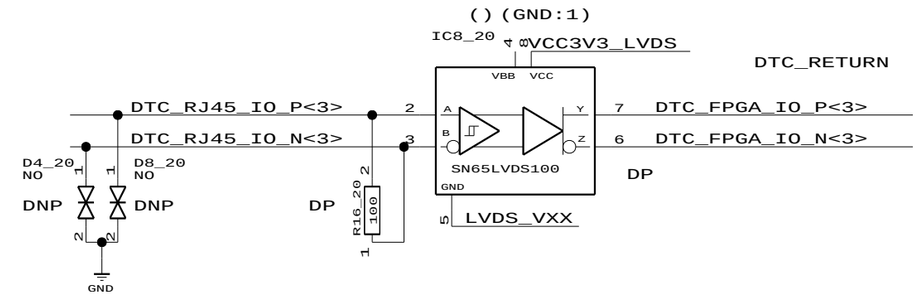


INPUTS

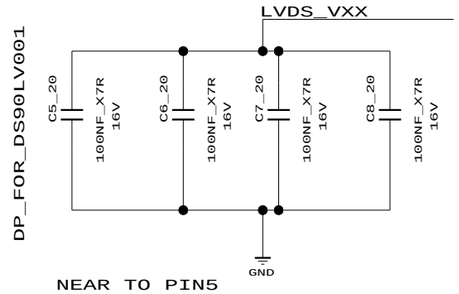


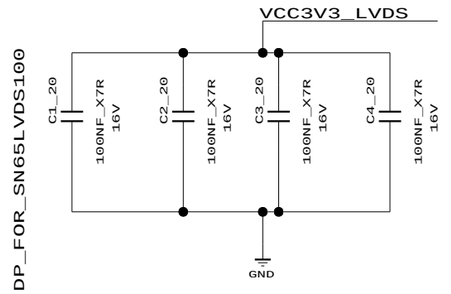






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

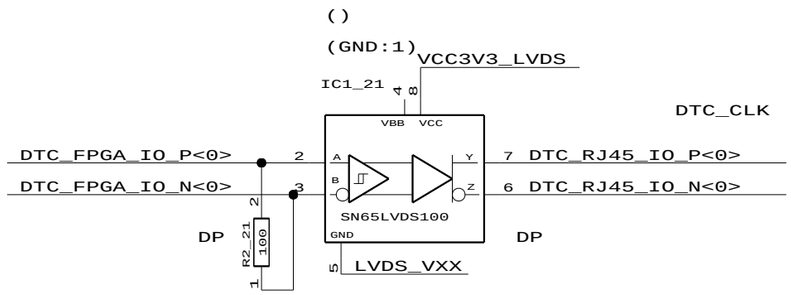
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

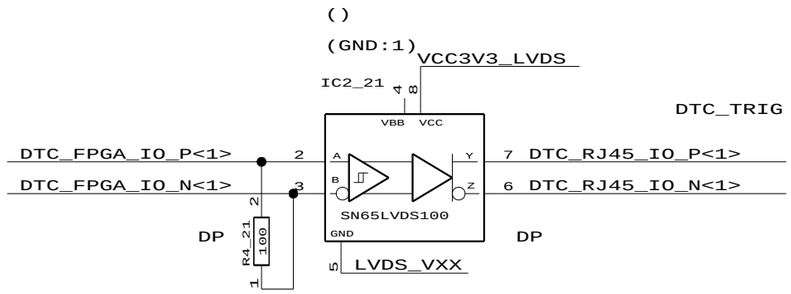
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 71/81

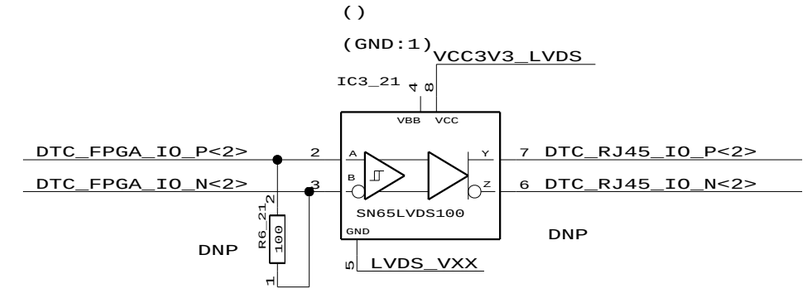
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

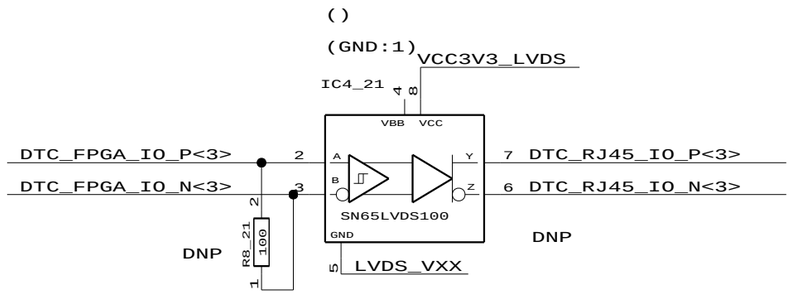
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

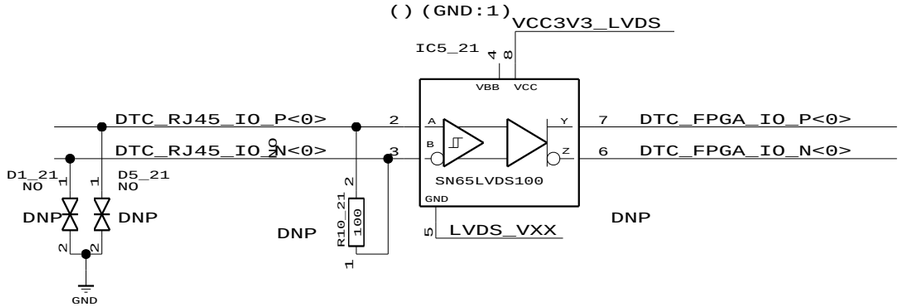


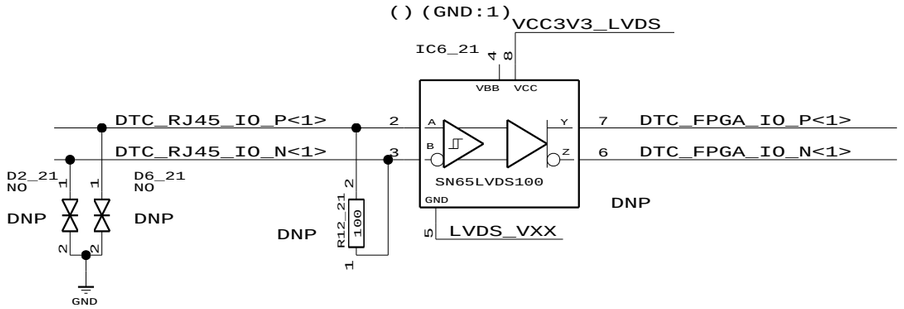


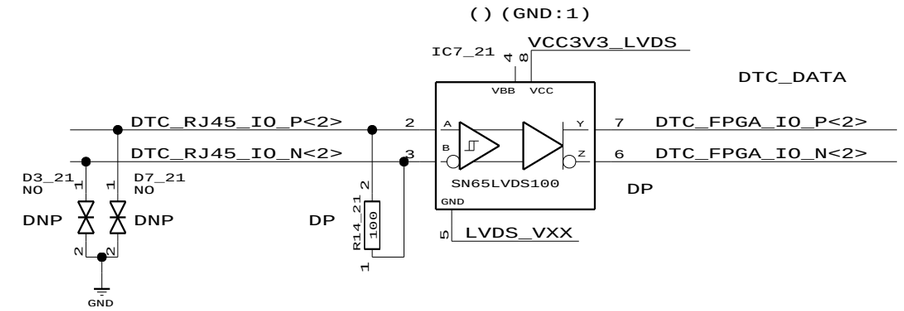


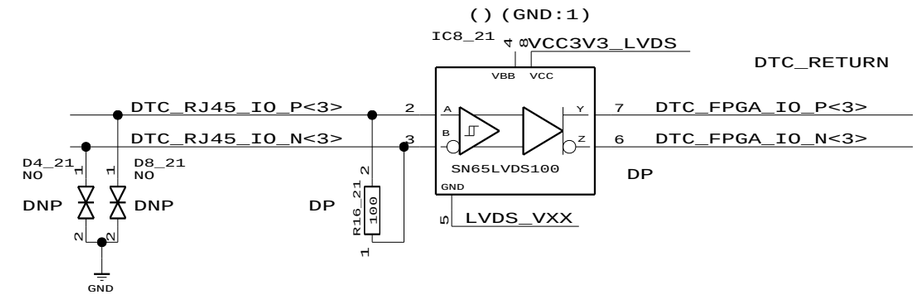


INPUTS

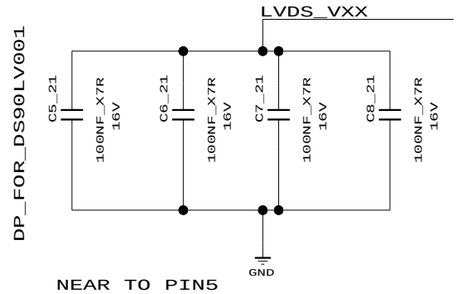


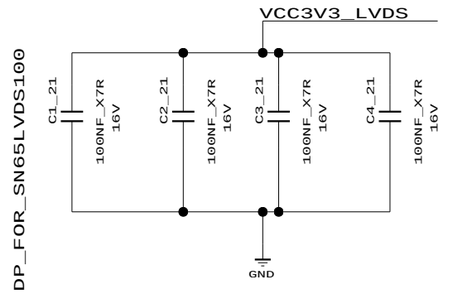






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

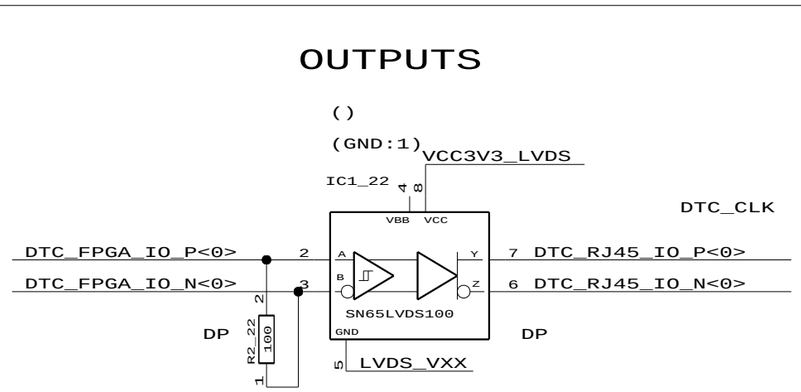
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

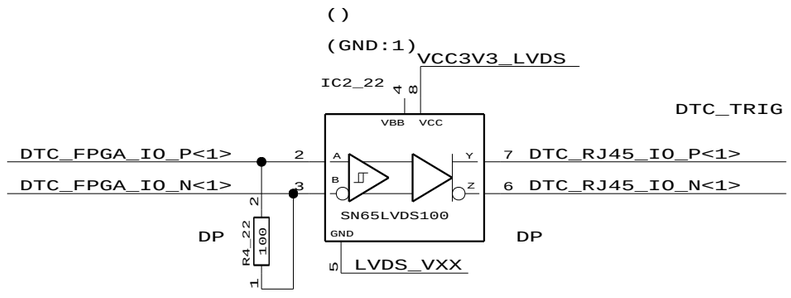
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 72/81

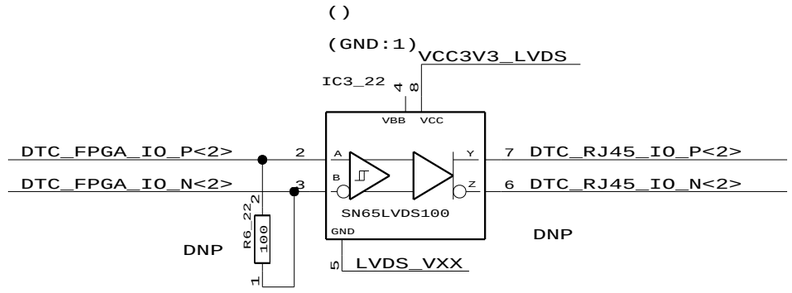
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

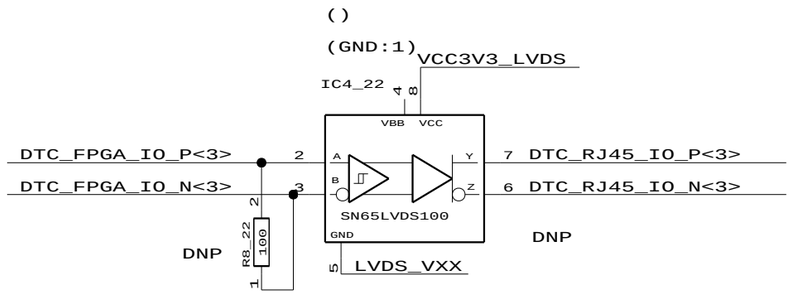
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

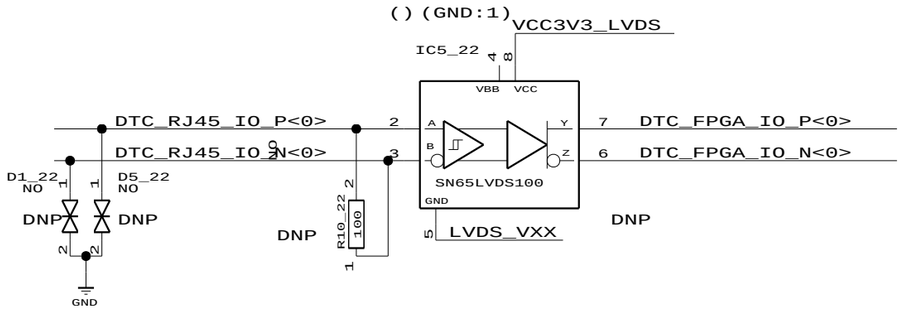


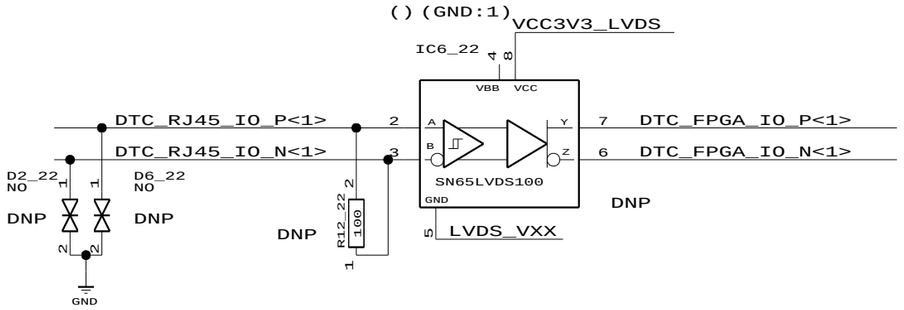


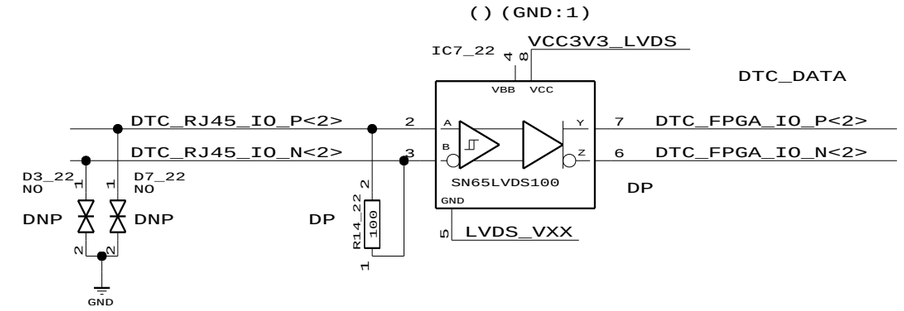


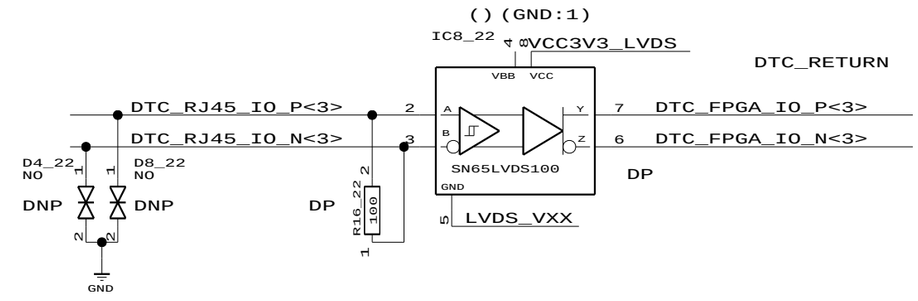


INPUTS

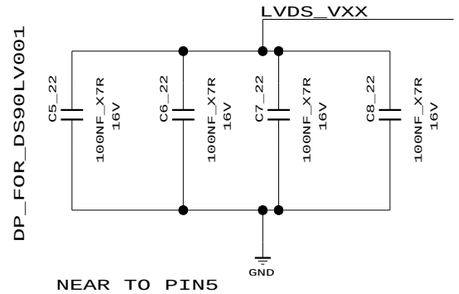


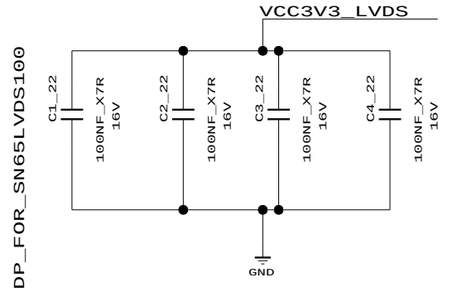






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

CERN TE/MPE European Organization for Nuclear Research 1211 GENEVA 23 SWITZERLAND

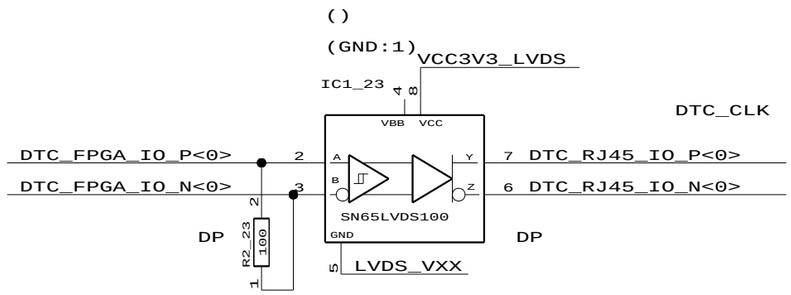
PROJECT:SRU v2.0

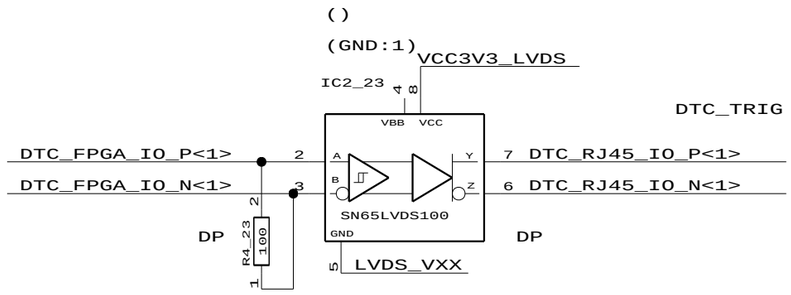
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 73/81

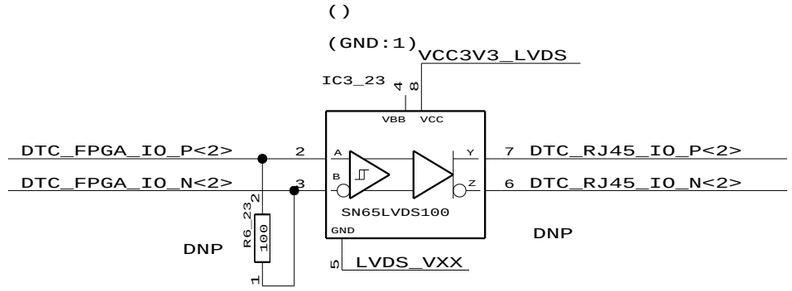
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

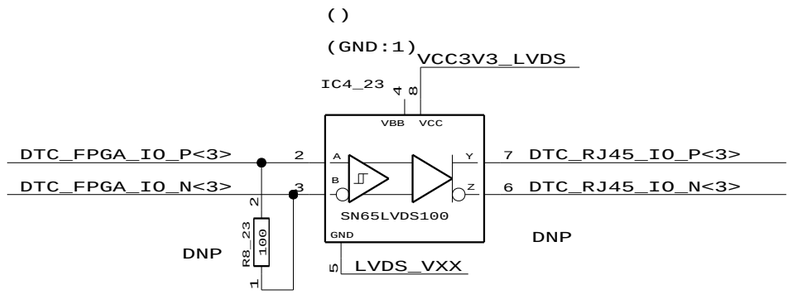
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

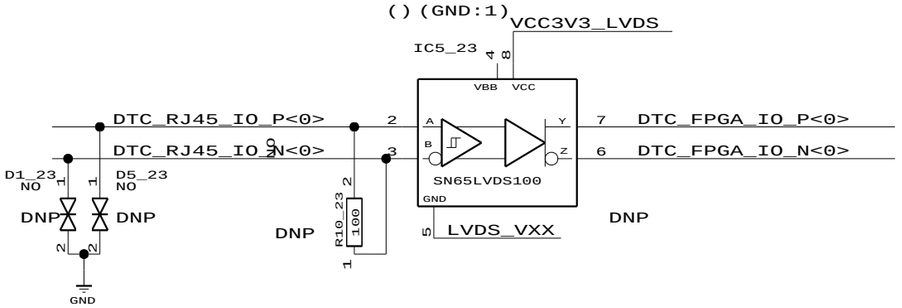


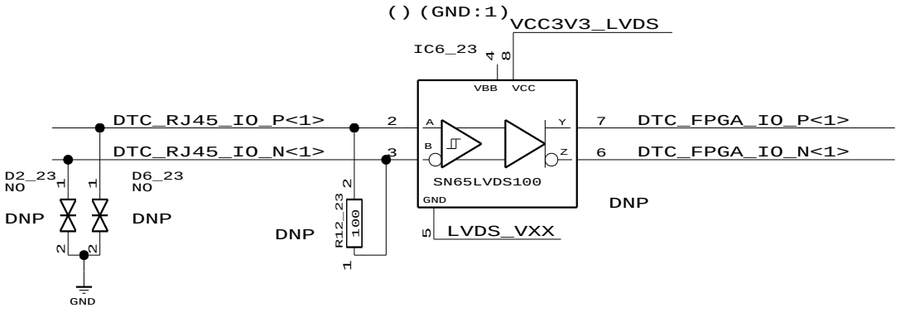


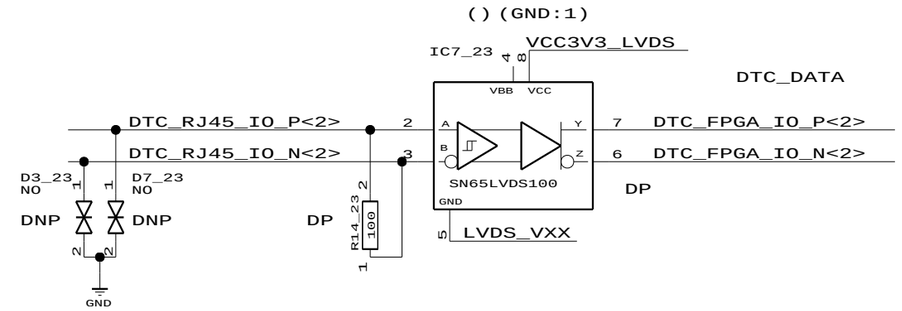


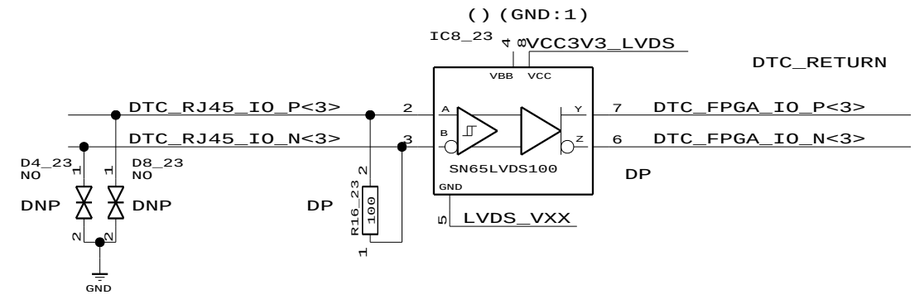


INPUTS

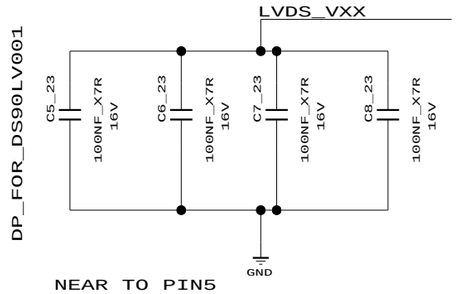


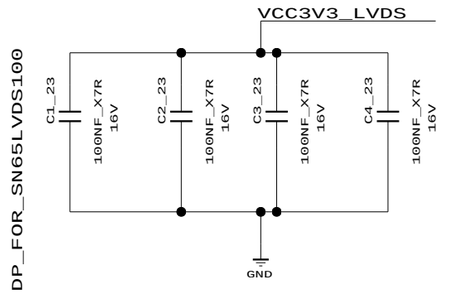






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

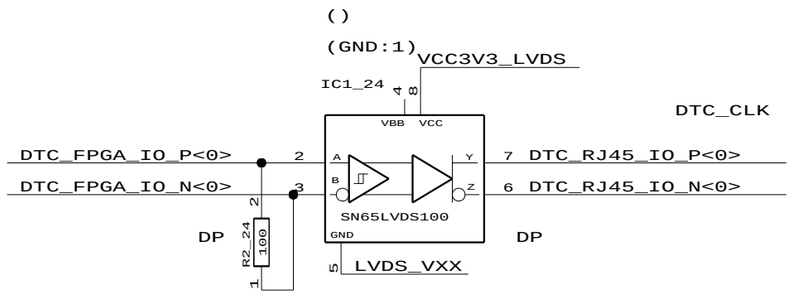
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

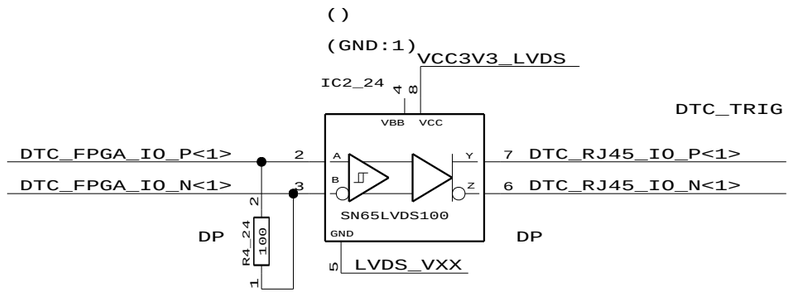
MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 74/81

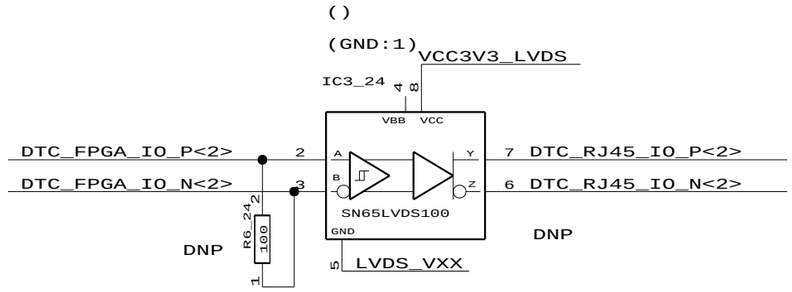
LAST_MODIFIED=Mon Dec 12 10:53:50 2011

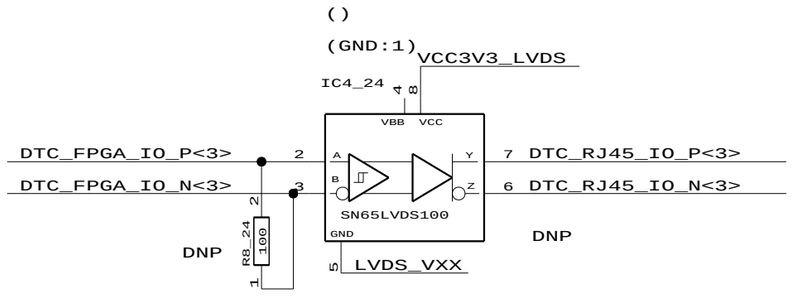
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

OUTPUTS

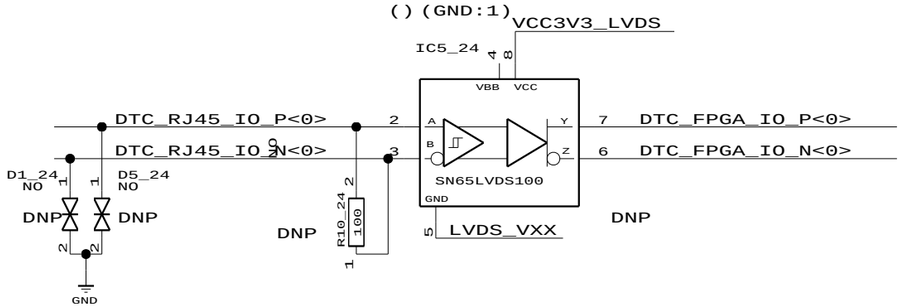


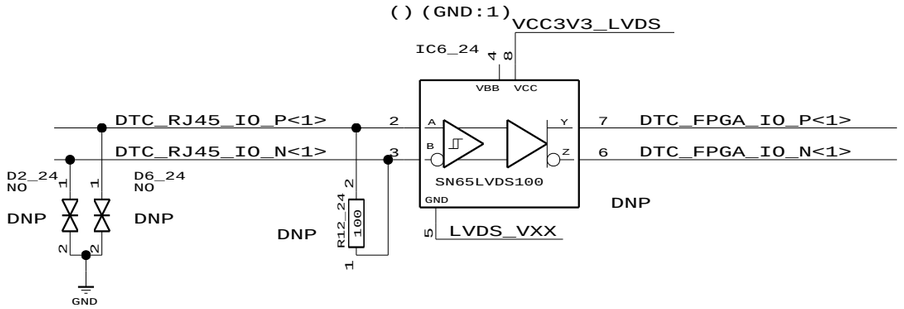


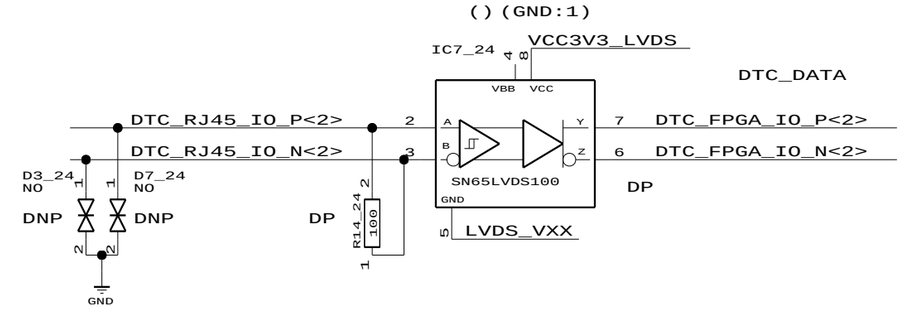


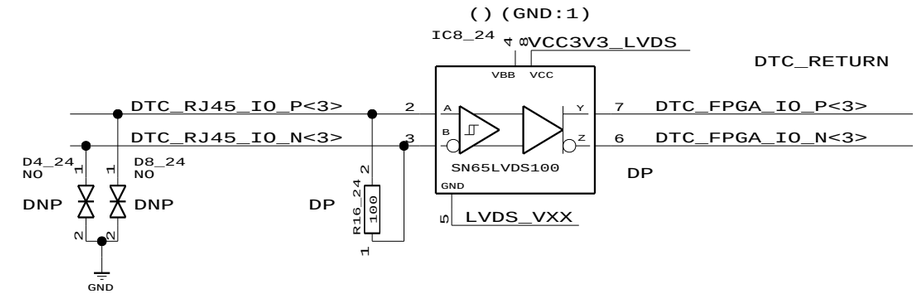


INPUTS

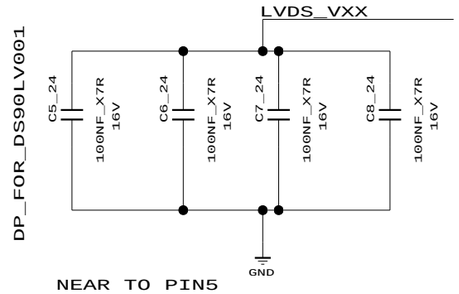


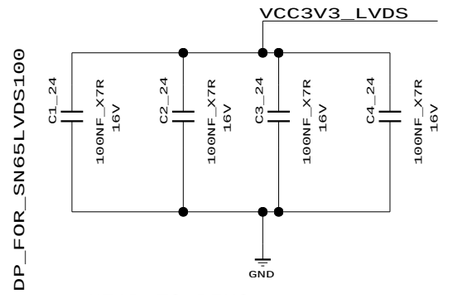






LOCAL DECOUPLING





IN LVDS_VXX

IN VCC3V3_LVDS

TO THE FPGA

IO DTC_FPGA_IO_P<3..0>

IO DTC_FPGA_IO_N<3..0>

TO CONN RJ45

IO DTC_RJ45_IO_P<3..0>

IO DTC_RJ45_IO_N<3..0>

Project file:sru_rev2.cpm SYSTEM:

PROJECT:SRU v2.0

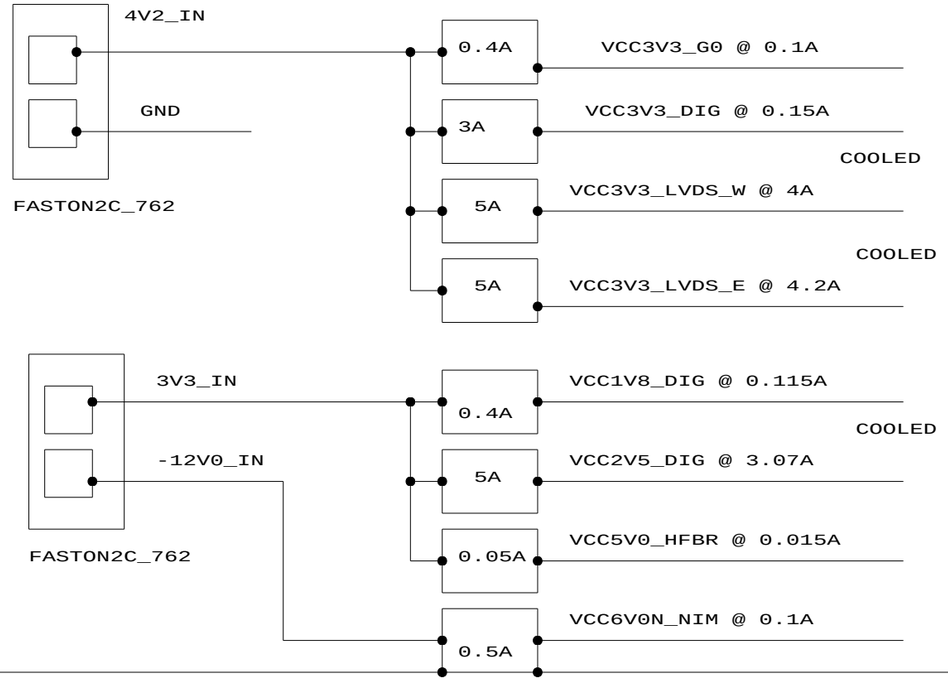
European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

MODULE:lvds_1x_rj45 Sheet: 1/1 Module: 1/1 Project: 75/81

LAST_MODIFIED=Mon Dec 12 10:53:50 2011

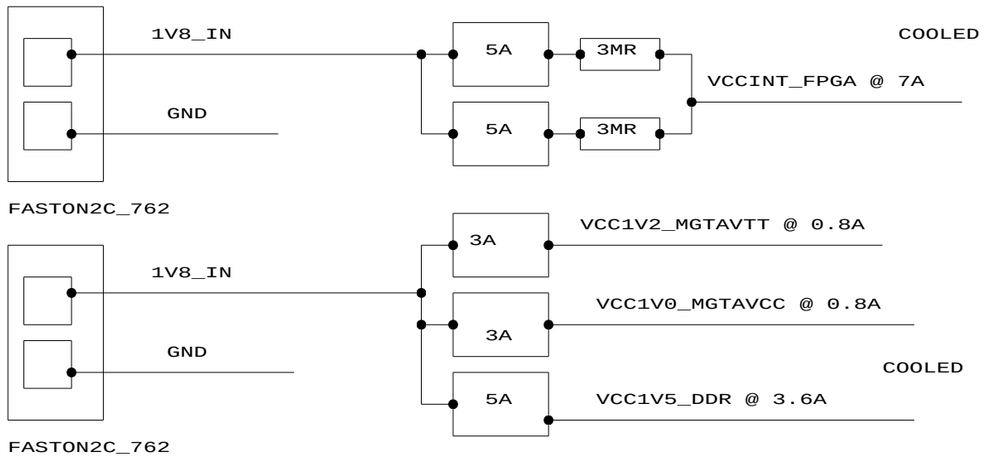
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

Note:
4 high current LDO below
heatsink 10 Watt
on right side of SRU



	10BGE PHY	TTC/GP PLL	
1.5A 4 X SFP	0.3A	0.5A	2.5A
	0.3A (SYNCETH PLL)		3.4A

0 MS (POWER ON)	VCC3V3_G0 @ 0.1A
10.8 MS (2 LDO START)	VCCINT_FPGA @ 7A VCC1V8_DIG @ 0.115A
20.4MS	VCC2V5_DIG @ 3.07A
30MS	VCC1V5_DDR @ 3.6A VCC1V2_MGTAVTT @ 0.8A VCC1V0_MGTAVCC @ 0.8A VCC3V3_DIG @ 0.15A VCC3V3_LVDS_W @ 4A VCC3V3_LVDS_E @ 4.2A VCC5V0_HFBR @ 0.015A VCC6V0N_NIM @ 0.1A
40.8MS	FPGA_PROGRAM_B (CONFIG START)
15S	CONFIG_MODE_CHG_B (PROM KEPT RESET CONFIG MODE CHANGED. NOW IS BPI_UP MODE)



0.6A	1.4A

Note:
3 high current LDO below
heatsink 7 Watt
on left side of SRU

Project file:sru_rev2.cpm

SYSTEM:

TE/MPE
CERN
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

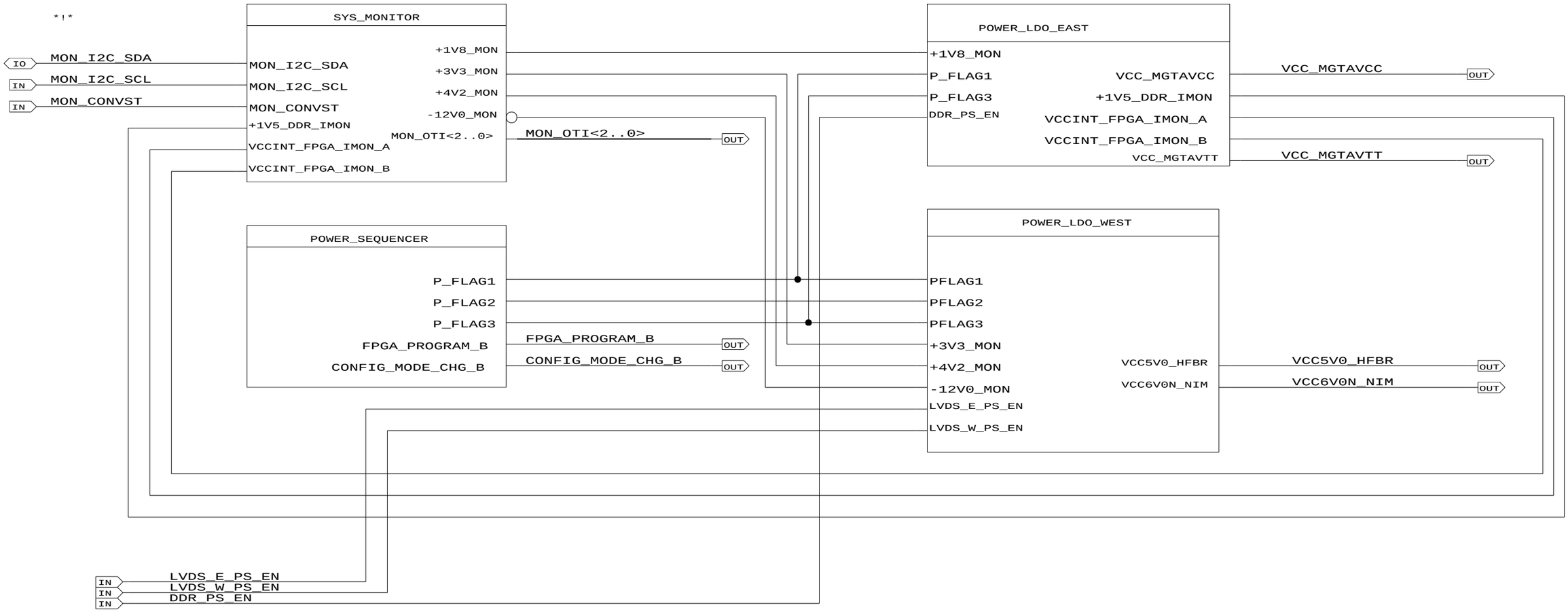
PROJECT:SRU v2.0

MODULE:power_supplies

Sheet: 1/2 (Module: / Project: 76/81)

LAST_MODIFIED=Mon Oct 10 16:50:27 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010



Project file:sru_rev2.cpm

SYSTEM:

European Organization
for Nuclear Research
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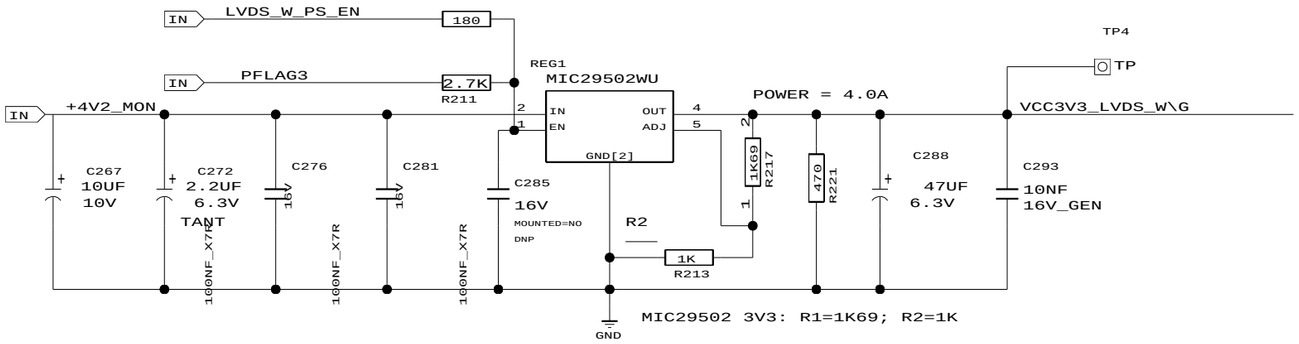
PROJECT:SRU v2.0

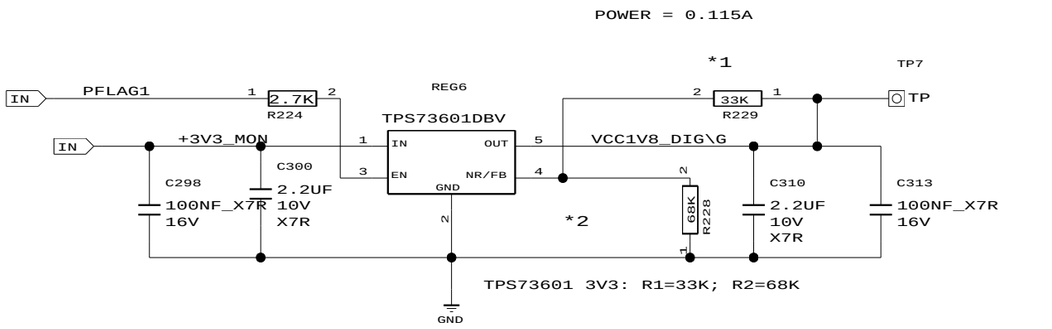
MODULE:power_supplies

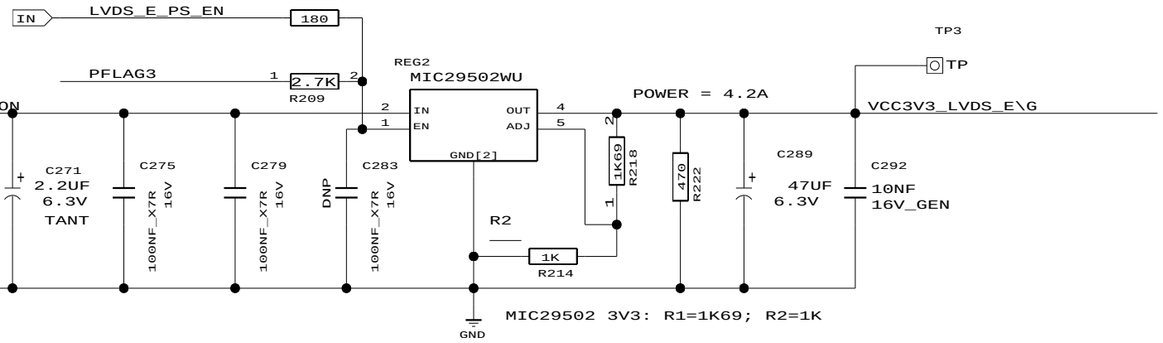
Sheet: 2/2 Module: Project: 77/81

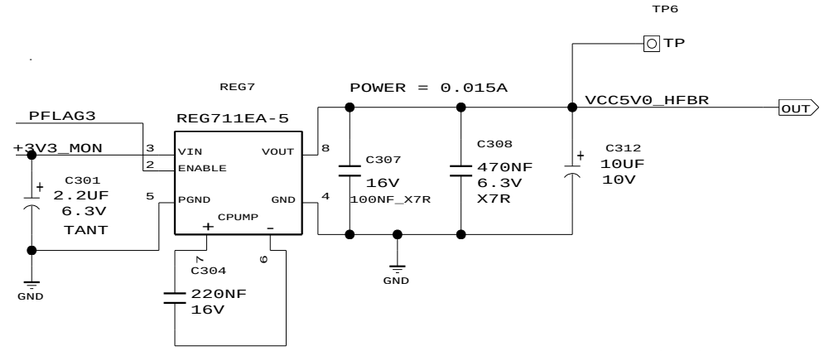
LAST_MODIFIED=Thu Dec 08 16:30:23 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

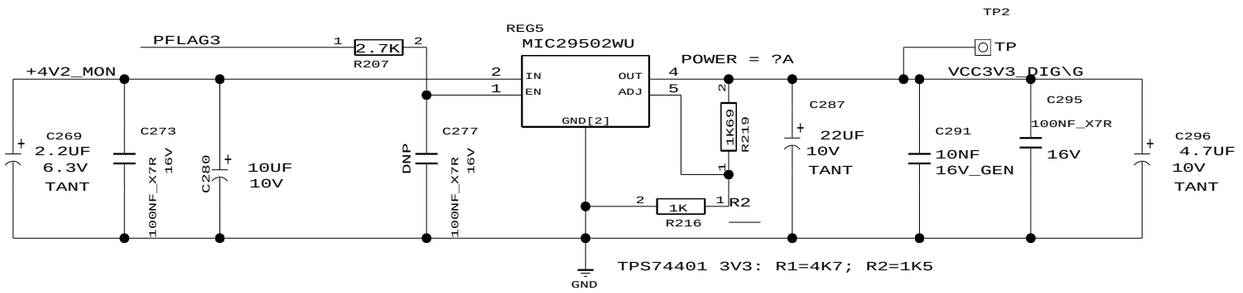


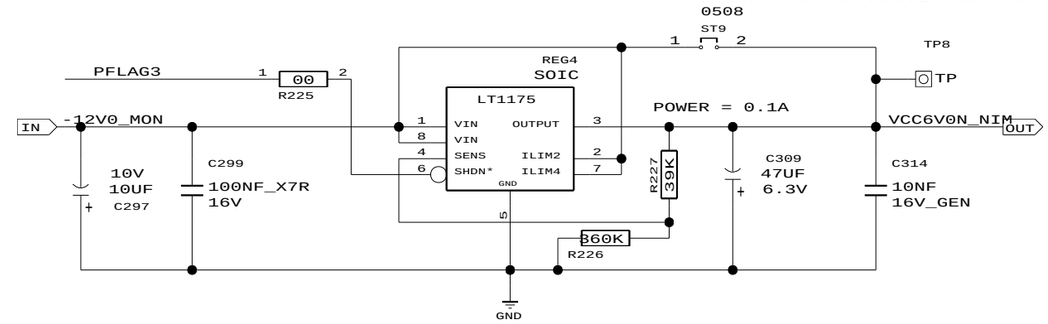


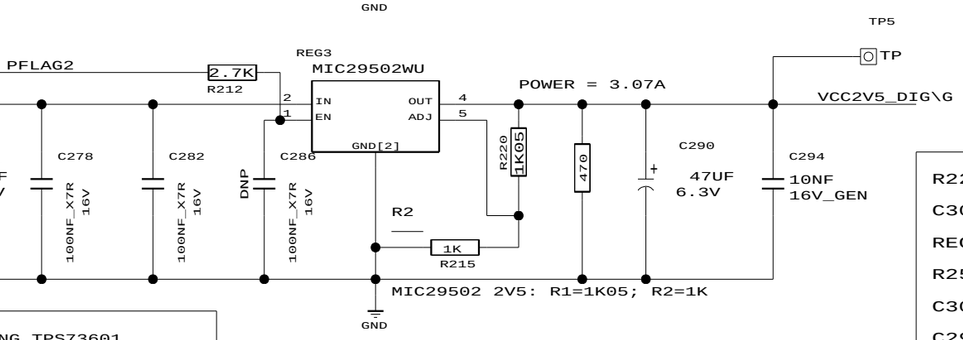


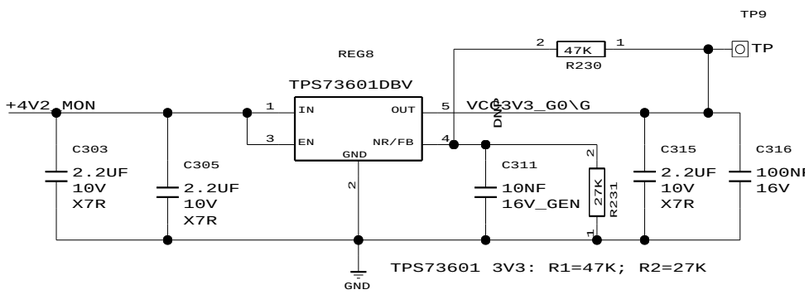


*3









NOTE:
FOR CALCULATING TPS73601
OUTPUT VOLTAGE USE
R1 = R2(VOUT/1.204 - 1)

R1/R2 = 19K FOR BEST ACCURACY

Note:
Trace large current power line
with low impedance,wide and
thick copper

NOTE:
FOR CALCULATING TPS74401
OUTPUT VOLTAGE USE
R1 = R2(VOUT/0.8 - 1)

NOTE:
FOR CALCULATING MIC29502
OUTPUT VOLTAGE USE
R1 = R2(VOUT/1.240 - 1)

R229 CHANGED TO 33K
C306 REMOVED
REG5.6 -> VCC5V0_HFBR
R255 -> 0R
C302 REMOVED
C297 POLARITY INVERTED

Project file:sru_rev2.cpm SYSTEM:

TE/MPE

European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

PROJECT:SRU v2.0

MODULE:power_ldo_west | Sheet: 1/1 | Module: 1/1 | Project: 78/81

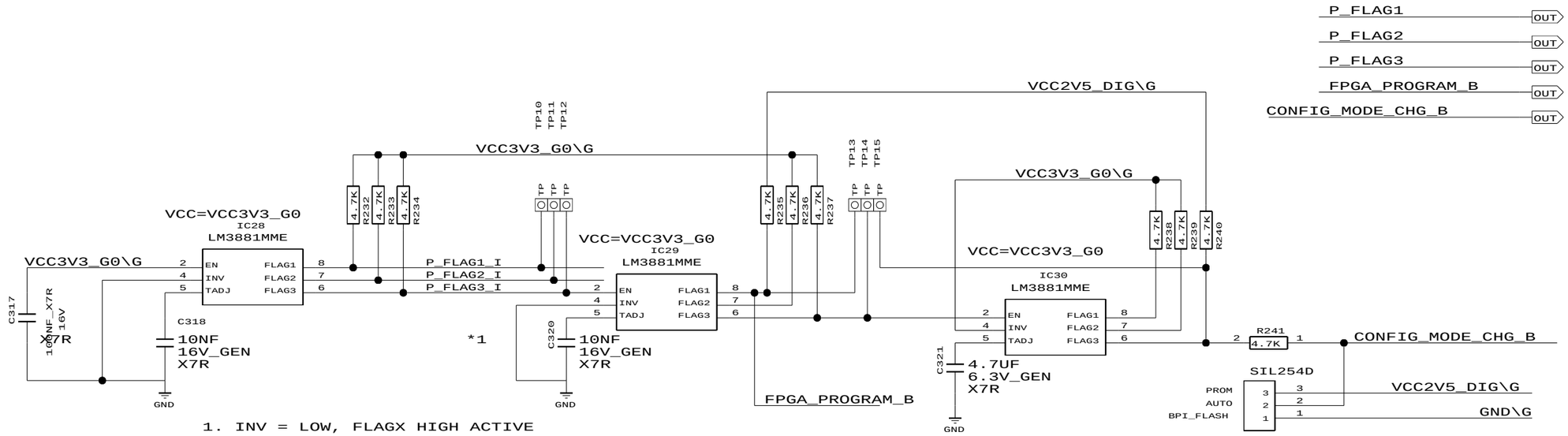
LAST_MODIFIED=Fri Dec 09 11:01:56 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

LM3881 SUPPLY CURRENT: 110UA MAXIMUM

C319 REMOVED

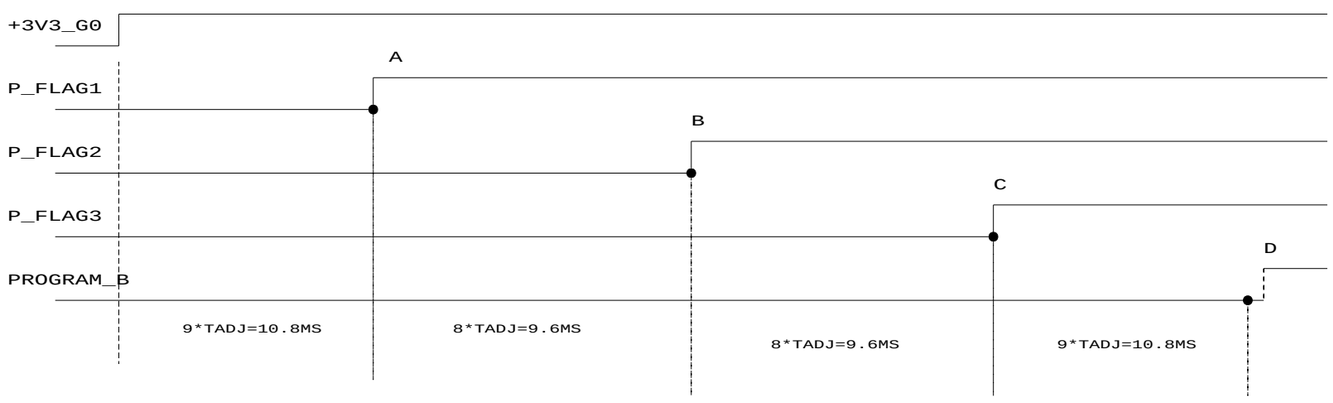
ADDED S/T BUFFERS ON PFLAGS



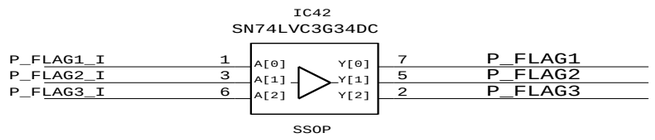
1. INV = LOW, FLAGX HIGH ACTIVE
2. C = 10NF, TADJ = 1.2MS

1. INV = HIGH, FLAGX LOW ACTIVE
2. C = 4.7UF, TADJ =0.55 S

POWER ON SEQUENCE TIMING



VCC=VCC3V3_G0 *!*



Project file:sru_rev2.cpm SYSTEM:

European Organization for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

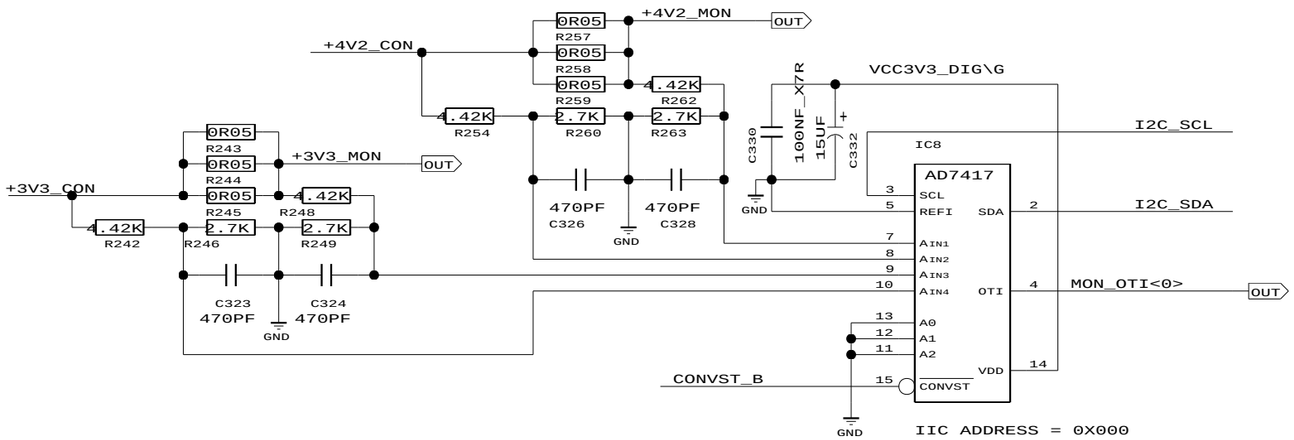
PROJECT:SRU v2.0

MODULE:power_sequencer Sheet: 1/1 Module: 1/1 Project: 79/81

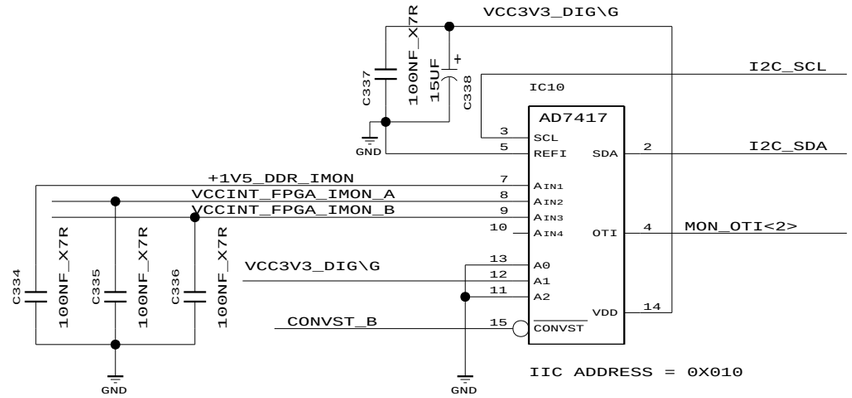
LAST_MODIFIED=Fri Dec 09 11:01:57 2011

Design by: FZhang/SMartoiu PCB by: EXT DATE: 29/07/2010

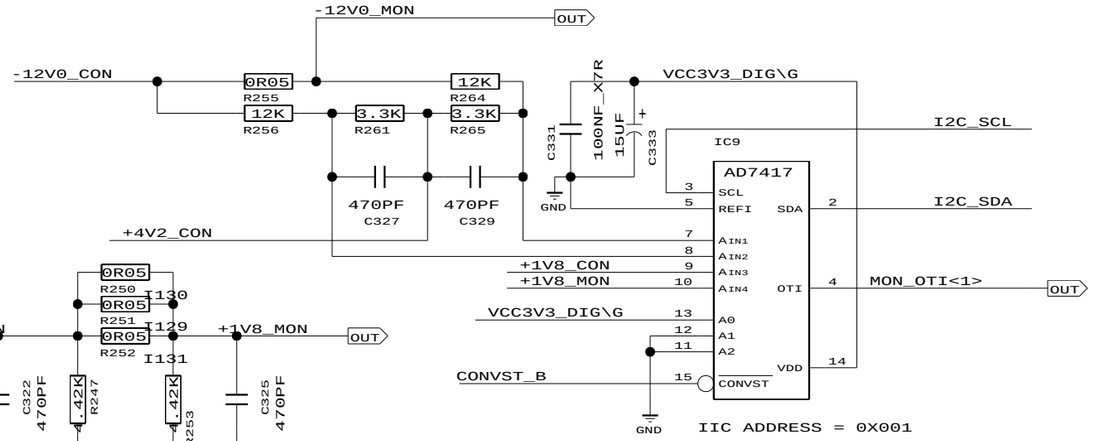
ADD 1000UF CAP ON 4.2V



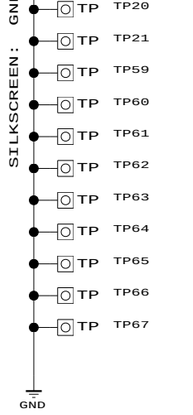
IIC ADDRESS = 0X000

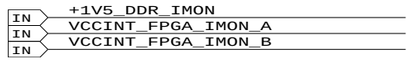


IIC ADDRESS = 0X010

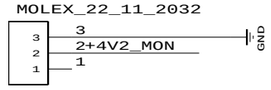


IIC ADDRESS = 0X001





FAN CONNECTOR

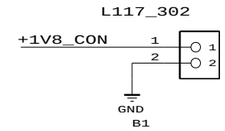


NOTE:

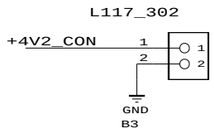
DISTRIBUTE GND TP

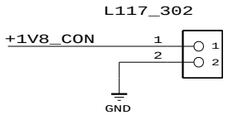
THROUGHOUT THE PCB

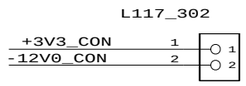
B2

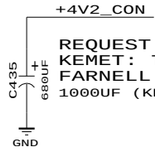


B4

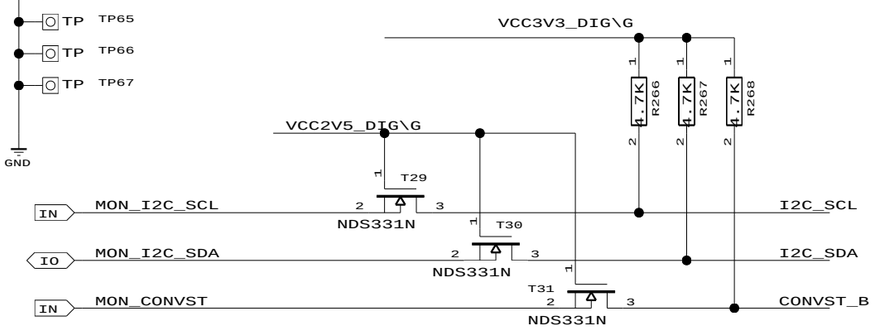








REQUEST 1000UF VERSION
KEMET: T495X108K006ZT E100
FARNELL : 1679288
1000UF (KEMET) T495X108K006ZT E100 (FARNELL 1679288)



NOTE:

LOW IMPEDANCE, WIDE AND THICK COPPER TRACE

FOR POWER SIGNALS WITH LARGE CURRENT

Project file:sru_rev2.cpm SYSTEM:

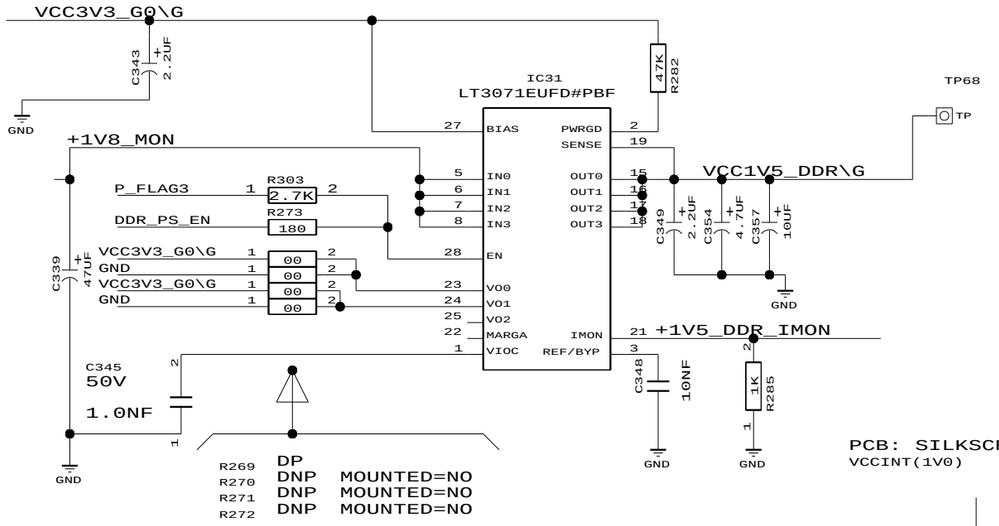
PROJECT:SRU v2.0

MODULE:sys_monitor Sheet: 1/1 Module: 1/1 Project: 80/81

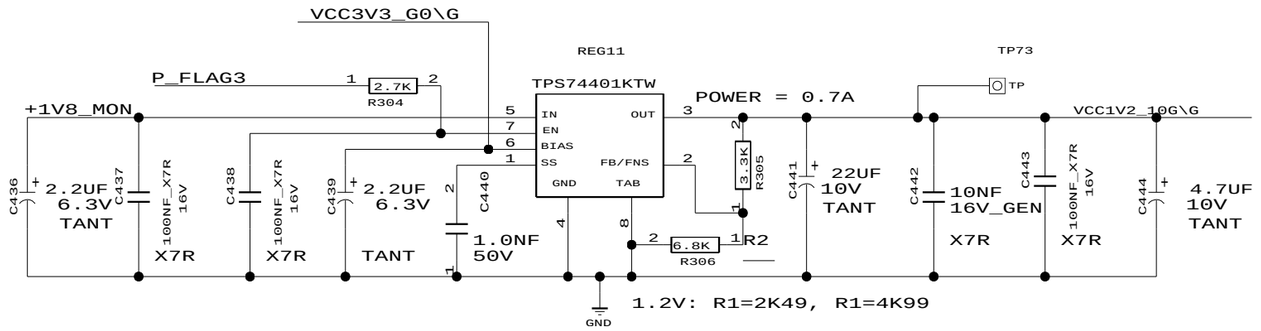
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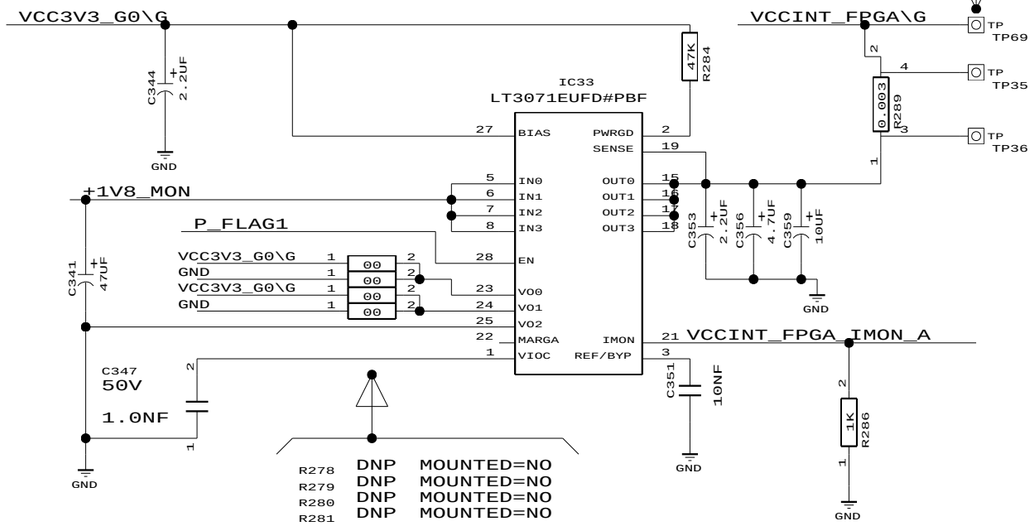
Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010

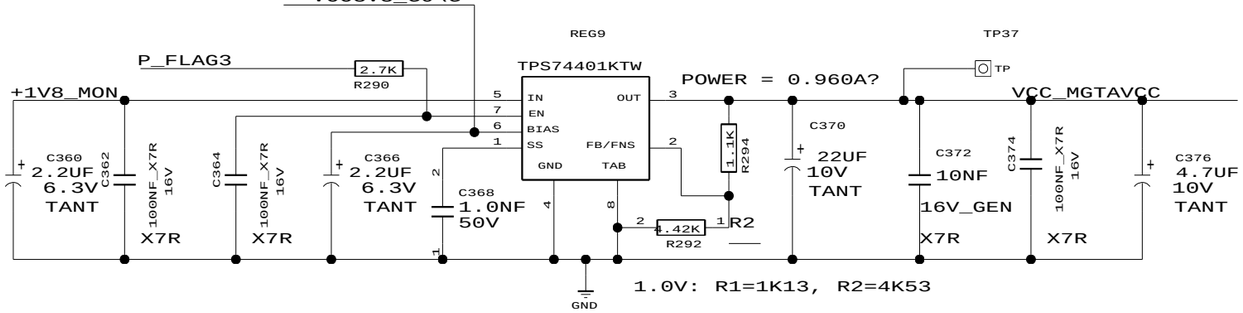
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND
TE/MPE

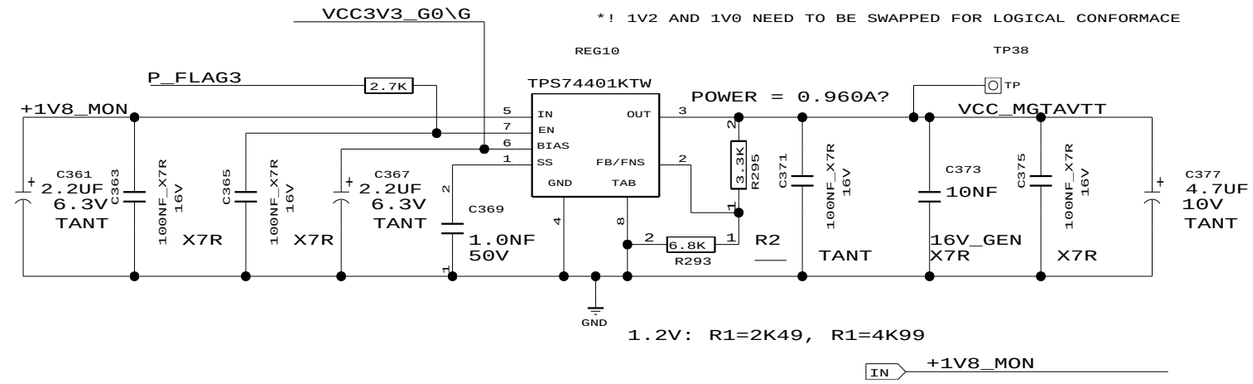


PCB: SILKSCREEN:
VCCINT(1V0)









*! 1V2 AND 1V0 NEED TO BE SWAPPED FOR LOGICAL CONFORMACE

IMON = 400UA PER AMP
R = 1K
V= 2V VS IOUT=5A

NOTE:
LOW IMPEDANCE, WIDE AND THICK COPPER TRACE
FOR POWER SIGNALS WITH LARGE CURRENT

IN +1V8_MON
IN P_FLAG1
IN P_FLAG3
+1V5_DDR_IMON OUT
VCCINT_FPGA_IMON_A OUT
VCCINT_FPGA_IMON_B OUT
VCC_MGTAVCC OUT
VCC_MGTAVTT OUT
IN DDR_PS_EN

Project file:sru_rev2.cpm
SYSTEM:

TE/MPE
CERN
European Organization
for Nuclear Research
1211 GENEVA 23
SWITZERLAND

PROJECT:SRU v2.0

MODULE:power_ldo_east | Sheet: 1/1 | Module: / Project: 81/81

LAST_MODIFIED=Fri Dec 09 11:02:00 2011

Design by: FZhang/SMartoiu | PCB by: EXT | DATE: 29/07/2010