Specification

SAltro16 carrier board

This document is a specification concerning the principle of mounting the SAltro16 die onto a small board to simplify its mounting onto electronics.

Document History

Rev.	Date	Author	Comment
0	2011-11-27	Björn Lundberg	
1	2012-01-01	Björn Lundberg	Added bond info
2	2012-11-24	Björn Lundberg	Layout update
3	2012-12-02	Björn Lundberg	Updated pics
4	2012-12-05	Björn Lundberg	Corrections
5	2013-08-14	Björn Lundberg	Added missing pin
6	2014-01-15	Björn Lundberg	Removed bias resistor
7	2016-09-22	Björn Lundberg	

Background

The SAltro16 chip is a 16-channel integrated low-noise amplifier, signal shaper, 10-bit ADC and a digital signal processing unit and was developed by CERN in order to be able to build compact detector electronics.

This document describes the mounting of the die onto a small intermediate chip carrier board.

Specification

The bare SAltro16 chip is a silicon die measuring 8.56x5.75 mm^2 with 229 bond-pads.
A chip carrier board's function is to fan out the die's bond-pads onto a footprint that is comparable to the size of the die itself while still possible to mount using standard component-mounting techniques. It should also allow chip-testing on a per-die basis instead of testing a complete mounted board with several bonded dies.

The size of the carrier board was initially chosen to be 8x11mm^2 as this allowed enough space for the bond-pads as well as some passive components that should be placed close to the chip to save board-space on the read-out board.
However, mainly because of uncertainties of the actual die-size after cutting and of the bonding procedure, the carrier board was grown to 8.90x12.0mm^2.

In order to connect the carrier to the read-out electronics, an underside BGA footprint with 0.5 pitch was selected in order to fit enough pads to fan out all the dies bond-pads.

Description

The SAltro16 carrier board has the die mounted on top together with some passive components around its peripheral on top of a 0.7mm thick PCB as shown in figure 1.
The passive components are de-coupling capacitors and filter networks (RC) and the capacitors and resistors are of the size 0201 or 0603 Metric which is 0.5x0.25mm^2 in size.

The bottom side of the PCB has a 0.5mm pitch BGA pattern arranged in a non-fully populated 20x13 ball-matrix with pin designation as shown in figure 3.
Table 1 list the pins in the BGA footprint

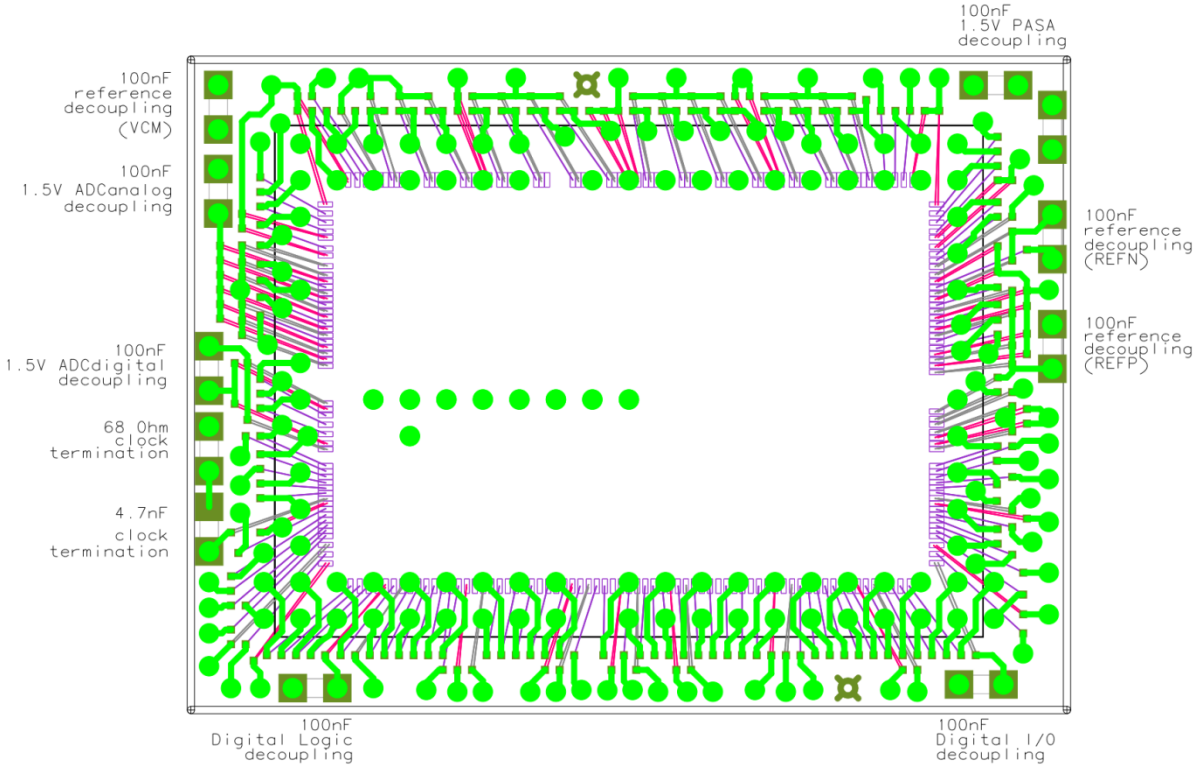


Figure 1 **Saltro16 carrier board chip bonding & component mounting**

Figure 2 **Carrier board and die in natural size!**

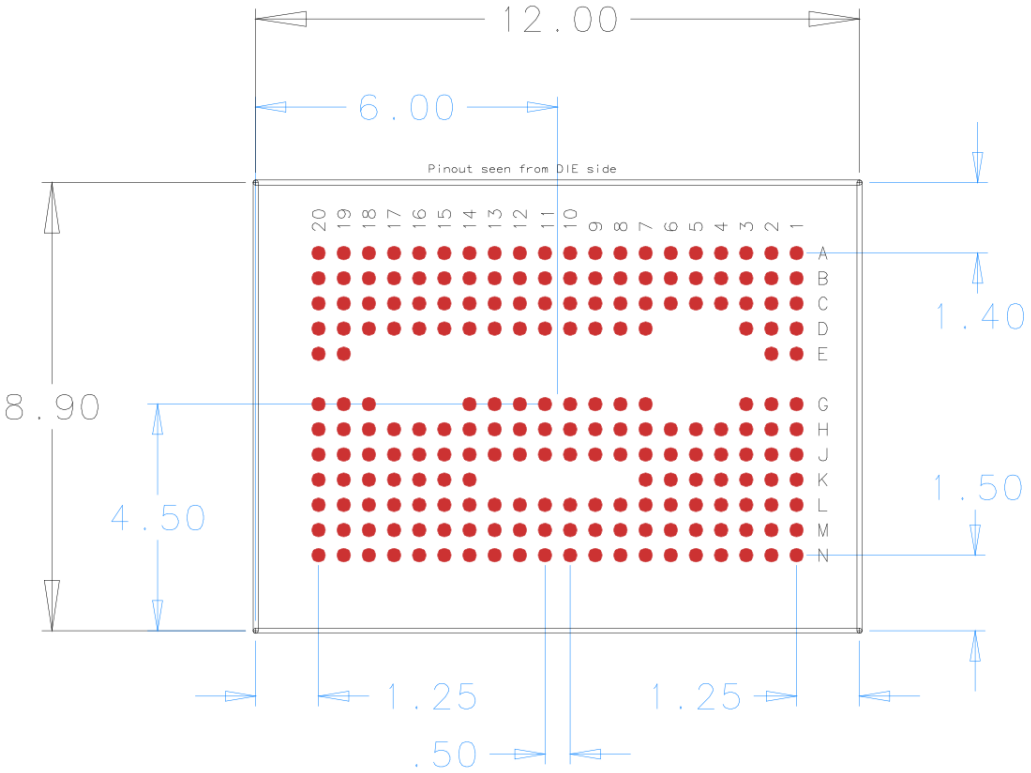


Figure 3 **SAltro16 carrier board footprint**

Pin function	Pin designation
ADC Analog ground	D7-D20
ADC Digital ground	G2,H6-H9
PASA power	C5-C12
PASA ground	D1
ADC Analog power	C13-C18
ADC Digital power	G7-G14
Digital power	G3,H2,H3,K4-K5
Digital ground	H10-H18
Output driver (IO Power)	K6,K7,K14-K16,L5,L6,L8-L10,L13-L16
IO ground	J5-J15
Chip guardring1-2	H4,H5
Chipaddress AD0-AD7	H1,J2-J4,J17,J19,K17,J20
Input 15-0	A3-A18
InputGround 15-0 (PASA ground)	B3-B18
Outputs 0,1,2…38,39	N1,M1,N2,M2,N3,M3…N19,M19,N20,M20
ADCTestN, ADCTestP	C2,D2
Gain1,Gain2	A19,B19
Shaper1-Shaper3	A20,C19,B20
RefN (2 pins), RefP	C1,E19 E1,G19
TestMode	A1
Shutdown	A2
PasaTestN,PasaTestP	B1,B2
PreampMode	C3
DecayBias	C4
Bias	D3
VCM	E2,E20
Polarity	C20
CMOut1,2	G20,G1
ClkSel	H19
CLKAUX	G18
ADCAdd0,1	K2,J1
ADCClk	H20
_TRG	K1
_L2Y	L2
_TMS	K3
_ACK	L4
_ACKEN	L3
SCANEN	L7
RDOClk	L11
ScanMode	L12
_ERROR	L20
_WRITE	K20
_CSTB	J16
_DSTB	L17
_RST	J18
_DOLOEN	K18
_GRST	K19
_TRSF	L18
_TRSFEN	L19
TSTOUT	L1

Table 1 BGA pinlist

Chip bonding

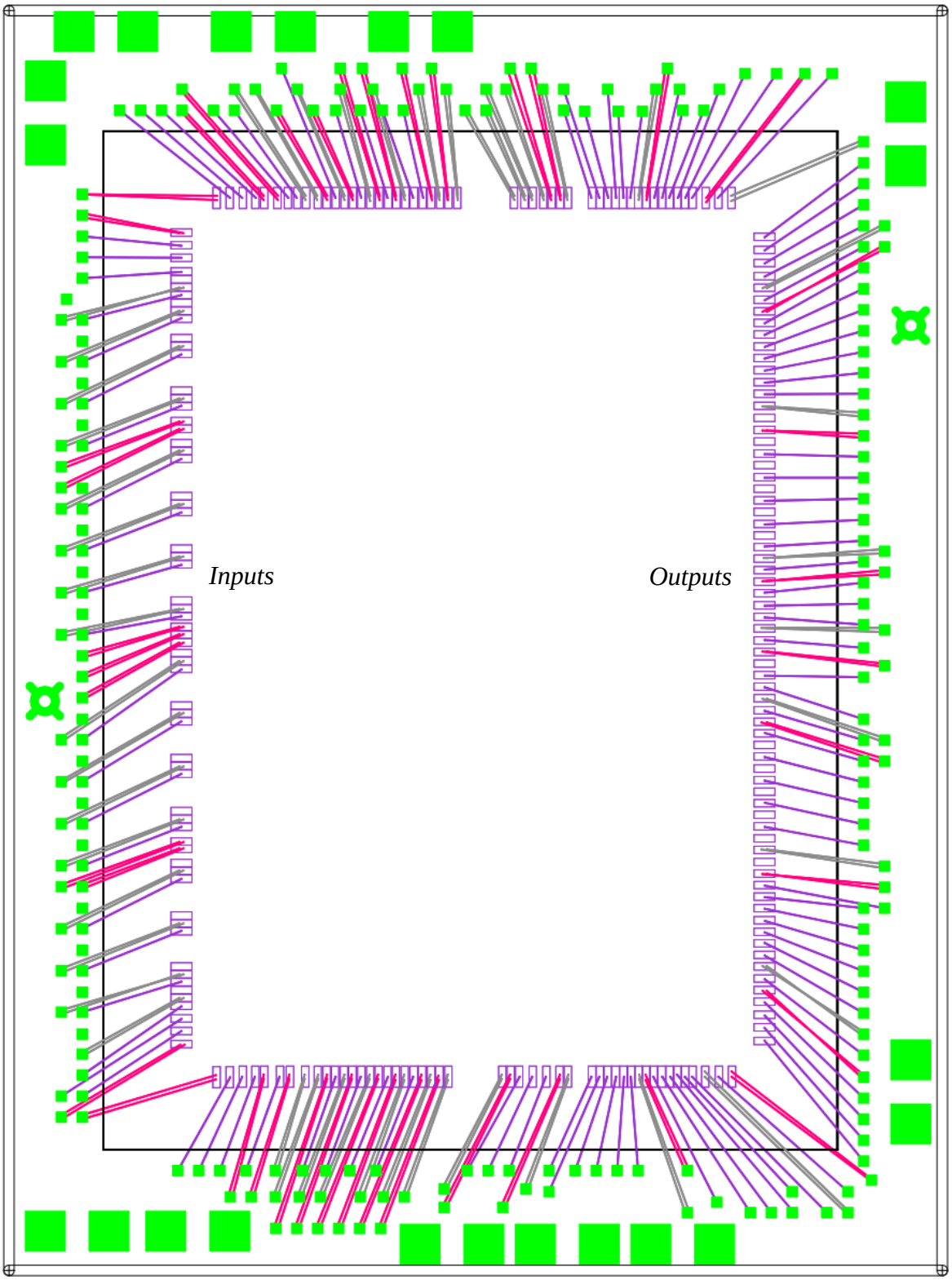


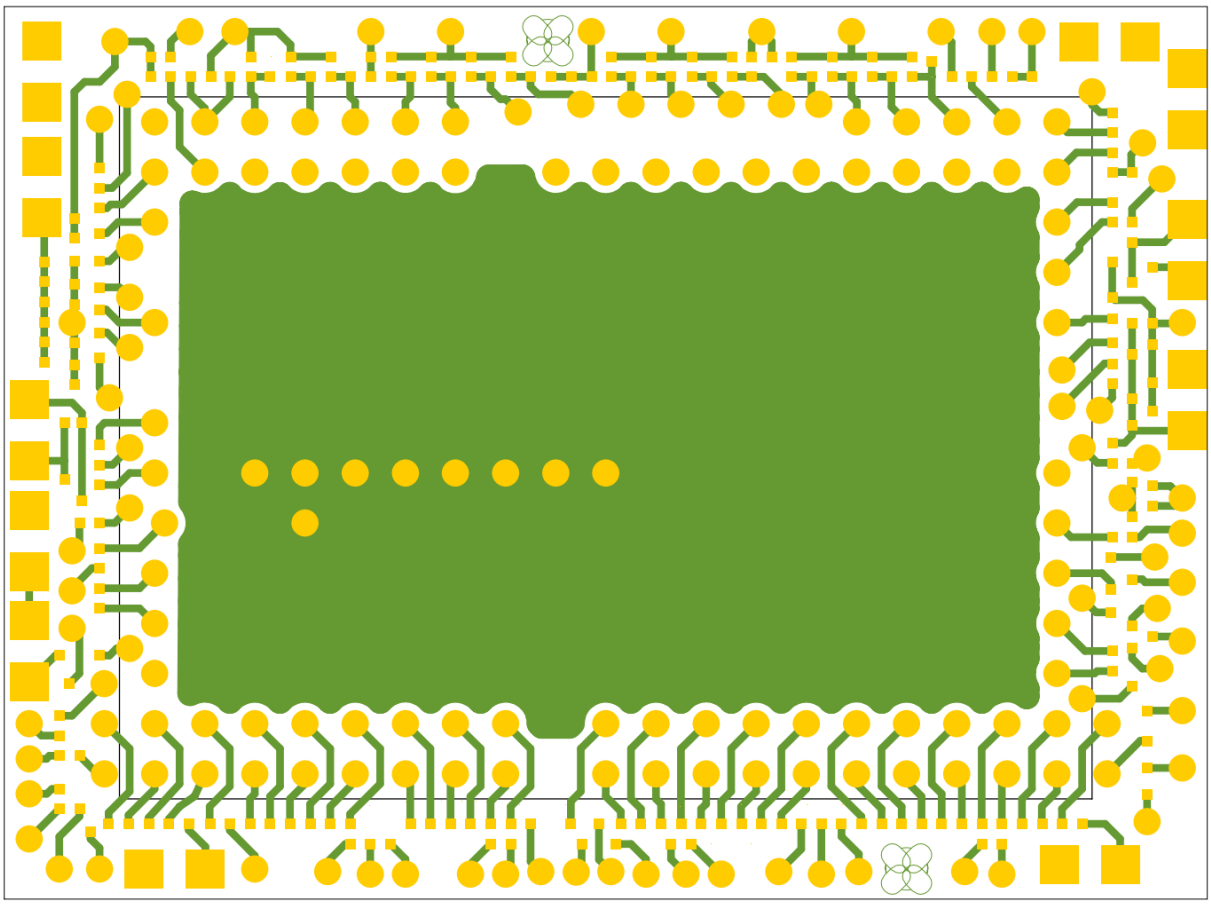
Figure 4 SAltro16 bonding

Figure 4 shows the expected bonding scheme for the SAltro16 die and the location of the bond-pads on the die.

In order to further decrease power impedance and increase the performance of the power delivery system by lowering resistance and inductance of power bonds, power pads should have multiple bond-wires attached.
Figure 4 shows the ground bond-wires in grey and power bond-wires in red.

The copper-area below the die itself has ground potential which is the same as the die substrate. However because of the density of the carrier-board, the area below the die itself can't be cleared from traces or vias and therefore the die should be glued onto the board with non-conducting glue.
The ground-plane below the die will however be connected with the other planes inside the board in order to help transport heat away from the die.

Inputs



Outputs

Figure 5 Top-layer layout view of carrier-board with die outline

Stack-up

The printed-circuit board (PCB) carrying the SAltro16 die is a 0.7mm thick 8-layer board with 4 signal layers and 2 pairs of power-planes. The chip is directly glued to the PCB and bonded onto the PCB bondpads, a technology called chip-on-board or COB.
A similar technique is when several chips are bonded onto a PCB which is called a multi-chip-module on laminate or MCM-L.
The bonding of the chips directly onto the PCB requires that the surface finish of the PCB can handle the bond-welding of the chip bond-wires and normally a 5um Nickel barrier with a 1um Gold plating is required (hardgold plating).
The suggested stack-up is shown in table 2.

Layer no	Saltro16bga board stack-up								
						Thickness			Usage
	Stackup				Material	Layer	Layer	Surface plating	
		Plating Gold				unpressed	pressed	0.001	
		Plating Nickel			Soldermask	0.02	0.02	0.006	
	Plating				Copper	0.02	0.02		
1	TOP				Copper	0.018	0.018		die, bond
a	Prepreg				1x1080	0.065	0.047		
2	SIGNAL				Copper	0.018	0.018		signal
b	CORE				1x2125	0.1	0.1		
3	PLANE				Copper	0.018	0.018		PASA, ADCA, IOPwr
c	Prepreg				1x108	0.05	0.0428		
4	PLANE				Copper	0.018	0.018		PASA, ADCA, IOGND
d	CORE				1x2125	0.1	0.1		
5	PLANE				Copper	0.018	0.018		PASA, ADCD, DigPwr
e	Prepreg				1x108	0.05	0.0428		
6	PLANE				Copper	0.018	0.018		PASA, ADCD, DigGND
f	CORE				1x2125	0.1	0.1		
7	SIGNAL				Copper	0.018	0.018		signal
g	Prepreg				1x1080	0.065	0.047		
8	BOTTOM				Copper	0.018	0.018		BGA balls
	Plating				Copper	0.02	0.02		
		Plating Nickel			Soldermask			0.006	
		Plating Gold				0.02	0.02	0.001	
	Via definition	L1-L2	L2-L7	L1-L8					
		L7-L8							
	Total thickness					0.754	0.7036		

Table 2 Carrier board stack-up

Although impedance matching of a board normally is critical in order to get best possible signal integrity, on a board of this size where the vias are more critical that the traces, impedance matching is in practice impossible to maintain and is therefore not enforced although it should be simulated and extracted as an S-parameter file in order to correctly simulate the board where it will be mounted.

Since the density of the board is very high and since the bottom side should be free from any copper except the BGA balls, the design has to be a high-density interconnect board (HDI) using a variety of via techniques interconnecting the different layers.
In order to get the most routing possibilities, the design utilizes blind and buried vias.
A blind via is a via that connects a subset of the available layers but starts from either top or bottom whereas a buried via only connects internal layers and isn't visible from external surfaces.

Power de-coupling

In order to de-coupling high-frequency noise, it’s critical to have as low inductance and low equivalent series resistance (ESR) of the de-coupling capacitors as possible.
To accomplish this the capacitors are placed as close to the chip power bond-pads as is physically possible.
The capacitor selection should also be performed with great care in order to get a component with a minimal stray-inductance and ESR and a generic de-coupling capacitor should not be selected.
The power impedance should be simulated to be able to simulate sufficient power de-coupling on the module where the carrier board will be mounted.
The dielectric layer between the two pairs of power-planes should be as thin as possible in order to increase its capacitance and therefore act as power de-coupling with minimal stray inductance for the highest frequency noise components.

The design requires 2 pairs of power-planes since the pads for output power and digital control as well as ADC analog and ADC digital power are physically interlaced and impossible to separate on a single power plane.

The power planes are generated as negative plots (i.e. everything drawn will be etched away) since this gives the highest resolution and best plane coverage.

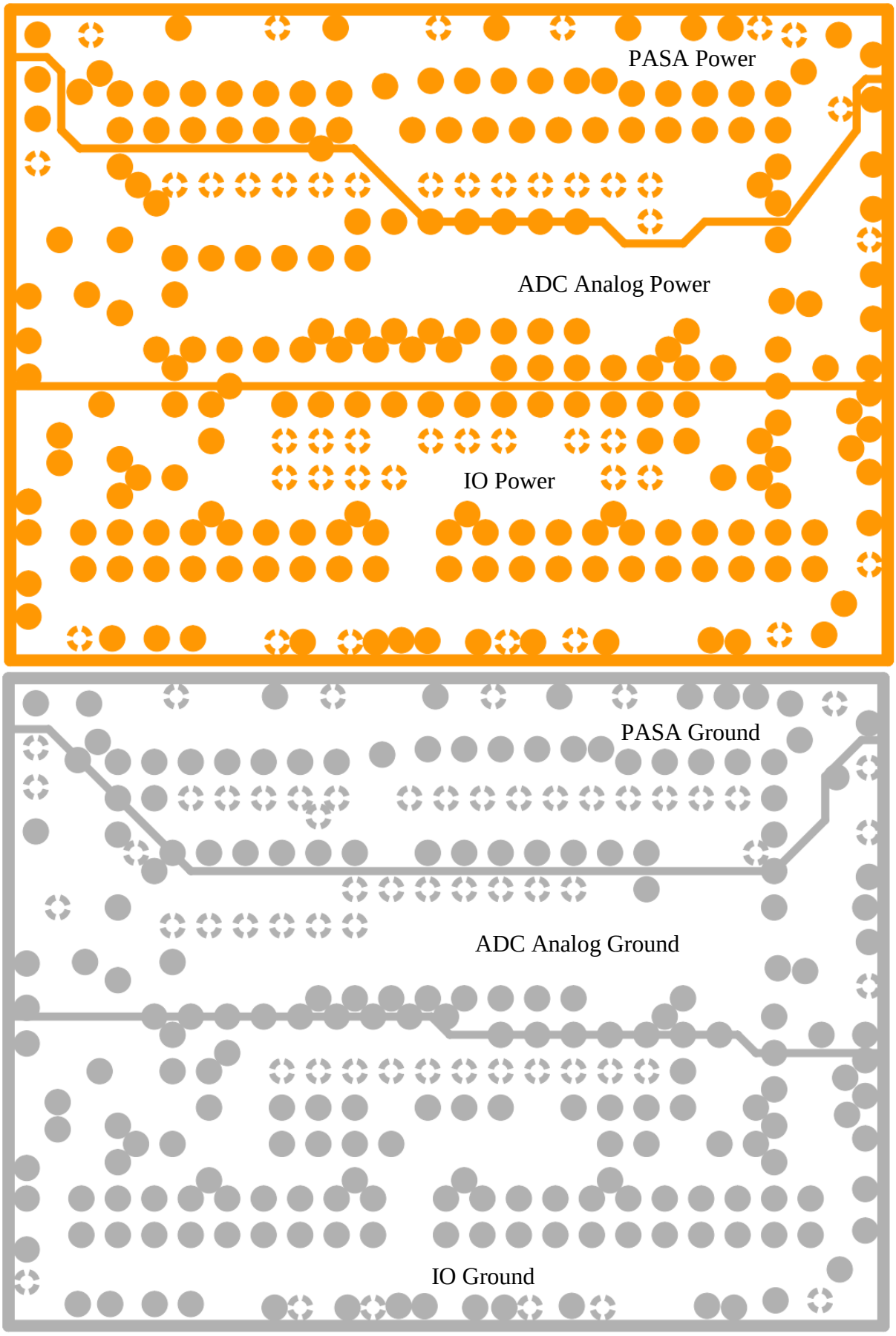


Figure 6&7 "Analog" power planes, layers 3&4

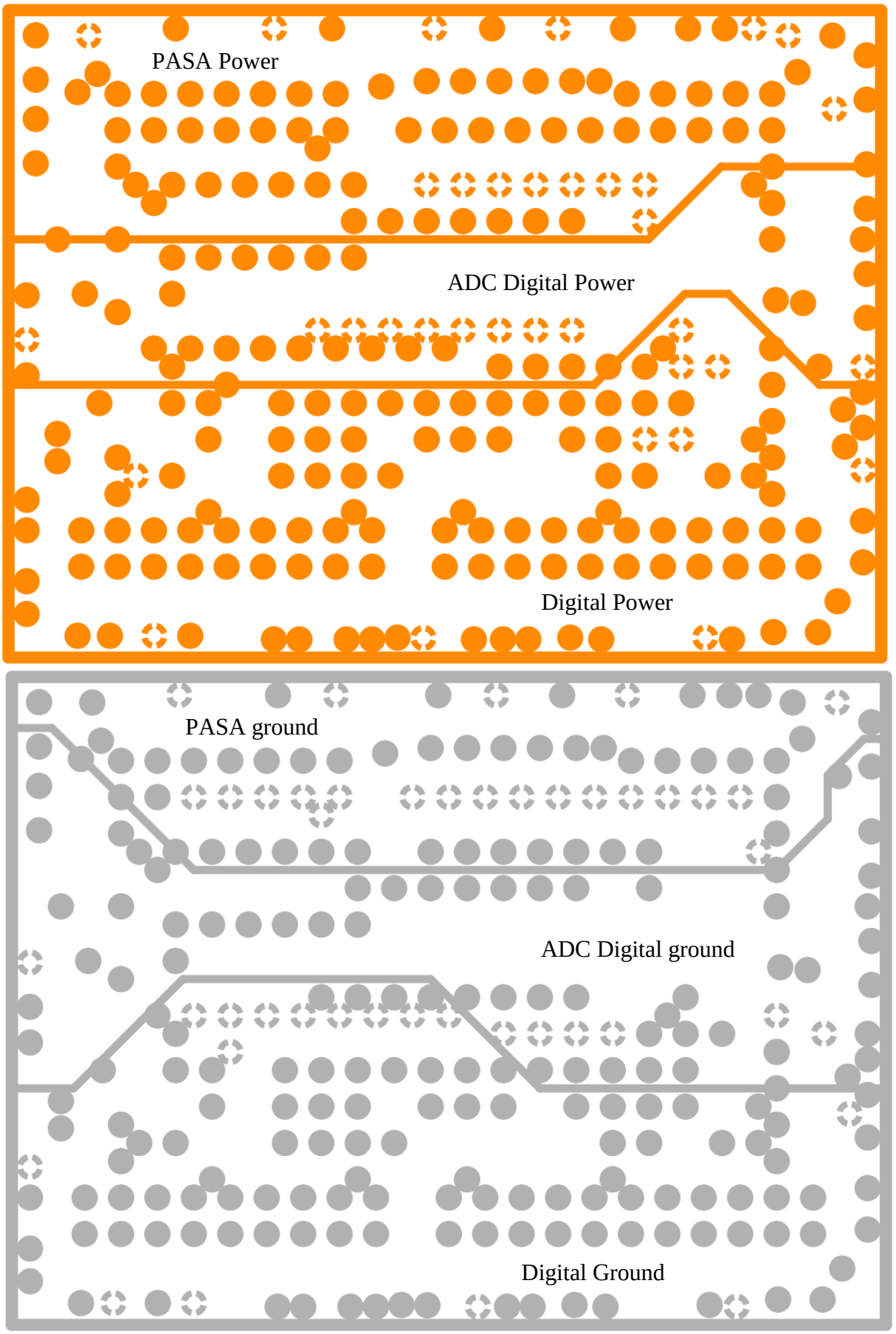


Figure 8&9 "Digital" power planes, layers 5&6

Manufacturing panel

Since the card are barely larger than the SAltro16 die, handling of the board during mounting is a difficult problem.
In order to simplify mounting and handling, 4 boards are manufactured together into a panel. The panel has milling paths in order to simplify separation of the physical boards after production and has some drill-holes in the periphery to aid fastening of the panel.
When the boards are fully assembled and protected, the boards should be separated from the panel. In order to get sufficient tolerance in the board's finished measurements, the preferred way is to machine out the excessive fiberglass between the board and the frame.

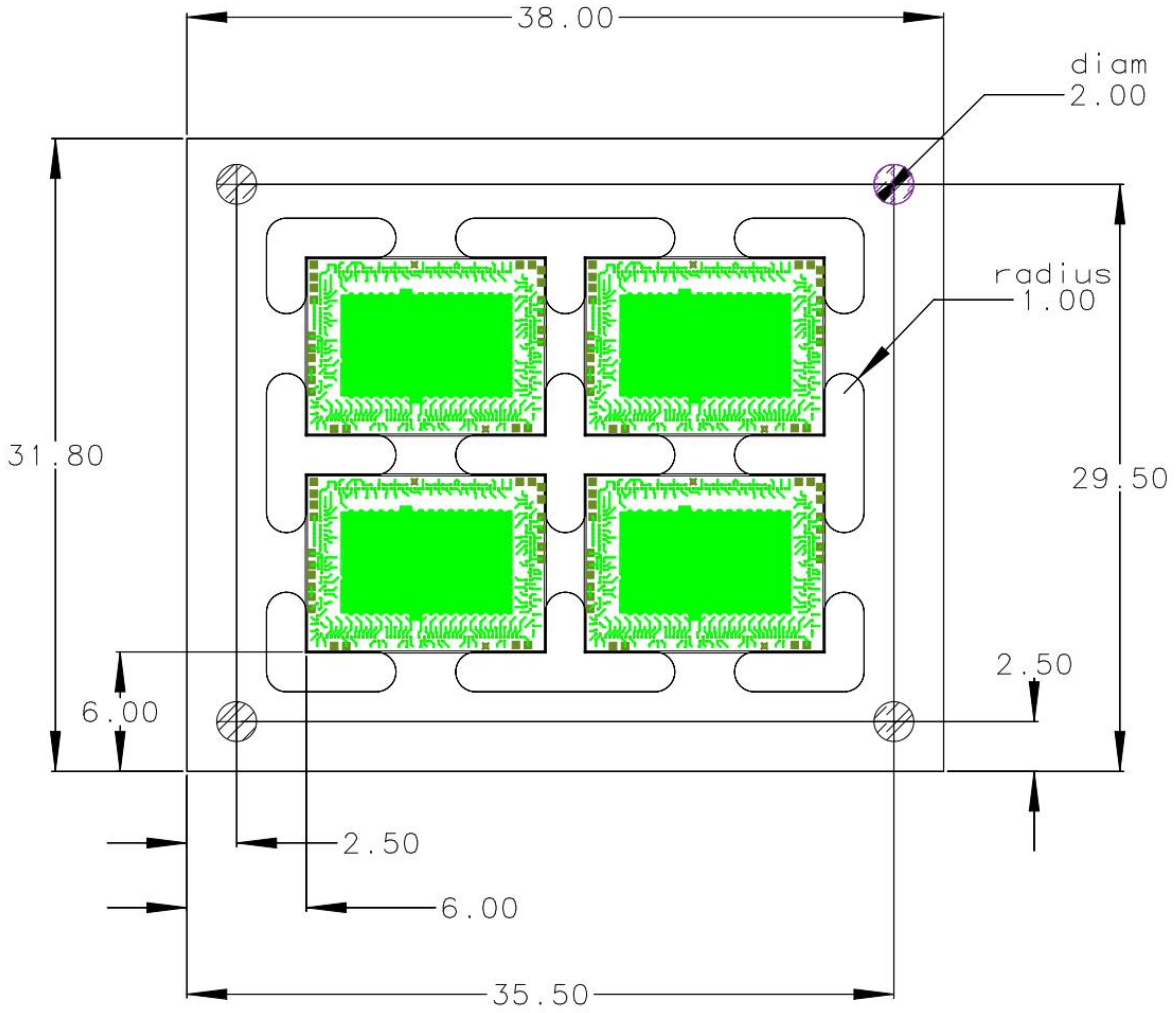


Figure 10 View of manufacturing panel