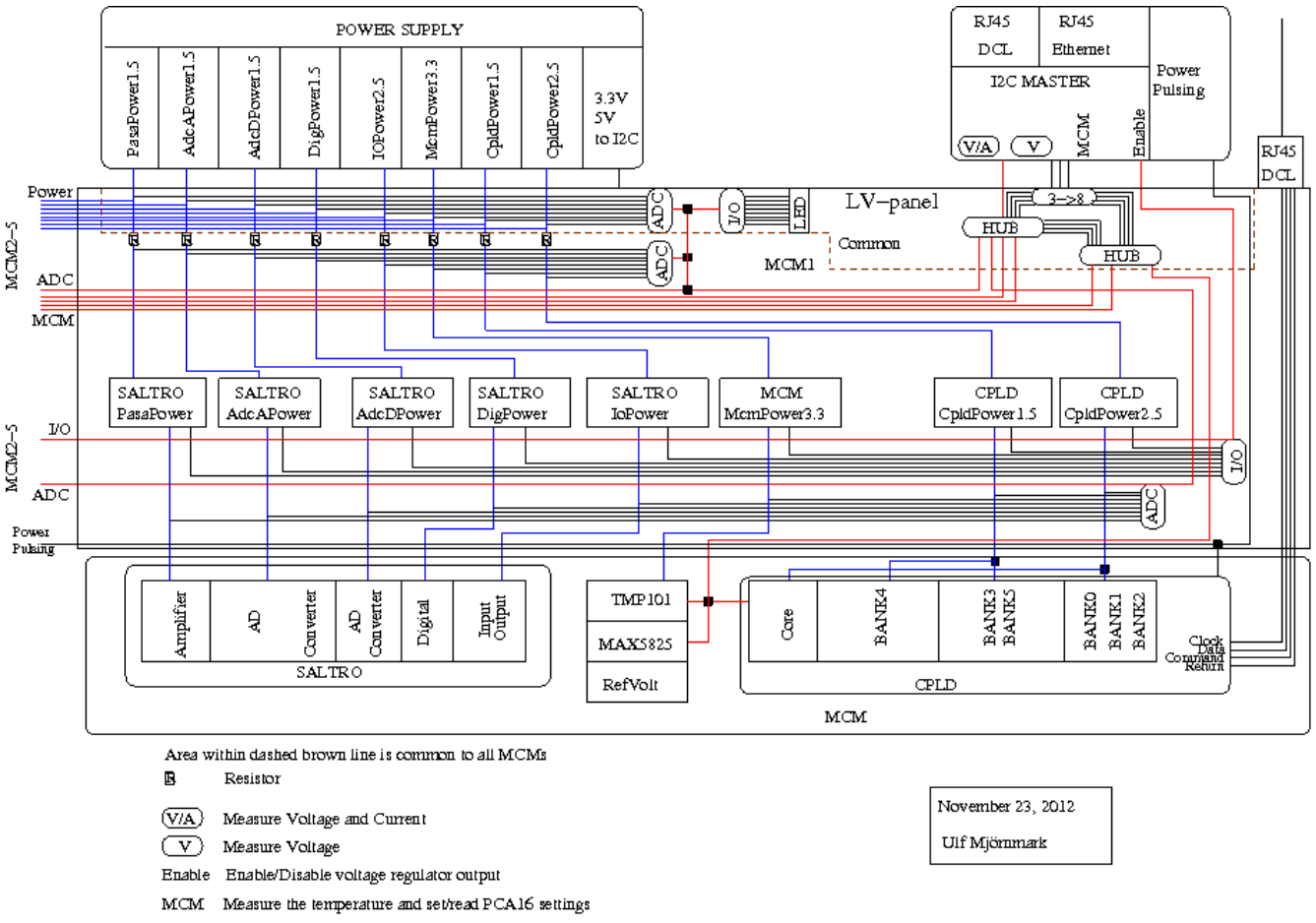
Some thoughts on power distribution and its monitoring with the I2C bus *Nov 15, 2012*

Power and I2C

The picture show an example of the power and I2C control needed for one MCM module.
For 5 LV panels of 5 MCMs each is the power supply the same.
The 8 SALTROs of an MCM share the same regulators, each MCM have different set of regulators.

The example is a maximum, one can most likely optimize it, the purpose of this document is to give an idea of what is needed.

Some questions:
How much current is drawn by the CPLD?
Can all CPLD on a panel have the same regulator?
Can the the regulators for the MCM, except the SALTROs, be the same for all MCMs on a panel?
Are the CPLD Bank voltages correct?
Cooling?
Etc ….



red lines are I2C buss, blue are power lines.

I2C bus

For a LV panel of 5 MCMs is the I2C MASTER (master of the I2C bus) the same.
The same master for more panels?

Some questions:
Should we measure the input Voltage/Current for each regulator or for a panel as a whole?
Should we measure the output of the MCM regulators?
How many devices can the I2C master handle?
Is there enough address space for the devices?
Which devices may be used for the V/A,V, and enable?
Etc ….

I2C controlled measurements per LV panel

Number of regulators:	(5(per 8 SALTRO) + 3(per MCM)) * 5 =8*5 = 40
V/A measurements:	8 + 5 (V & A) * 8 = 48
V measurements:	same number as regulators = 40

In total 88 measurements.

Proposed I2C devices

Device	*Number of*
8 ch ADC: LTC2309	11
8 ch I/O register: MCP23008	5

Divided into 8 I2C buses:
bus 1: 6 ADCs
bus 2: 5 ADCs
bus 3: Power on off – 5 MCP23008
bus 4.1: MCM1
bus 4.2: MCM2
bus 4.3 : MCM3
bus 4.4: MCM4
bus 4.5 : MCM5

On the LV panel are two I2C HUBS (PCA9518A) for selecting the I2C bus in use. Optionally a ninth bus to set LED status indicators (using an extra I/O register MCP23008)

Prefer to have bus3 independent of the I2CHUB, want power on/off to be independent of extra hardware.

I2C Devices on MCMs for one LV panel

Temperature and PCA16 DAC settings:
MCM I2C devices: 3 (TMP101,MAX5825,CPLD) * 5 = 15
Should these be controlled from CPLD or external master?

Programming of the CPLD

To be defined.

Power distribution

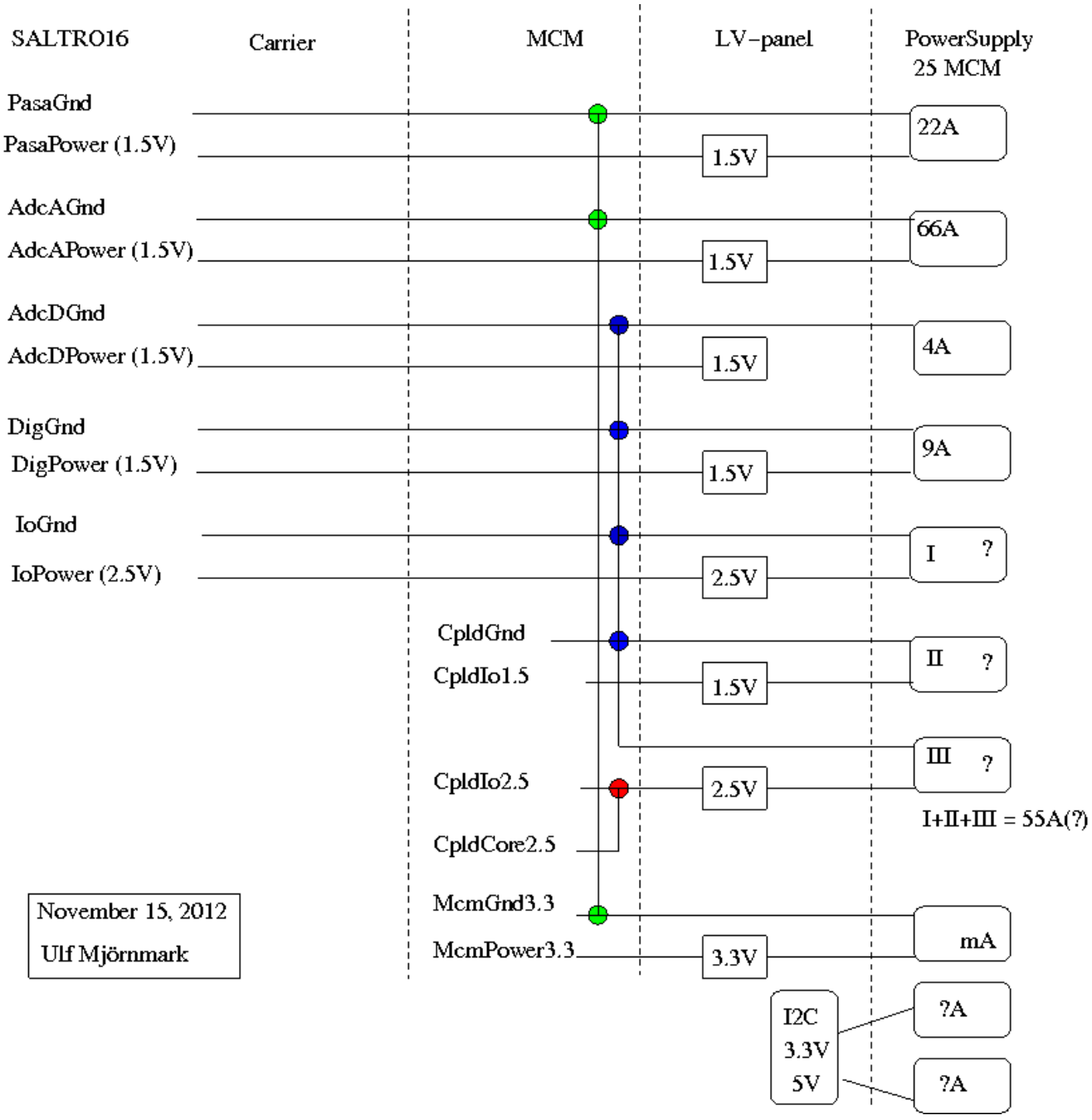
The figure below show a schematic proposal for the power/ground lines from supply to MCM/carrier.

SALTRO:
PasaPower, AdcAPower, AdcDPower, DigPower, IoPower
PasaGnd, AdcDGnd, DigGnd, IoGnd

MCM:
CpldIo1.5, CpldIo2.5, CpldCore2.5, McmPower3.3
CpldGnd, McmGnd3.3

Please note where the power and grounds are connected together.
The numbers in the power supply boxes are the currents for 25 MCMs as taken from the table below the figure, the table is taken from Anders calculations.

The example is a maximum, one can most likely optimize it, and is intended to give an idea of what is needed.



domain	*channel*	*chip*	*Vcc*	*A/chip*	*A/MCM*	*A/5MCM*	*A/25MCM*
PasaPower	0.01026	0.16416	1.5	0.10944	0.87552	4.3776	21.888
AdcAPower	0.03128	0.50048	1.5	0.33365	2.66922	13.346	66.730
AdcDPower	0.00171	0.02736	1.5	0.01824	0.14592	0.7296	3.648
DigPower	0.00404	0.06464	1.5	0.04309	0.34474	1.7237	8.618
IoPower	0.0427	0.6832	2.5	0.273	2.18624	10.9312	54.656
+FPGA/CPLD??							

Can the last line (IoPower+FPGA/CPLD) be correct?

Devices		*mA/MCM*	*mA/5MCM*	*mA/25MCM*
TMP101 (3.4MHz,Bus active)	3.3	0.15	0.75	3.75
MAX5825 (max at 5V)	3.3	2.5	7.5	22.5
CPLD	?	?	?	?