Front-end electronics for the TPC in ILD; a status report October 2013

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Abstract

A high resolution TPC is the main option for a central tracking detector at the future International Linear Collider (ILC). The MPGD (Micro Pattern Gas Detector) technology has been used to read out a Large Prototype TPC with electronics built for the ALICE experiment and further developed to meet the requirements of the ILC. The first step was to demonstrate that the MPGD readout provides the necessary precision, set by the physics goals of the ILC. The next step, which is aiming for a miniaturization of the electronics to approach the final goals of the front end electronics, is discussed and the status as of October 31^{st} 2013 is given.

1 Introduction

The realization of the readout electronics for the TPC in the ILD proceeds in three steps. The first step (EUDET) was to provide front-end electronics for the proof of principle phase, the aim of which was to demonstrate the feasability of the Micro Pattern Gas Detectors (MPGD), GEM's and MicroMegas, with respect to the requirements set by the physcis challenges at the future Linear Collider. This step has been successfully completed. The electronics system set up for the EUDET project provides very flexible test environment and if tests with really small pads turn out to be necessary the EUDET system should be used also in the future, since the electronics is connected to the pad plane via long kapton cables and thus the pad size is not directly correlated to the size of the electronics.

The second step (AIDA), which is presently ongoing, is the engineering phase with the aim of constructing an electronic system, which essentially meets the various requirements of the final front-end electronics. The electronics of the second step is based on the SALTRO16-chip, developed at CERN. (For a detailed description of the SALTRO16-chip and its charactrization see the theses of Massimiliano De Gaspari, http://archiv.ub.uni-heidelberg.de/volltextserver/13806/, of José García, http://riunet.upv.es/handle/10251/16980 and of Hugo Franca, http://cds.cern.ch/record/1563856/). The LCTPC-collaboration has obtained 610 such chips (210 as a contribution from CERN and 400 bought by Japanese groups). In order to achieve a significant reduction in size of the front end electronics, most modern techniques for circuit assembly is used. In almost all aspects, it means to stretch the techniques beyond what is used in industrial manufacturing today. Thus the development has to be done in close cooperation with industry. The major complication arises from the fact that the SALTRO16 dies are untested. Further restrictions are due to cost and availability of the chips, and that the yield is unknown.

The third step is to develop and produce the final electronics for the ILD.

2 The SALTRO16 Chip and the Carrier Board

The SALTRO16 readout system is schematically shown in Figure 1 for one pad module. It is a highly advanced development project, which includes several subsystems like the Carrier Board, the MCM-board, the Low Voltage Board, the Detector Control Boards, the Serial Readout and the Monitoring. A complication is that these subsystems are not independent but has to be developed in parallel. In order to facilitate testing and debugging of the various subsystems, it has in some cases been necessary to construct prototype systems to avoid complications due to the requirements of compactness or due to other constraints. The Carrier Board and the MCM-board are especially challenging due to the tight space limitation and the high precision required. The project has to be performed in collaboration with industry, which has the necessary competence and experience. Due to the limited number of chips existing, the unknown chip yield and their high costs we have to take extreme care to minimize the number of prototype steps and in the choice of industry partner in order to minimize the loss due to unpredictable fabrication yield.

The SALTRO16 chip combines the analogue and digital signal processing of the incoming charge. The silicon die itself is 8.7x6.2 mm^2 and contains 16 readout channels which equals an occupancy of 3.37 mm^2 per channel. The new chip can be turned off when no signals are expected, which reduces the power consumption and the demands for cooling drastically.

The alternative of using packaged chips is not a realistic choice since it requires too much space on the pad board in order to allow small enough pad sizes, although testing, mounting and service would

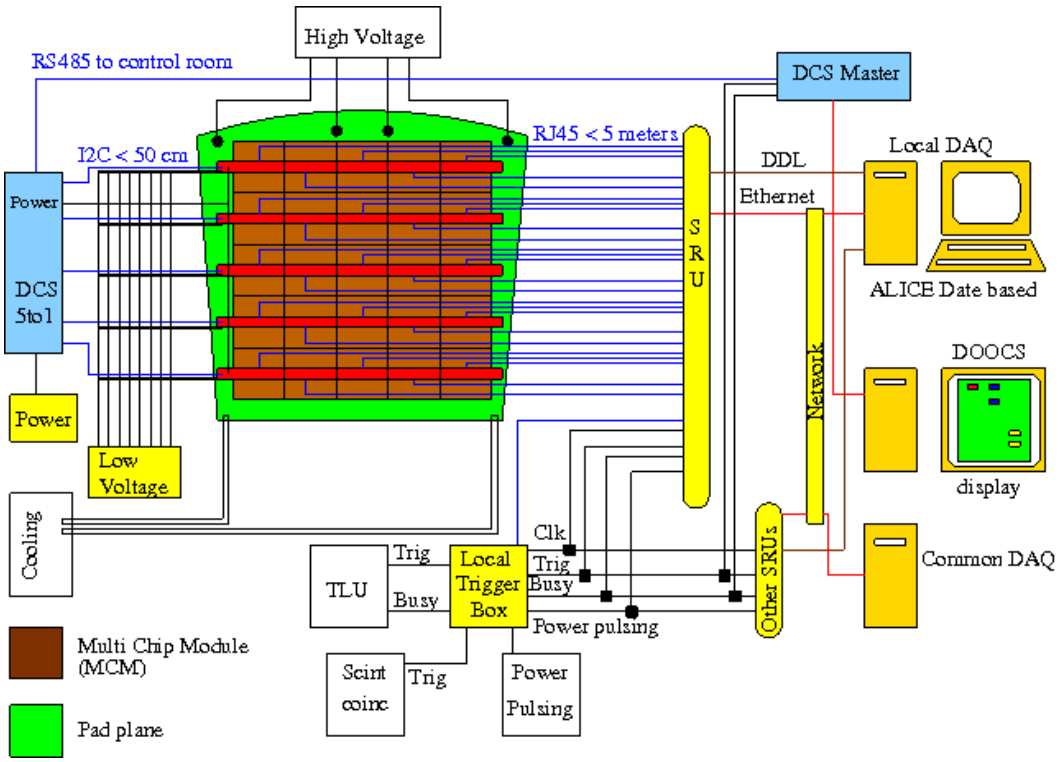

Figure 1: *Schematic view showing the DAQ architecture of the SALTRO system.*

be simpler. Due to the uncertainty in the yield it is unrealistic to assemble untested dies directly on a pad module with the requirement that all chips should work. Instead the chips will be mounted on Carrier Boards, only slightly bigger than the chips themselves, which simplifies the handling and enables tests of individual chips. The size of the Carrier Boards is 12.0x8.9 mm^2, which also includes space for bonding wires and some passive components. Eight of these Carrier Boards are mounted on one so called Multi Chip Module (MCM) (see Section 4), using BGA soldering. The BGA grid has a pitch of 0.5 mm.

The layout of the Carrier Board is shown in Figure 2.

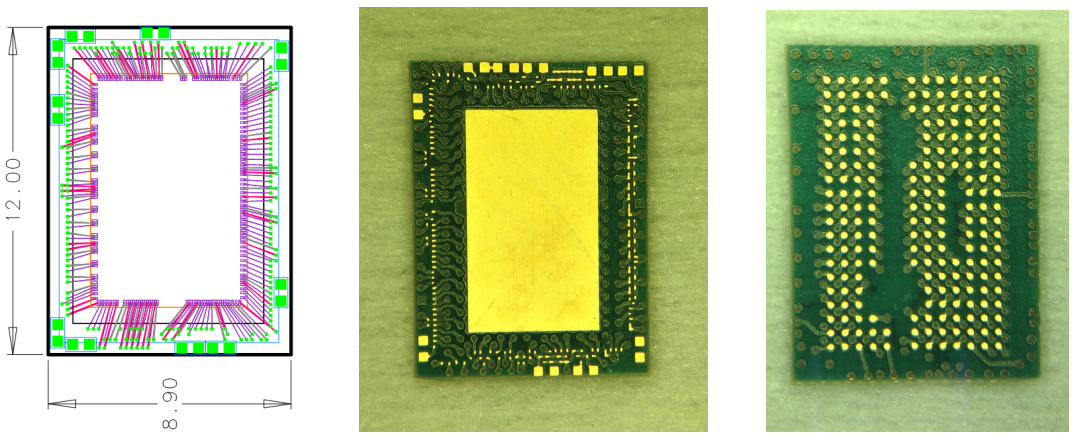

Figure 2: *Layout of the carrier board with bonding wires and passive components (left) together with photos of the top (middle) and bottom (right) surface, respectively, of one circuit board.*

Recently 250 boards were delivered and Figure 2 also shows photos of the top and bottom surface,

respectively, of one board. The yellow area on the top surface is where the SALTRO16 die will be glued. The application of small tin balls on the bottom side of the Carrier Board has been succesfully accomplished. Further has the mounting jig for mounting of the chip and other components been produced and the first fully mounted Carrier Boards for testing are expected in week 45.

For the final electronics system, the dies must be tested directly on the wafer and then the assembly will be much more like a standard assembly and even smaller size is possible by either bonding the chips directly to the MCM-board without carrier boards or mounting by flip-chip technology. Together with an integration of more channels per chip (64 or 128) a further miniaturization of at least a factor 2 is expected.

3 The Test Socket and the Test Socket Board

For functionality tests of SALTRO16-chips mounted on Carrier Boards, a Test Socket will be used. This is a jig with an insert which fits the Carrier Board (see Figure 3).

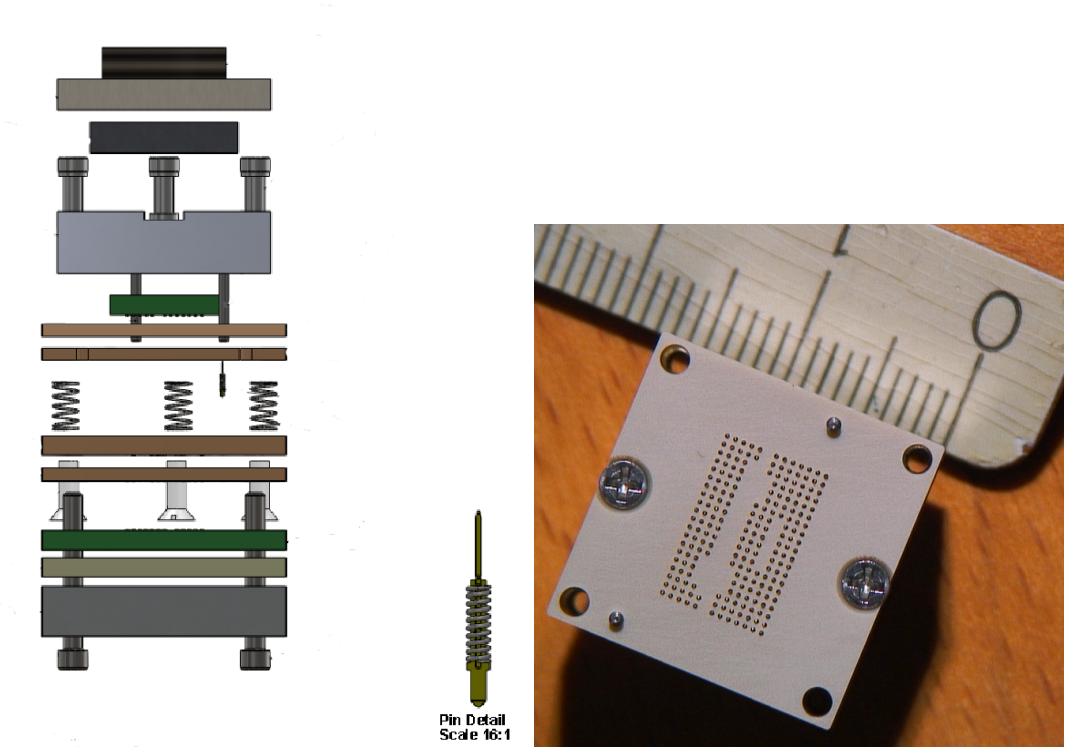

Figure 3: *Exploded view of the Test Socket and a photo of the delivered Test Socket showing the BGA-pattern of holes for the probes pins. A probe pin is shown to the left of the photo*

There are spring loaded probe pins guided by small holes in the bottom of the Test Socket, which make contact with the solder balls on the bottom surface of the Carrier Board. In order to secure sufficient contact of the 208 probe pins, a strong force has to be applied from above. A thin layer of epoxy protects the chip, bondwires and passive components on the Carrier Board. This epoxy glob has to have a flat surface to distribute the force evenly over the whole board. The pins connect from the solder balls to the Test Socket Board, which has a matching BGA-grid and provides an interface between the Test Socket and pin grid array (PGA) socket on the CERN SALTRO test board, which

was used to characterize the first packaged SALTRO16-chips. The CERN SALTRO test board is read out with the EUDET readout system.

The Test Socket itself is a commercially available, high tech product offered by Ironwood Electronics, USA. The socket has to be modified to fit our BGA pattern and chip dimensions. The Test Socket has been delivered and drawing of the Test Socket together with a photo of it are shown in Figure 3 (note the small size). The design of the Test Socket Board is completed and will be ordered, after som final inspection, within a few weeks.

4 The MCM-Board

The Carrier Boards are mounted onto the MCM-boards by soldering of small tin balls on the back side of the carrier board, organized in a so called BGA foot-print. Figure 4 shows the layout of the two sides of an MCM-board.

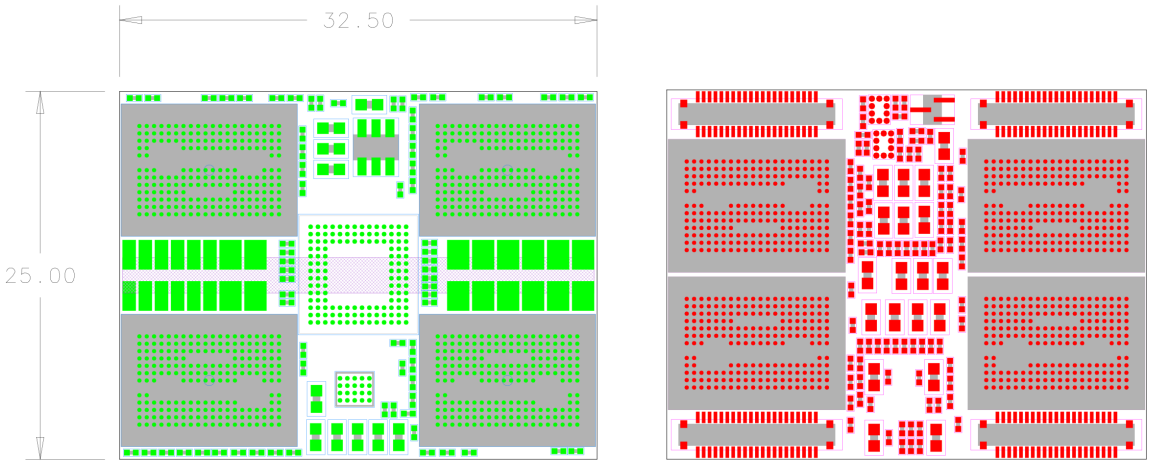

Figure 4: *The MCM-board top surface (left, green) and bottom surface (right, red)*

The advantages in placing the electronics components on separate boards, compared to soldering them directly onto the pad board, are listed below.

- Trace routing from the pads to the SALTRO chip becomes simpler since translational routing will essentially only be necessary at the edges of the pad module.
- With fewer or no active electronics components on the pad board it will be easier to design.
- Changes during the electronics prototyping will be cheaper and easier to implement and test.
- The interface between the SALTRO-part and the controller/readout-part is well defined.
- The trace routing on the plug-in board will be easier compared to the trace routing in the case all the electronics components are placed directly on the pad board. The pad board will need less layers.
- It moves heat away from the TPC endplate.
- It facilitates service. A malfunction in the readout chain can be fixed by replacing the electronics board instead of dismounting the whole pad board.

The MCM-boards will be attached to the pad board via 4 micro-connectors of type Panasonic P4S, which have a lead pitch of 0.4 mm and a mated height of 3 mm, and transmit the signals from the pads to the preamplifier of the SALTRO16-chip. The connectors have to be mounted with very high precision on the pad board and on the carrier board since four such connectors have to fit simultaneously and the space between the MCM boards is very small.

In order to meet the area constraints, the Carrier Boards have to be mounted on both sides of the MCM-board. That is possible since the Panasonic connectors are elevating the MCM-board by 3 mm above the pad board, which thus leaves enough space for components on both sides of the MCM-board. In Figure 4 the rectangles with a dot-matrix of 20x13 dots are 8 sets of BGA patterns (4 on each side) for the SALTRO Carrier Boards. These boards are placed in each corner of the MCM-board such that the analogue inputs are facing outwards towards the long edges of the MCM-board. On the bottom surface the four 42-pin connectors for the 32 input signals (plus grounds) also are placed along the long edges of the board. The digital signals are concentrated towards the centre of the board. In the centrally placed square on the top side of the MCM-board, the BGA footprint of a CPLD (Complex Programmable Logic Device) is seen, which has an area of only 8x8 mm^2 (for details see Section 4.1). Also on the top surface of the MCM-board a connector for distribution of the low voltage and transmission of the signals from the MCM-board has to be placed. The available space is, however, very limited and the connector needs to have a minimum of 26 pins. The total current drawn by the MCM-electronics is about 16 A per MCM at 8 different voltages, corresponding to a power consumption of about 10 W per board, and it might be that some voltage needs more than one pair of pins (voltage and ground). Samtec offers connectors that have two rows of 30 pins per row, one for edge mounting and one for surface mounting. Each pin can take a current of 1 A. The connector has a length of 31.2 mm, which corresponds to almost the total length of the MCM-board, and it has a width of 6.7 mm. Possible solutions to mount these connectors are shown in Figure 5. Efforts continue to find the best possible solution.

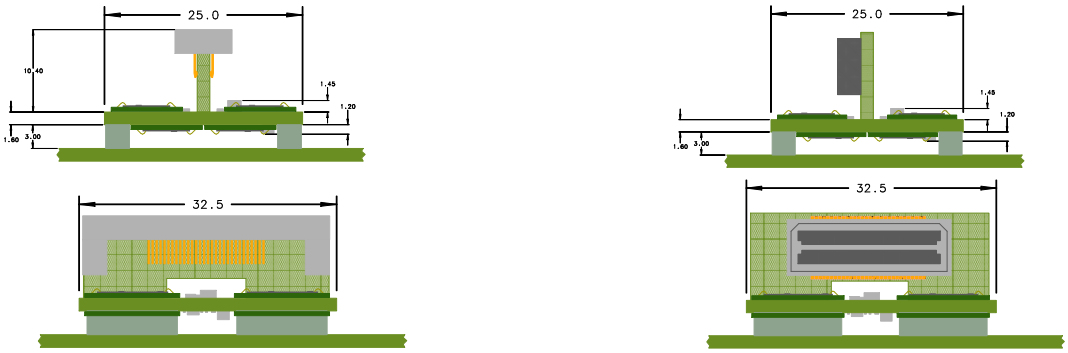

Figure 5: *Side views of the MCM-board showing two versions of the Samtec connector mounted on a vertical board glued to the top surface of the MCM-board. To the left a connector for edge mounting is used and to the right a connector for surface mounting.*

On the MCM-board there is also a DAC for setting the decay time in the preamplifier and references voltages to the SALTRO16, as well as a temperature sensor. These are controlled via an I2C bus.

The dimensions of the MCM-board, which serves 128 channels, are 32.5x25 mm^2. This corresponds to a space occupancy per channel of about 6.4 mm^2. However, also some space is needed for HV-supply

of the MPGD system and cooling of the electronics so that the available area for electronics is further reduced.

The design of the MCM-board is essentially ready but we await test results from the MCM Development Board (see Section 4.2) before the design will be finally fixed.

4.1 The CPLD

The heart of the readout system on the MCM-board is the CPLD (Complex Programmable Logic Device) chip.

There are four types of communication between the DAQ and the individual channels of an SALTRO16 chip handled by the CPLD.

- Send a command.
- Write data to a register.
- Read data from a register.
- Read the data of an event.

Most of these operations are concurrent during data taking and the control of the operations is handled via a serial link. Other controls on the MCM, which are done by the CPLD, are:

- The 8 bits for configuring the SALTRO16 preamp/shaper.
- Controlling the power pulsing of the SALTRO chip.
- Sending error and status messages to the DAQ

Tasks that do not need to involve the CPLD are foreseen to be done via the I2C communication from the 5to1-board through the LV-board. These operations include:

- Serial control of the DAC to set the decay time.
- I2C communication with the temperature sensor.

The CPLD will have two I2C interfaces, one for programming the CPLD, and one in the case we decide to communicate with the CPLD via the I2C as well.

The development of the firmware for the CPLD is done by the group from Université Libre de Bruxelles. The group has already purchased a development board and has started to develop the firmware.

4.2 The MCM Development Board

The MCM-board is a very dense board and not ideal for testing, and for development and debugging of the digital readout. We have therefore decided to produce a bigger MCM Development Board with a size of 210 x 145 mm^2, which will contain only one SALTRO-chip but the full digital readout functionality. It will be a stand alone board, also including the necessary voltage regulators and with testpoints and connectors for connecting a logic analyzer.

The MCM Development Board is an 8-layer board of which 3 layers are signal layers and 5 power layers. This indicates the complexity of the power lines due to the many different power levels which are needed. The board will house one SALTRO16-chip in QFP package and the other components, planned to be on the MCM Development Board, in sizes suitable for lab work.

The PCB has been delivery and will be followed by the mounting of components in Lund.

5 The Low-Voltage Board

The LV-board provides low voltage for five MCM-boards. Each MCM-board requires eight different voltage levels and thus the LV-board contains 8x5 = 40 voltage regulators. The communication with the CPLD and the I2C bus on the MCM is transmitted through the LV-board. There are five LV-boards per pad module. The board contains I/O registers to switch on/off the regulators, ADCs to monitor voltages and currents, and a temperature sensor.

Although the width of the board is given by the dimensions of the pad module, the depth has essentially no limitation. We investigate the possibility to connect the boards directly to the MCM-board without using cables, which would probably simplify the assembly of the system and provide closer and better grounding. A schematic view of such an arrangement is shown in Figure 6.

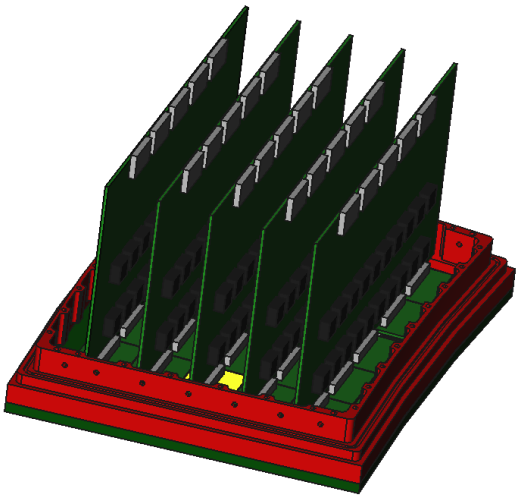

Figure 6: *LV-boards mounted directly on MCM-boards.*

The design is ready and we are waiting for the tests results with the Low Voltage Prototype Board (see Section 5.1), and the final dimensions of the board, defined by the mechanichal support structure, has to be fixed before the PCB can be ordered.

5.1 The Low-Voltage Prototype Board

The LV Prototype Board provides voltage for one MCM-board and is used to develop the LV-board. Further, it will provide voltage to the Test Socket Board for testing the SALTRO16-chips on the Carrier Boards, using the Test Socket. It will also be used to test the I2C communication between the Detector Control Boards (see Section 6) and the MCM Development Board.

The LV Prototype Board, shown in Figure 7, is currently being comissioned.

6 The Detector Control System

In order to control and monitor the LV-boards and the MCM-boards, we have designed two boards, a master control and one slave module (called 5to1) both containing microprocessors. The slave module contains one microprocesser per LV-board for one pad module. The master board contains

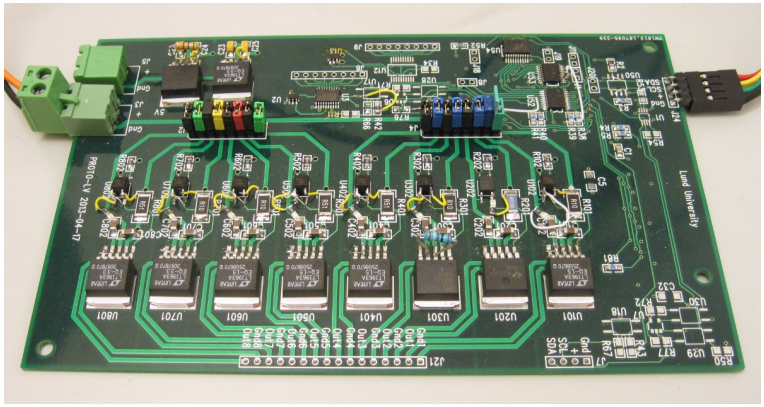

Figure 7: *The LV Prototype Board.*

one microprocessor only and can communicate with up to four 5to1 boards. A schematic drawing of the system is shown in Figure 8.

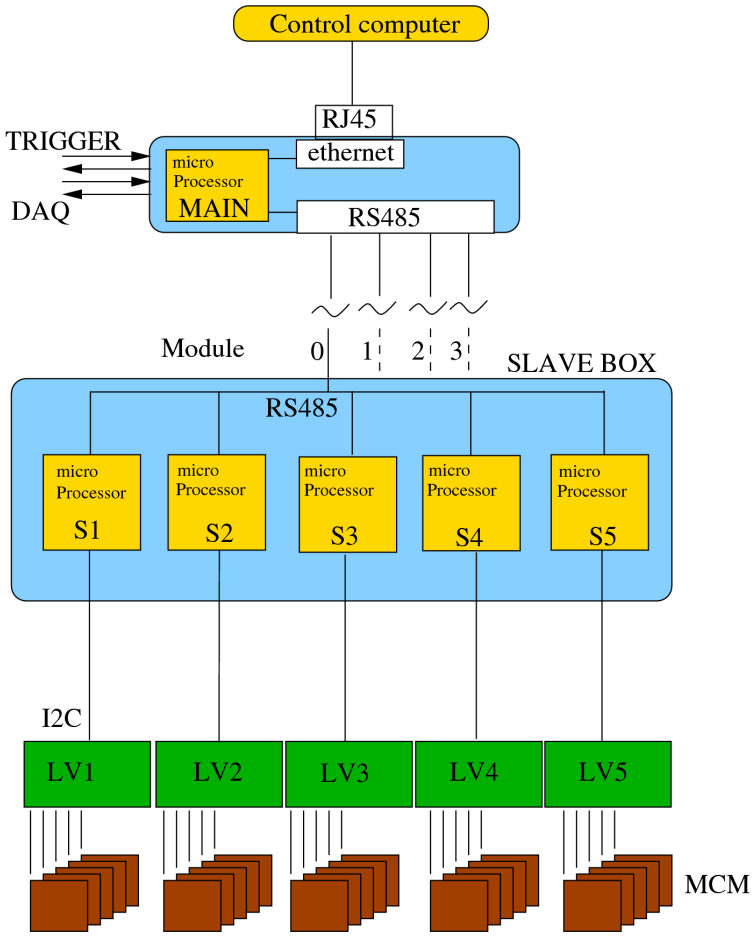

Figure 8: *A schematic drawing of the Detector Control System.*

Both the master board and 5to1 boards, shown in Figure 9, are ready and are being tested.

We plan to monitor about 700 parameters from the LV- and MCM-boards per module. For this we are proposing to use DOOCS, which is already used by the DESY LCTPC-group with good experience.

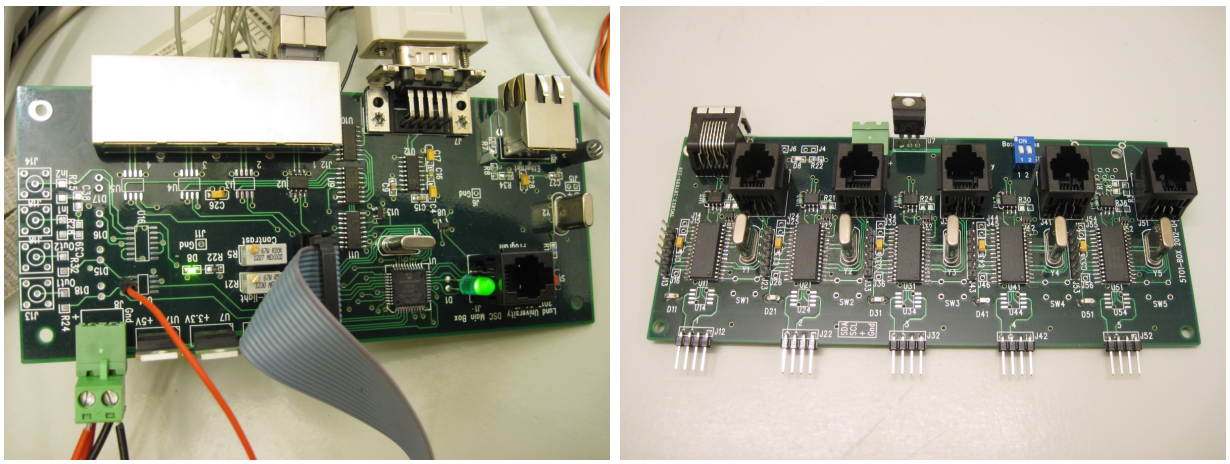

Figure 9: *The master board (left) and the 5to1 board (right).*

Oliver Schäfer from Rostock University has agreed to install our system into DOOCS. Software for the system is currently being developed.

7 Readout of a Pad Board

Figure 10 shows how a pad panel with 25 MCM's are arranged in a 5x5 matrix i.e. they contain 3200 channels in total. This leads to pad sizes of about 1x8.5 mm^2. This layout has been judged to give sufficient room for cooling and HV connections. Most likely, a final solution will have to leave about the same area of a pad panel for HV, cooling and other services. So, to fit the readout electronics inside a 17.0x13.0 cm^2 rectangle, with the present module size, is a reasonable design goal also for the final system and to place the MCM-boards in regular rows and columns to simplify the construction of the cooling system.

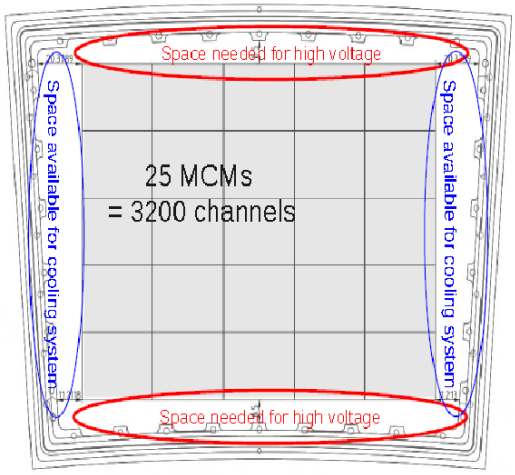

Figure 10: *The layout of the MCM-boards on a pad module with spaces for HV connectors and cooling indicated.*

8 The DAQ-system

For the readout of the MCM-boards and communication to the DAQ we will use serial readout. The functionality needed locally in the vicinity of the MCM-board is the serial to parallel conversion of the downloaded data and the parallel to serial conversion of the uploaded (readout) data. This is accomplished by the CPLD chip and there are chips which have enough logic gates to serve the purpose and which fit on the MCM-board itself.

Serial high speed readout has become possible with the development of a new generation of FPGA's that provide serial interfaces supporting data rates of several Gbit per second. A rather general purpose serial connection suitable for many experiments is the SRU (Scalable Readout Unit) developed by the RD51 collaboration. We plan to use the SRU to directly communicate with the MCM via the Data Trigger Control (DTC) link, which contains clock, trigger/control and data. However, this requires that the FPGA firmware on the SRU is adapted to include also the customized communication to and from the MCM.

8.1 The SRU

One SRU can handle 40 MCM-boards. The DTC protocol uses the four pairs of leads in the RJ45 cable for the fast signals. The solution reading the MCM-boards directly to the SRU is the cheapest as it uses commercial hardware.

It is not yet decided in the readout software what kind of commmunication will used between the SRU and DAQ computer. Two possibilities are considered, either to use ALICE DATE with the DDL optial link or direct readout using optical ethernet.

One SRU with power box and cables have been purchased and delivered. The necessary modification of the firmware for the SRU will be made by Fan Zhang from Wuhan University in China, who has developed a similar firmware for the SRU used to read out the ALICE electromagnetic calorimeter. She has been invited to visit Brussels in the period 5 - 25.1.2014, to work in close collaboration with Yifan Yang, who is writing the firmware for the CPLD.

9 Tests of the MCM-boards without an SRU

Considering that the firmware for the communication between the MCM-boards and the SRU will not be ready before some time in 2014, we are discussing to build a simple system to be able to test the readout of the MCM-boards without having an SRU.

10 Mechanics

The aim is to find a solution that satisfies the needs of everything that is attached to the padplane (electronics with cables, HV-cables, cooling etc.) The idea is to have an open but rigid Aluminum structure with guide rails to position the connectors of the LV-boards into the the connectors of the MCM-boards. The open structure will provide good access during the mounting procedure. The LV-board has to be cooled but the design of such a system has still to be worked out. The total power consumption per LV-board is 22 W.