LP TPC DAQ

Present understanding and plan

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Based on the ALICE TPC readout

Front End Card (FEC), modified for new amplifier
Readout Control Unit (RCU), Source Interface Unit (SIU)
ReadOut Receiver Card (DRORC), Destination Interface Unit (DIU)
ALICE Data Acquisition and Test Environment (DATE)
Trigger Timing Control (TTC)

EUDET: 1 RCU
10000 ch: 4 RCU
possible to distribute 1 RCU system
Modified Front End Card (mFEC)

ALICE FEC:
PASA amplifier & ALTRO readout chip

Modifications:
FPGA – additional data readout
New preamplifier

Motivations:
Event number into data stream
Time synchronization with other systems etc

ALICE FEC:
PASA amplifier & ALTRO readout chip
Modifications:
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New preamplifier
Proposed Trigger Timing Control

- Get trigger from central Trigger Logic Unit
- Distribute trigger/data to mFEC & RCUs
- Distribute 40MHZ clock to RCUs
- Require: trigger timing accuracy < 1ns
Use ALICE drivers and APIs as is.
Build DAQ (readout/control) on top.
Interface to common DAQ.
SUMMARY

- Based on the ALICE TPC DAQ
- Modify the FEC for the new amplifier
- Modify the FEC for additional data
- Need to distribute trigger to RCU and trigger number to mFEC
- Need modification to the RCUs for clock/trigger (done in ALICE tests)
- Use standard DRORC and ALICE API/drivers for the DRORC
- Build our own DAQ on top
- Interface to common DAQ