Proposal for a distributor - DRAFT 0

The purpose of the distributor is to handle the communication with the Trigger Logic Unit (TLU), and distribute the trigger information to the front end electronics. The trigger is received from the TLU and an event number is read. The distributor issues the trigger to the Readout Control Unit (RCU), as well as the 40MHz clock needed by the RCUs.The distributor has the option to act as a local "TLU", it has X inputs for PM-signals, which are fed into discrimators and a trigger can be formed from a predefined pattern. The event number, and other data if needed (to be specified), is sent serially to all mFEC (mFEC is a modified version of the ALICE FEC, which has an FPGA instead of an ALTRO chip). The distributor also outputs the trigger and event number (m bits) as levels and has inputs to specify the mode of running, e.g. used by the DAQ PC. The synchronization is done with a set of busy signals. Figure 1 gives an overview of the proposed system.

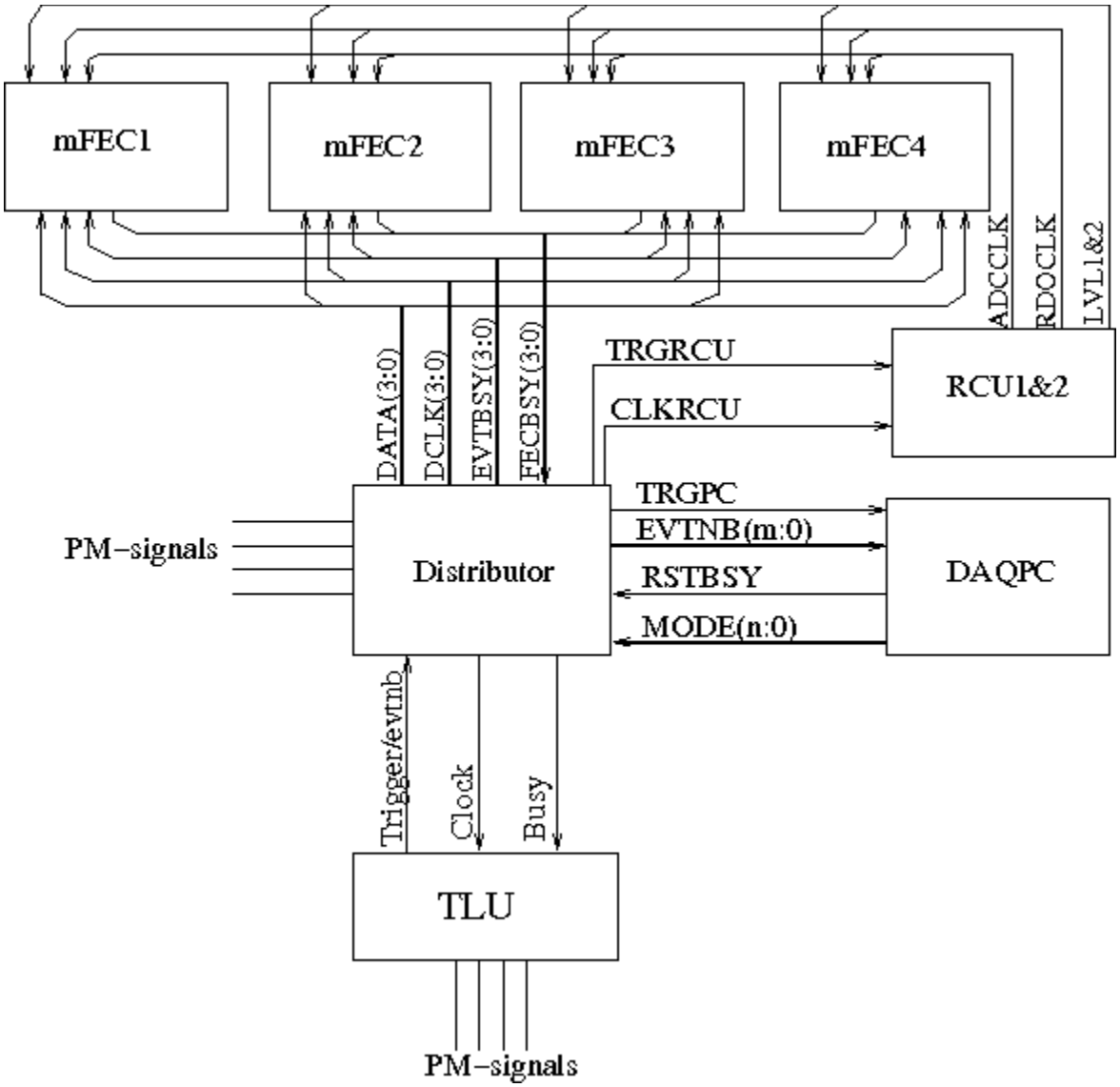


Figure 1: Overview of the proposed distributor system

Distributor signals

Signals to/from TLU:

Trigger/Eventnb	Trigger and event number	In
Clock	Readout Clock of even number	Out
Busy	System busy, asserted until readout finished	Out

Signals to RCU (one set for each RCU):

TRGRCU	Trigger to the RCUs, one to each RCU	Out
CLKRCU	40 Mhz clock to the RCUS, one to each RCU	Out

Signals to/from mFECs (one set for each mFEC):

DATA	Serial line for data	Out
DCLK	DataClock, when data on DATA is available	Out
EVTBSY	Asserted from trigger until readout finished	Out
FECBSY	Asserted by mFEC while busy with readout	In

Signals to/from host:

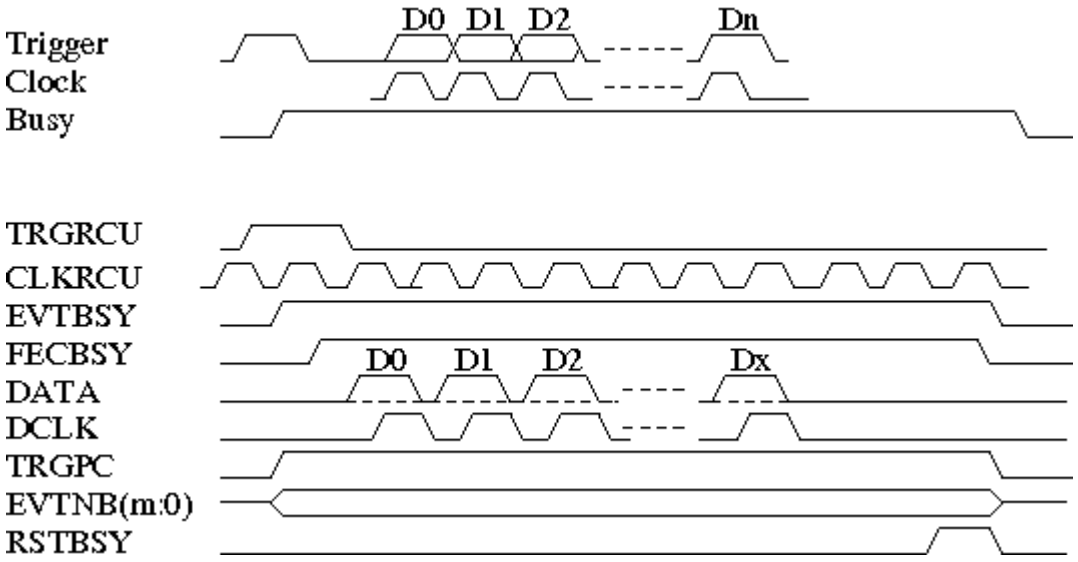
TRGPC	Trigger to host	Out (level)
EVTNB	m-bit event number	Out (levels)
RSTBSY	Pulse when host is ready	In
MODE	n-bit runmode: bit 0: enable global trigger (level) bit 1: host active (level) bit 2: enable local trigger (level) bit 3: reset (pulse)	In

Trigger data handshake

1. TLU asserts Trigger
2. On receipt of Trigger going high, the distributor: asserts Busy and EVTBSY, issues TRGRCU
3. The RCU issues LVL1 trigger to FECs, which starts the sampling in the ALTROs.
4. On receipt of Busy, the TLU deasserts Trigger and switches the Trigger line to event number
5. The distributor clocks the event number from the TLU, and collect any other information
6. On receipt of the EVTBSY (+LVL1?), the mFECs asserts FECBSY
7. The distributor clocks the data to the mFECs, asserts TRGPC and sets EVTNB
8. The RCU issues after a programmable time the LVL2 trigger, and starts reading the data.

9. After a programmable period of time (+LVL2?) and when there is a free front end buffer, the mFECs deassert FECBSY
10. The distributor deasserts EVTBSY when all FECBSY are deasserted, and if the runmode (MODE) includes the handshake with a host, when RSTBSY is asserted.
11. The distributor deasserts Busy, TRGPC, EVTNB
12. The system is ready for a trigger

Figure 2 shows a rough timing diagram of the handshake.



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